Materials Science-Poland, 40(3), 2022, pp. 125-134
http://www.materialsscience.pwr.wroc.pl/
DOI: 10.2478/msp-2022-0037

Defect-minimized directly grown graphene-based solar cells

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Using plasma-enhanced chemical vapor deposition (PECVD) to directly grow graphene nanowalls (GNWs) on silicon to preparate the solar cells is compatible with current industrial production. However, many defects in the GNWs hinder improvement of the power conversion efficiency (PCE) of solar cells. In this work, we found that the defects in GNWs can be reduced under the condition of keeping the appropriate sheet resistance of GNWs by simultaneously reducing the growth temperature and increasing the growth time. Then, a PCE of 3.83% was achieved by minimizing the defects in the GNWs under the condition of ensuring adequate coverage of GNWs on bare planar silicon. The defects in GNWs were further reduced by adding a poly(3,4-ethylenedioxythiophene) (PEDOT):Nafion passivation coating, and the PCE was significantly improved to 10.55%. Our work provides an innovative path and a simple approach to minimize the defects in graphene grown directly on silicon for high-efficiency solar cells.

Keywords: *graphene, PECVD, solar cell, defect*

1. Introduction

Graphene, as a new material, has received extensive attention from many different fields since its inception. Because of its adjustable work function [1, 2], extraordinary conductivity [3], high optical transparency, and high stability [4, 5], graphene has gained more attention in the field of photovoltaics [6, 7]. The power conversion efficiency (PCE) of crystalline silicon solar cells has reached >26% and occupied most of the market share [8], but high temperature and cost occur inevitably during the ion doping process [9]. The fabrication of solar cells with low consumption and cost is urgently needed in the industrialization of the world. Therefore, graphene-based solar cells have been developed rapidly.

The PCE of graphene-based solar cells obtained by the transfer method was rapidly improved from 1.5% in 2010 [10–12]. The efficiency of graphene/GaAs reached 18.5% as far back as 2015 [12]. However, the transfer method will lead to serious damage to graphene, such as contaminants, wrinkles, and tears [13, 14], which are bad for the cell performance and are not suitable for the current industrial development. In 2015, Liu et al. [15] first manufactured graphene nanowalls/Si (GNWs/Si) solar cells via direct growth of GNWs on the Si substrate by plasma-enhanced chemical vapor deposition (PECVD) and obtained a PCE of 3.5%. The PECVD direct growth method is compatible with the current industrialization and has excellent competitiveness. However, many defects exist in the GNWs with quite a lot of open edges, which will introduce a large number of recombination centers and damage the performance of solar cells [16]. The defects can be reduced by adjusting the growth conditions of graphene or introducing a passivation layer. Researchers were more interested in the latter, and the former seems to be neglected. Muhammad Fahad Bhopal et al. [17] and Malik Abdul Rehman et al. [18], respectively, demonstrated that the defects in graphene can be reduced by introducing HfO_2 and Al_2O_3 as an interfacial layer for the graphene/silicon

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(Gr/Si) solar cells, whereby PCEs reached up to 4.54% and 8.4%, respectively. In 2020, Malik Abdul Rehman et al. [19] reduced the graphene defects by co-doping with HNO_3 and poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) and achieved a PCE of 10.97%. In 2021, through an interfacial layer of NH_3-H_2O_2 co-passivated Al_2O_3, Kim et al. [20] exhibited a PCE of 9.49% for the direct growth graphene/Si solar cells. However, there is no research report on how to reduce defects in graphene by adjusting the growth conditions of graphene to improve the performance of Gr/Si solar cells. For graphene films rather than solar cell devices, the defects can be reduced in a straightforward way, such as by simply increasing the graphene growth time or temperature [15, 21]. However, increasing growth time or temperature will inevitably reduce the sheet resistance and transmittance. The balance relation between sheet resistivity and transmittance has been discussed in-depth for Gr/Si solar cells in previous reports [7, 15]. How to reduce the defects by improving the quality of graphene is not an easy problem under the condition of maintaining appropriate sheet resistance.

In this work, we minimized the defects in GNWs via two paths: improving the quality of GNWs itself and passivating to improve the efficiency of directly grown GNWs-based solar cells. To begin with, we demonstrated that the defects in GNWs can be reduced by simultaneously lowering the growth temperature and increasing the growth time under the premise of maintaining the appropriate sheet resistance of GNWs. Then, a PCE of 3.83% was achieved by minimizing the defects in GNWs for ensuring their adequate coverage on the bare planar silicon. Finally, the defects in the GNWs were further reduced by adding a poly(3,4-ethylenedioxythiophene)(PEDOT):Nafion passivation coating, and the PCE was significantly improved to 10.55%. This work demonstrates an innovative path and a simple approach to minimize the defects in graphene grown directly on silicon for high-efficiency solar cells.

2. Experiments

2.1. Device fabrication process

Phosphorus doped *n*-type single-crystal double-sided polished silicon wafers with a thickness of 300 ± 20 μm and resistivity of 1∼ 10 Ω·cm were used to fabricate the solar cells. Before GNWs growth, the silicon substrate was immersed in HF solution for 3 min to completely remove natural oxide, and then the silicon wafer was immersed in deionized water for cleaning and dried with inert gas. The cleaned silicon wafer was placed in the PECVD chamber to directly grow GNWs. The growth conditions were 20 W power with a continuous flow of hydrogen (H_2, 2 sccm), methane (CH_4, 20 sccm), and argon (Ar, 150 sccm) for the generation of RF ions. Different GNW samples were prepared by changing the growth temperature and time under a fixed pressure of 300 pa. The solution of PEDOT:Nafion was prepared by adding the Nafion (5 wt% in a mixture of lower aliphatic alcohols and 45% water) to the PEDOT:PSS (Clevios, PH-1000) mixed with 5 wt% dimethyl sulfoxide (DMSO) with Nafion:PEDOT ratios of 1.3 [22]. The PEDOT: Nafion coatings were fabricated using a spin-coating method at 600 rpm for 6 s and 3,500 rpm for 30 s on the GNWs. After spin-coating, the sample was annealed at 120°C for 15 min in an ambient atmosphere. Both the front electrode (Ag, 100 nm) and the back electrode (Ag, 150 nm) were deposited by magnetron sputtering with a power of 200 W and continuous flow of argon (Ar, 30 sccm), the chamber pressure was 0.005 pa, and a mask of the front electrode was used to prepare the H-shaped gate line pattern.

2.2. Characterization

High-resolution atomic force microscope (AFM, Bruker, Germany) was used to measure the thickness of GNWs and observe the surface of GNWs. Raman spectroscopy (Jobin-Yvon HR800 Raman spectroscopy) with a wavelength of 532 nm was used to analyze the microstructure characteristics and crystal quality of directly grown GNWs under different experimental conditions. To analyze the photovoltaic performance of GNWs/Si

schottky junction solar cells, the semiconductor parameter analyzer (Agilent b1500-a) was used to measure the current density voltage (J–V) in the AM1.5 solar simulator. The system spectral response, that is, external quantum efficiency (EQE) of GNWs/Si schottky junction solar cell devices at 300-1200 nm was measured using a crowntech 1000 ADX QE device. The morphology characteristics of the GNWs before and after adding PEDOT:Nafion coatings were observed by field emission scanning electron microscopy (FESEM, FEINova Nano SEM450). The optical transmittance and reflectance spectrums of the GNWs before and after adding PEDOT:Nafion coatings were collected using an ultraviolet-visible spectrophotometer (UV-Vis, Hitachi U-4100) equipped with an integrated sphere. Ultraviolet photoelectron spectroscopy (UPS) was performed to identify the change in work function after adding PEDOT:Nafion coatings using a Thermo Scientific Escalab 250Xi photoelectron spectrograph (He I, 21.22 eV). The sheet resistivity of all samples was measured using a four-probe tester (M-3 Mini type four-probe tester).

3. Results and discussion

By simultaneously changing the growth time and temperature, four GNW growth conditions with the appropriate sheet resistance (about 1.3 kΩ/sq) are obtained, which are 610°C – 70 min, 600°C – 80 min, 590°C – 100 min, and 580°C – 120 min, respectively. The specific sheet resistance after adjustment is shown in Figure 1A. For the sake of contrast, the optimized sheet resistance of graphene and the performance of the highest-efficiency cells in previous reports are summarized in Table 1. The sheet resistance of graphene of these highest efficiency cells is generally between 0.8 kΩ/sq and 1.6 kΩ/sq; the sheet resistance (about 1.3 kΩ/sq) of GNWs in the present work is also in this range.

Raman spectrum is an essential tool for graphene research [16, 24, 25]. The Raman spectra of graphene grown directly on bare polished silicon at different growth temperatures are shown in Figure 1B. All samples have three Raman peaks: D peak 1,344 cm^{-1}, G peak 1,580 cm^{-1}, and 2D band around 2,687 cm^{-1}. In addition, the acromion (G′ peak 1,618 cm^{-1}) can also be seen. The G′ and D peaks indicate the structural disorder and defects in graphene. The ultimate nature of graphene can be confirmed by the 2D band and the G peak reveals the pairs of graphene [16, 26–28]. The I_D/I_G ratio is often used to evaluate the defect density in graphene. As shown in Figure 1C, with an increase in growth temperature and a reduction in growth time, the value of I_D/I_G increases, implying more defects and poorer quality of GNWs. The lowest value (1.02) of I_D/I_G indicates minimum defects at 580°C – 120 min. At 590°C – 100 min, 600°C – 80 min, and 610°C – 70 min, the values of I_D/I_G are 1.41, 1.43, and 1.72, respectively. The decreasing tendency of I_{2D}/I_G (from 0.51 to 0.41) with a decrease in growth time and increase in growth temperature implies a reduction in GNW thickness.

The surface morphology of the GNWs with the simultaneous variation of growth temperature and growth time is revealed by the test result of AFM in Figures 1D–1G. The thickness of GNWs is decreasing with a decrease in the growth time and increase in the growth temperature, which is in good agreement with the results of Raman spectrum. The thickness of the GNWs reaches >100 nm at 580°C – 120 min, while the coverage of the GNWs on the silicon surface is low. With an increase in the growth temperature and a decrease in the growth time, the coverage of GNWs increases. At 600°C – 80 min, GNWs has almost covered the whole surface of the silicon wafer. When the experimental condition is 610°C – 70 min, the GNWs cover the whole silicon surface and the thickness of GNWs is only >60 nm.

To ensure repeatability and reproducibility, multiple (not less than 8 in each group) solar cells were prepared and tested, and the results are shown in Figure 1H. With the increase in growth temperature and decrease in growth time, the efficiency increases first and then decreases. The defects in GNWs are least at 580°C – 120 min, but the PCE (2.26%) of the solar cell is the lowest. It is easy to infer that the lowest PCE is due to the low coverage of GNWs and discontinuous film. With the increase in growth time and reduction in growth tempera-

Table 1. A comparison of the present results with those of previous studies

Device structure	Active area (cm^2)	Sheet resistance (kΩ/sq)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	PCE (%)
Gr-Uncertain silicon surface [15]	0.09	0.9	0.35	28	36	3.5
Gr-micropyramidal silicon [23]	-	1.28	0.351	28.7	38	3.8
Gr-polished silicon [17]	0.3	0.8	0.4	21.99	34.79	3.5
Gr-polished silicon [7]	0.3	1.64	0.391	25.17	56.03	5.51
Gr-polished silicon [20]	0.9	3.38	0.395	18.91	42.7	3.19
Present work	0.45	1.3	0.399	23.1	41.52	3.83

PCE, power conversion efficiency

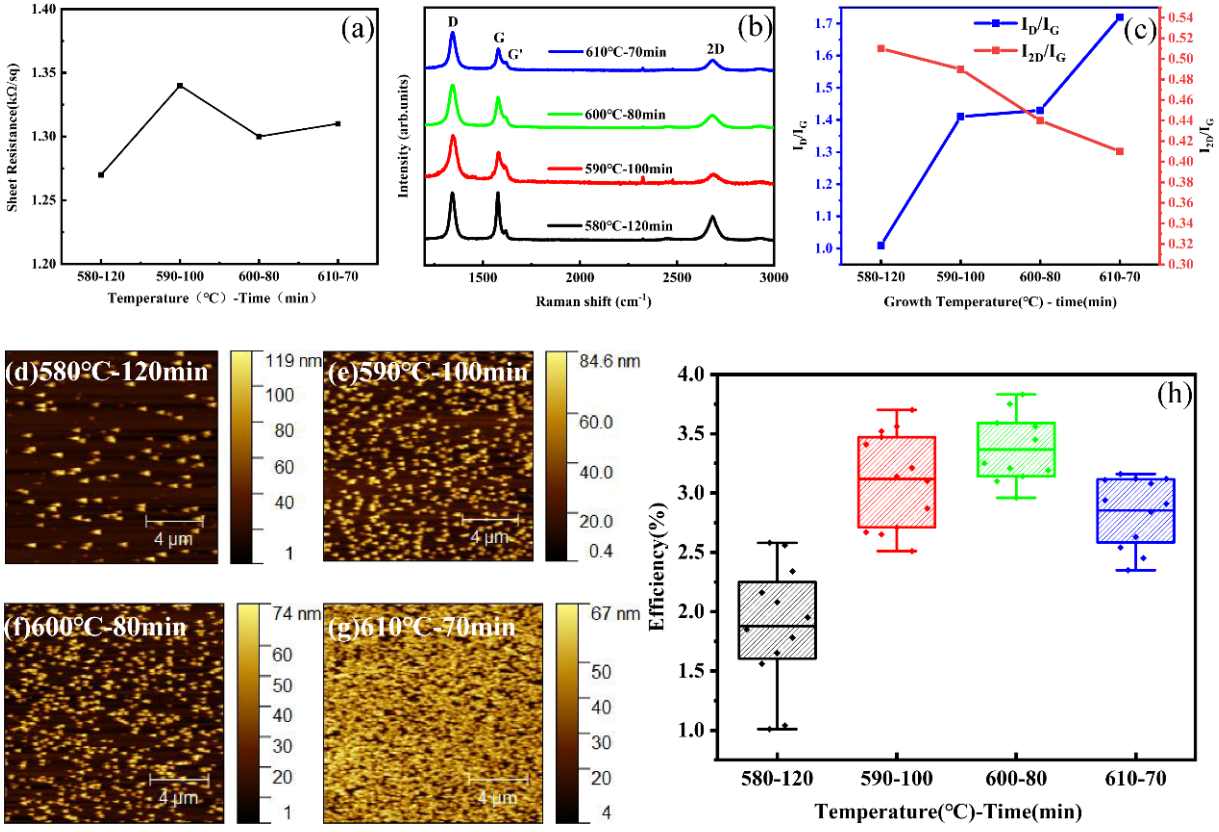

Fig. 1. The characterization is obtained when GNWs are grown at different growth temperatures and growth times. **(A)** Sheet resistance of the GNWs. **(B)** Raman spectra of the GNWs. **(C)** I_D/I_G ratio (blue curve) and I_{2D}/I_G ratio (red curve). **(D–G)** AFM image of the GNWs. **(H)** the efficiency distribution of the GNWs/Si solar cells. AFM, atomic force microscope; GNWs, growth graphene nanowalls

ture, although the defects increase, the efficiency is significantly improved because of the increase in the coverage of GNWs. The efficiency reaches up to 3.6% at 590°C – 100 min, and the highest efficiency of 3.83 is achieved at 600°C – 80 min. From 600°C – 80 min to 610°C – 70 min, the coverage no longer plays a major role in affecting the cell performance. Concurrently, the conclusion that defects in GNWs increase can be confirmed on the basis of the significant increase in the I_D/I_G ratio from 1.43 to 1.72 (Figure 1C), which leads to a noticeable decrease in PCE.

Devices with the highest efficiency in each experimental group were selected for further study.

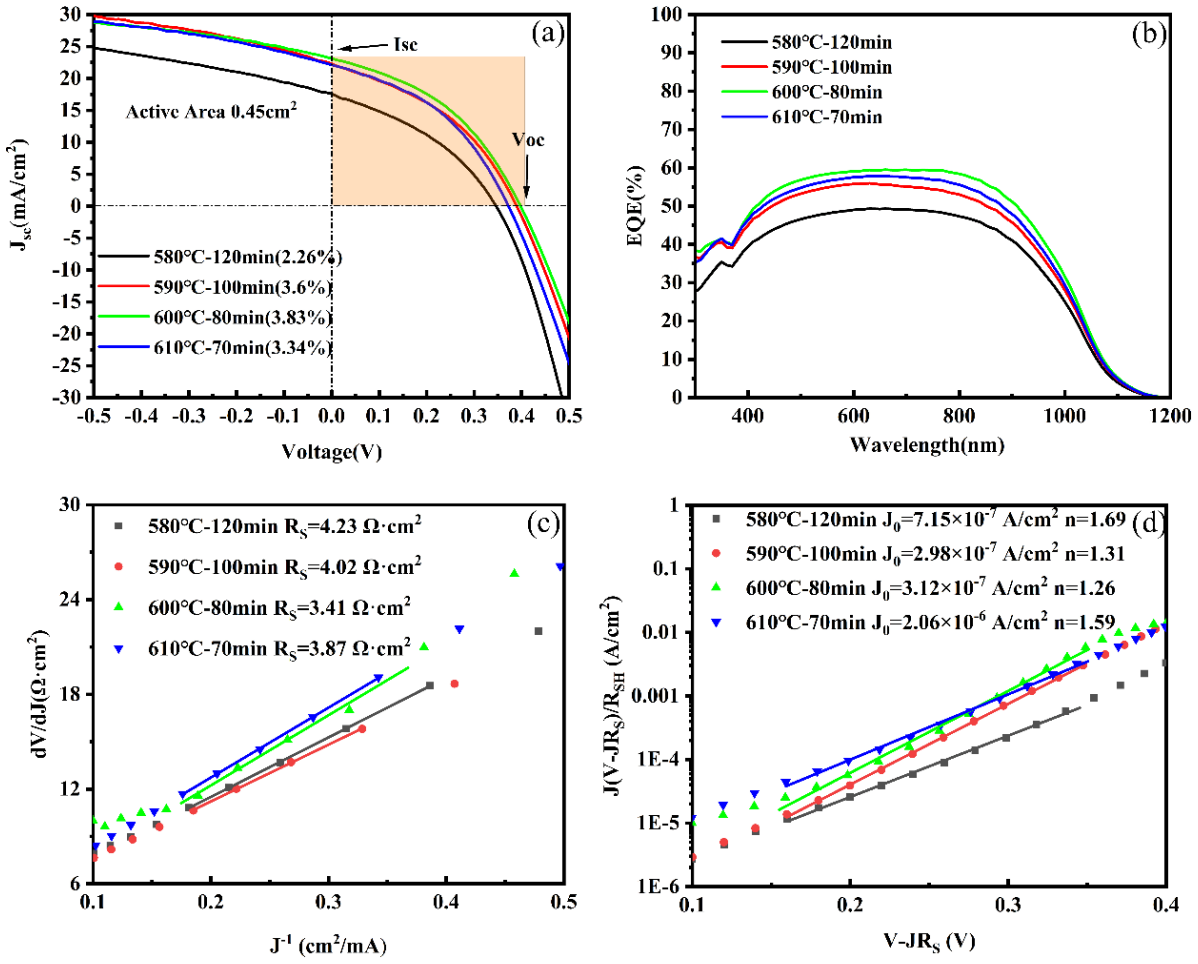

Fig. 2. Comparison of photovoltaic characteristics and performance parameters under different growth temperatures and growth times of direct-grown GNWs on bare silicon. **(A)** Light J–V characteristics of GNWs/Si solar cells. **(B)** EQE spectra of GNWs/Si solar cells. **(C)** The extraction of series resistance by plotting dV/dJ vs. J^{-1} in forward bias region. **(D)** The extraction of ideality factor n and reverse saturation current density J_0 by plotting $\log[J + (J–VR_S)/R_{SH}]$ vs. $(V\text{-}JR_S)$ near forward bias region

Table 2. Parameters and photovoltaic properties of GNWs/Si solar cells under different growth temperatures and growth times

Temperature (°C) – time (min)	**V_{oc} (V)**	**J_{sc} (mA/cm²)**	**FF (%)**	**PCE (%)**
580 – 120	0.346	17.51	37.28	2.26
590 – 100	0.391	22.25	41.39	3.6
600 – 80	0.399	23.1	41.52	3.83
610 – 70	0.37	22.1	40.9	3.34

GNWs, growth graphene nanowalls, PCE, power conversion efficiency

The I-V curve and the EQE are shown in Figures 2A and 2B; there is a good correspondence between the two groups of results. The performance parameters V_{oc}, J_{sc}, FF, and PCE are illustrated in Table 2.

The quality of the diode can be evaluated by characterizing the dark J–V. The J–V relationship can be described as [29]

$$J = J_0\left\{\exp\left[\frac{q}{AkT}(V - JR_S)\right] - 1\right\} + \frac{V - JR_S}{R_{SH}} \quad (1)$$

where J_0 is the reverse saturation current and n is

the ideality factor of the device, q is the electric charge, T is the absolute temperature, and K is the Boltzmann constant. Eq. (1) is insoluble, but the device parameters can be approximately extracted by some algorithms [29]. Ignoring 1 in the parentheses and assuming R_{SH} is infinite, Eq. (1) can be simplified as [29]

$$\frac{dV}{dJ} = R_S + \frac{AkT}{q} J^{-1} \tag{2}$$

By plotting dV/dJ vs. J^{-1} in the forward bias region, as shown in Figure 2C, R_S and n can be extracted. The R_S of the device at 580°C – 120 min is the highest, which could be due to the discontinuity of conductive channels due to the low coverage of GNWs. R_S decreases with an increase in growth temperature. When the growth temperature reaches 600°, R_S decreases to the lowest value at $3.41 up\Omega{\cdot}cm^2$ as the GNWs have almost covered the entire surface of the silicon wafer. Here, the n is ignored because of the assumptions of R_{SH}.

Arranging Eq. (1) again, we can get [29]

$$\log\left(J - \frac{V - JR_S}{R_{SH}}\right) = \log\frac{J_0}{e} + \frac{q(V - JR_S)}{AkT}\log e \tag{3}$$

R_{SH} may be obtained from the slope near $0V$ in the dark J–V curve. R_S has been extracted from the above results. By plotting $\log[J - (J - VR_S)/R_{SH}]$ vs. $(V - JR_S)$ near the forward bias region, as shown in Figure 2D, J_0 and n can be extracted.

At 580°C–120 min, the defects in GNWs are the least; however, the highest n and higher J_0 are obtained due to the high R_S as the low coverage of GNWs. The high R_S not only directly results in the high n and low FF, but also leads to high J_0 and low V_{oc} as the high R_S enhances the recombination rate. Besides, the low light absorption of silicon due to thicker GNWs leads to a reduction in J_{sc}. Compared with 580°C – 120 min, the n and J_0 decrease and the FF and V_{oc} improve at 590°C – 100 min, which is due to the decrease in R_S with a significant increase in the coverage of GNWs. Meanwhile, the J_{sc} increases with decreasing thickness of GNWs. The PCE was improved to 3.6%, which is only a little lower than that of 600°C – 80 min. From 590°C – 100 min to 600°C – 80 min, the carrier recombination center increases with an increase in GNW defects, while the reduction of R_S indicates that carrier recombination will be inhibited, making n slightly lower and J_0 close. The thinner thickness of GNWs ensures the higher J_{sc}. Therefore, PCE at 600°C – 80 min is higher than that at 590°C – 100 min. When the experimental condition is 610°C – 70 min, according to the high I_D/I_G ratio and high J_0, we infer that an increase in GNW defects leads to a significant drop in V_{oc}, resulting in a reduction in PCE. In summary, under the condition of ensuring adequate coverage of GNWs on silicon and appropriate sheet resistance of GNWs, the PCE of GNW solar cells can be improved by concurrently reducing the growth temperature and increasing the growth time to minimize the defects in GNWs.

To reduce the defects in GNWs and further improve the performance of solar cells, the GNWs were modified by adding a PEDOT:Nafion coating with conductivity and passivation [22]. The SEM images shown in Figures 3A and 3B manifest that the thickness of PEDOT: Nafion coating and pristine GNWs are the same. The device structure diagram of the solar cell after adding PEDOT: Nafion coating is shown in Figure 3C.

Figure 4A presents a comparison of the light J–V characteristics of solar cells with the PEDOT:Nafion coating and pristine GNWs. Meanwhile, the diode quality of the sample with PEDOT:Nafion coating on the pristine GNWs is evaluated according to the dark J–V characteristic (Figures 4C and 4D). Cell performance after adding the PEDOT:Nafion coatings was improved, as V_{oc}, J_{sc}, FF, and PCE were 0.557 V, 29.56 mA/cm^2, 64.09%, and 10.55%, respectively.

From Figures 4C and 4D, we can see that the value of n decreases from 1.26 to 1.12 and the J_0 decreases nearly 65% (from 3.12×10^{-7} to 1.08×10^{-7}A/cm^2) after adding the PEDOT:Nafion coating. The decrease in J_0 indicates the reduction in GNW defects, which obviously benefited from the passivation of the PEDOT:Nafion coatings. One reason for the reduction in n is the passivation of PEDOT: Nafion coatings, another reason will be

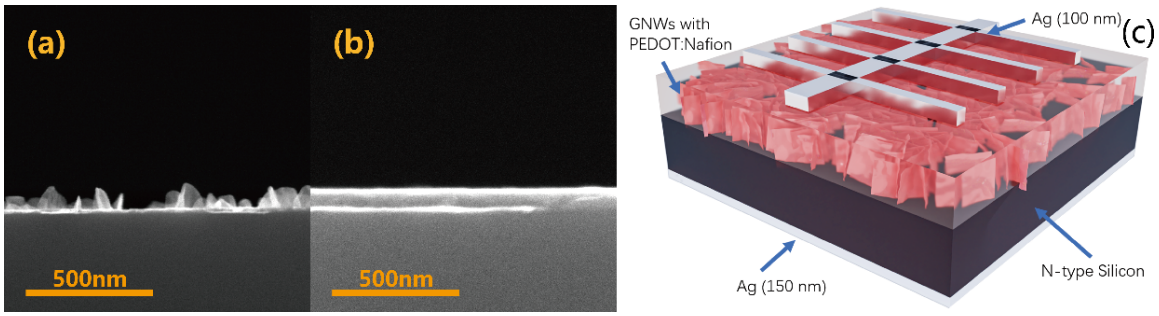

Fig. 3. SEM images of devices. **(A)** The cross-section of GNWs. **(B)** The cross-section of GNWs with PEDOT:Nafion coatings. **(C)** Device schematic to illustrate the structure of directly grown GNWs silicon Schottky junction solar cell after adding PEDOT: Nafion coating. GNWs, growth graphene nanowalls; SEM, scanning electron microscopy

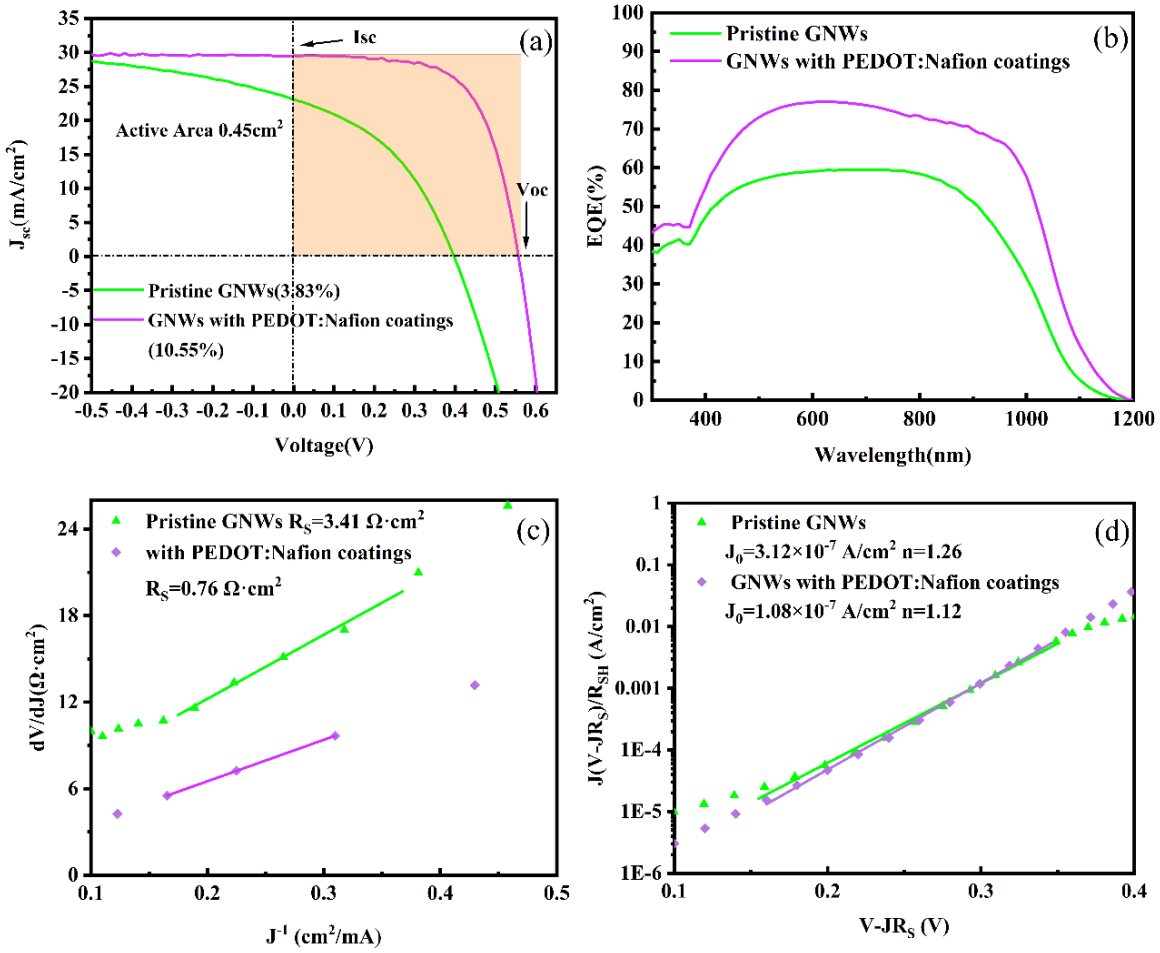

Fig. 4. **(A)** Light *J–V* characteristics **(B)** and EQE characterization of solar cells with PEDOT:Nafion coating and pristine GNWs. Dark state measurements of the GNWs/Si solar cells with and without PEDOT:Nafion coatings. **(C)** The extraction of series resistance by plotting dV/dJ vs. J^{-1} in forward bias region. **(D)** The extraction of ideality factor n and reverse saturation current density $J0$ by plotting $\log[J + (J–VR_S)/R_{SH}]$ vs. $(V–JR_S)$ near forward bias region. EQE, external quantum efficiency; GNWs, growth graphene nanowalls

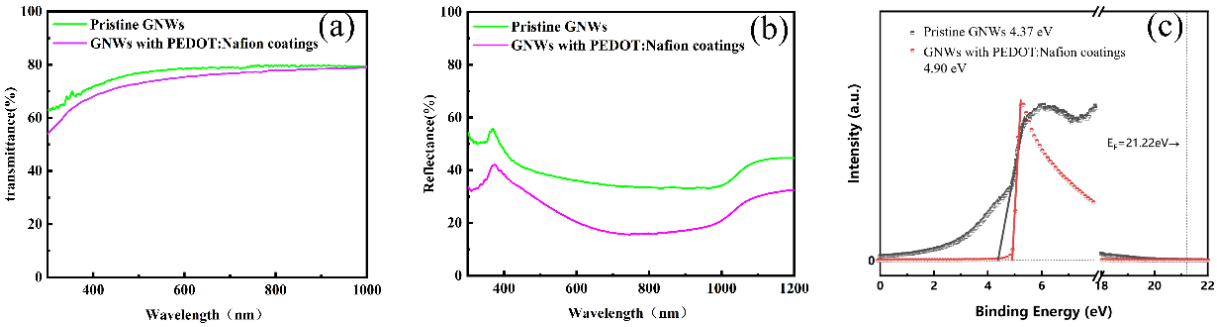

Fig. 5. **(A)** Transmittance and **(B)** reflection comparison of direct growth of GNWs and GNWs with PEDOT:Nafion coatings. **(C)** UPS results of GNWs with and without PEDOT:Nafion coatings. GNWs, growth graphene nanowalls; UPS, ultraviolet photoelectron spectroscopy

given in the following. The decrease of J_0 and n indicates that the V_{oc} and FF are improved. In addition to passivation, the PEDOT:Nafion coatings have many other functions in improving the cell performance. On one hand, the thin PEDOT:Nafion coating not only guarantees high transmittance (Figure 5A), but also greatly reduces the reflectivity (Figure 5B). The reflectivity of the sample with PEDOT:Nafion coating could be as low as $\sim$ 17% in the range of 550-1000 nm. Clearly, the enhanced J_{sc} is mainly related to the increment of light absorption, because the PEDOT:Nafion coating reduces the reflectivity. On the other hand, the UPS test results in Figure 5C show that the work function of GNWs was increased from 4.37 eV to 4.9 eV after the addition of Nafion:PEDOT coatings, which indicates a p-doping by PEDOT:Nafion coatings. The increase in work function of GNWs would result in an increase in the built-in voltage of the GNWs/Si Schottky junction, which further increases the V_{oc}. Last but not least, as an important parameter, the sheet resistance is a great obstacle to improving the PCE of GNW solar cells. Due to the excellent conductivity of the PEDOT:Nafion coating, the sheet resistance is reduced from 1.3 kΩ/sq to 0.6 kΩ/sq. Reduced sheet resistance results in a decrease in R_S from 3.41 Ω·cm^2 to 0.76 Ω·cm^2, which further improves the n and FF on the basis of passivation.

4. Conclusion

The defects in GNWs were minimized via two paths: improving the quality of GNWs itself and passivating to improve the efficiency of directly grown GNW-based solar cells. By simultaneously lowering the growth temperature and increasing the growth time, the defects in GNWs can be reduced under the premise of keeping the appropriate sheet resistance of GNWs. The PCE of 3.83% was achieved by minimizing the defects in GNWs under the condition of making sure of adequate coverage of GNWs on the bare planar silicon. The GNW defects were further reduced by adding a PEDOT:Nafion passivating coating, and the PCE was significantly improved to 10.55%. This work demonstrates an innovative path and a simple approach to minimize the defects in graphene grown directly on silicon for high-efficiency solar cells.

Acknowledgements

This study was supported financially by the National Key Research and Development Program of China (Grant No. 2018YFB1500503-02).

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Received 2022-09-28
Accepted 2022-12-22