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Design of CMOS low noise amplifier with inductive degeneration for navigation application

Abhishek Sharma[1], Dheeraj Kalra[1], Manish Kumar[1], Rajiv Bhatia[2]

This paper presents an advanced Low Noise Amplifier (LNA) tailored for high-precision navigation applications, designed using the 180nm technology node and implemented in Cadence Virtuoso. The LNA features a single-ended amplifier configuration with cascaded NMOS transistors to achieve superior isolation and input matching through source degeneration, optimizing gain and noise performance. At 1.2 GHz, the amplifier achieves a gain of 33 dB and a noise figure of 1.3 dB. It demonstrates a 1 dB compression point of –16 dBm and a third-order intercept point (IIP3) of –10 dBm, with a power consumption of 44 mW from a 1.8 V supply. Post-layout simulations reflect a noise figure of 2.9 dB and a gain of 19.5 dB, highlighting practical design considerations. The layout area is 0.51 mm², underscoring the compact yet highly efficient design.

Keywords: Navigation Application, 180nm technology, Single-ended LNA, Source Degeneration Technique

1 Introduction

The rapid advancement in navigation systems, particularly in Global Positioning System (GPS) technology, has necessitated the development of high-performance receiver front-ends that operate with low noise and high linearity. As navigation applications increasingly rely on precise signal processing, the ability to amplify weak satellite signals while minimizing noise is critical for reliable operation. Low Noise Amplifiers (LNAs) play a pivotal role in achieving these performance goals by providing necessary gain and reducing the overall noise figure of the receiver. Serving as the first amplifying block in any receiver, LNAs significantly impact overall performance [1]. Given that signals received from the antenna are typically very weak (≈1 μVp), LNAs must effectively boost these signals while maintaining a low noise figure [2]. The growing demand for wireless communication and the emergence of IoT applications necessitate optimal LNA design to ensure robust amplification without adding significant noise [3]. Recent trends in LNA design have focused on advanced configurations and materials that enhance performance. Techniques such as multi-stage amplification, negative feedback, and the use of advanced semiconductor technologies like GaN and SiGe are becoming prevalent. These innovations allow for higher gain, improved linearity, and better thermal performance, all of which are essential in mitigating the challenges faced in navigation applications. The linearity of the LNA, often quantified by the third-order intercept point (IIP3), is crucial for preventing signal distortion and intermodulation in the presence of strong interfering signals. An ideal narrowband LNA must exhibit excellent gain, minimal noise figure, unconditional stability, and low power dissipation [4]. Specifications for LNAs in navigation systems vary based on application requirements, typically operating within frequency ranges of 0.5-8 GHz, 1-2.5 GHz, or 2.4-2.5 GHz. The noise figure can be as low as 1 dB or as specific as 1.3 dB at 2 GHz, while gain can range from 12.4 dB to 23 dB, with some designs achieving 20 dB or 22 dB. Additionally, the output voltage standing wave ratio (VSWR) is generally kept below 2, with input and output return losses of less than –10 dB. In industrial applications, NMOS transistors are commonly used for LNA designs due to their integration capabilities, which help reduce system costs and improve reliability. Recent advances in VLSI technology have scaled down the channel lengths of MOS transistors to the nanometre range, thus enhancing transit frequencies to the GHz range and reducing power consumption [5]. However, achieving an optimal balance among various performance criteria remains a significant challenge, often necessitating compromises based on specific application requirements [6].

In this paper, we present the design of an LNA utilizing modern CMOS technology for navigation applications. Inductive degeneration technique helps in improving the linearity of the circuit and also improve the input impedance matching of the circuit. These design leverages the high electron mobility and low threshold voltage of advanced NMOS transistors to achieve low noise, high gain, and power efficiency while maintaining stability. Key aspects include careful transistor sizing, biasing, and innovative matching network configurations that optimize performance across the targeted frequency range. The LNA's performance is evaluated through extensive simulations

[1]ECE Department, GLA University, Mathura, India
[2]Semiconductor Laboratory, Chandigarh, India
abhishek.sharma_ec23@gla.ac.in, dheeraj.kalra@gla.ac.in, manish.kumar@gla.ac.in, rajiv.bhatia@scl.gov.in

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using Cadence software, focusing on metrics such as gain, noise figure, input reflection coefficient S_{11}, output reflection coefficient S_{22}, and IIP3. In addition to pre-layout simulations, we present post-layout simulation results to validate the design after considering the parasitic effects introduced during layout. The LNA layout has been verified to be Design Rule Check (DRC) free and Layout Versus Schematic (LVS) verified, ensuring that the physical design meets all manufacturing constraints and accurately reflects the intended circuit design.

The structure of this paper is designed to provide a thorough exploration of the high-performance Low Noise Amplifier (LNA) for navigation applications. Sections 2 and 3 focus on the design methodology, detailing the theoretical analysis and critical parameter calculations. Section 4 presents simulation results that validate theoretical predictions and illustrate the LNA's performance. Finally, Section 5 concludes with a summary of findings and suggests potential directions for future research. Through this comprehensive analysis, the paper aims to contribute to the advancement of more efficient and reliable navigation systems.

2 Design methodology

2.1 Transistor sizing and biasing

The NMOS transistors are chosen with a width of $W = 540\ \mu m$ and a length of $L = 0.180\ \mu m$. These parameters influence the transconductance (g_m), which is calculated as follows:

$$g_m = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}} \tag{1}$$

where I_D is the drain current, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W is the width of the transistor, L is the length of the transistor.

This equation ensures that the transistors operate in the saturation region, maximizing g_m and thus improving gain and noise performance. Proper transistor sizing leads to achieving the desired gain of 33 dB and a noise figure of 1.3 dB in pre-layout simulations.

2.2 Threshold voltage

The threshold voltage V_{th} is adjusted to account for the body effect using the following equation:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{2}$$

where V_{th0} is the zero-bias threshold voltage, γ is the body bias coefficient, V_{SB} is the source-to-bulk voltage, ϕ_F is the Fermi potential. Adjusting V_{th} ensures that the transistors operate in the correct region, improving the compression point and IIP3 performance, which are crucial for linearity in high-precision applications.

2.3 Gain calculation

The voltage gain A_v of the common-source stage with inductive degeneration is expressed as:

$$A_v = \frac{g_m \cdot R_D}{1 + g_m \cdot (r_s + R_s)} \tag{3}$$

where g_m is the transconductance, R_D is the drain resistance, r_s is the source resistance, and R_s is the degeneration resistance.

For the cascode configuration, the overall gain simplifies to:

$$A_v = g_m \cdot R_D \tag{4}$$

In this design, the high g_m is achieved by selecting appropriate dimensions and biasing, while R_D controls the gain. The resonant circuit, formed by an inductor and capacitor in the upper transistor stage, provides selective frequency amplification at 1.2 GHz, ensuring the LNA achieves the target gain.

2.4 Input and output impedance

The input impedance Z_{in} with inductive degeneration is given by:

$$Z_{in} = (1 + g_m \cdot R_s) \cdot (r_{ds} \,||\, R_D) \tag{5}$$

where r_{ds} is the drain-source resistance, R_s is the source degeneration resistance.

The output impedance of the cascode amplifier is approximated as:

$$Z_{out} \approx g_m \cdot r_{ds1} \cdot r_{ds2} \tag{6}$$

where r_{ds1} and r_{ds2} are the drain-source resistances of the two cascode transistors.

By optimizing g_m and R_s, both input and output impedance are properly matched, ensuring minimal signal loss.

2.5 Noise figure

The noise figure NF is approximated as:

$$NF \approx 1 + \frac{\gamma}{\alpha g_m R_s} \tag{7}$$

where γ is the body bias coefficient, α is a proportionality factor, g_m is the transconductance.

A high g_m helps minimize the noise figure, ensuring that the amplified signal retains a high signal-to-noise ratio (SNR). This is crucial for maintaining a low noise figure, as seen in the post-layout result of 2.9 dB.

2.6 Stability and matching networks

To ensure stability, the stability factor K is calculated as:

$$K = \frac{2 \cdot (g_m \cdot R_L + 1)}{g_m \cdot R_L - 1} \tag{8}$$

where R_L is the load resistance.

For optimal impedance matching, the following equations are used for the matching network:

$$L_1 = \frac{R_{in}}{2\pi f_0} \tag{9}$$

$$C_2 = \frac{1}{2\pi f_0 Z_{in}} \tag{10}$$

where f_0 is the operating frequency, Z_{in} is the input impedance.

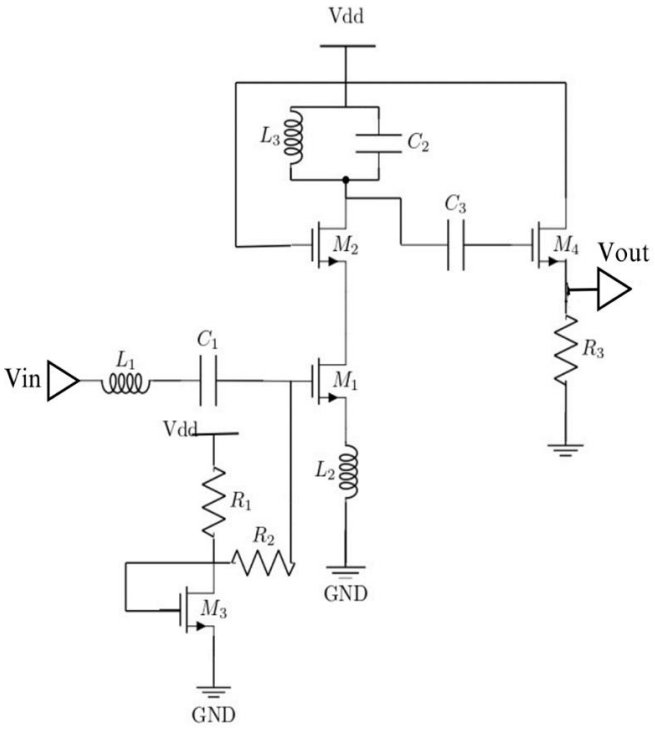


Fig. 1. Realized LNA for navigation application

3 Realized LNA circuit

The designed LNA operates by first amplifying the weak signal received from the antenna using the lower NMOS transistor configured in a common-source stage with inductive degeneration. This stage provides initial gain and sets the input impedance. The inductive degeneration involves an inductor placed at the source of the NMOS transistor, which improves linearity and stability by providing negative feedback and reducing the overall noise figure. The amplified signal is then further boosted by the cascode configuration, where the upper NMOS transistor enhances gain and improves isolation. The high transconductance $\boldsymbol{g_m}$ of the cascode NMOS transistors is pivotal in achieving the desired performance. A resonant circuit, consisting of an inductor and capacitor in parallel, is connected to the drain of the upper NMOS transistor, which helps in tuning the frequency response and maximizing gain at the desired operating frequency. An inter-stage capacitor connects the cascode stages, ensuring proper signal transfer and aiding in impedance matching. This capacitor helps in blocking DC components while allowing AC signals to pass, maintaining the integrity of the signal as it is transferred between stages. The common-drain transistor at the output stage, often referred to as a source follower, ensures that the output impedance is suitable for subsequent stages or loads. Its transconductance $\boldsymbol{g_m}$ is set to 30 mS for optimal matching, providing a low output impedance crucial for driving the next stage with minimal signal loss. The role of each component in the LNA is as follows: the lower NMOS transistor in the common-source stage provides initial amplification and sets the input impedance, with the source degeneration inductor improving linearity and reducing noise figure. The upper NMOS transistor in the cascode stage enhances gain and provides isolation between the input and output, reducing the Miller effect and increasing bandwidth. The degeneration inductor at the source of the lower NMOS transistor provides negative feedback, improving linearity and stability. The resonant circuit connected to the drain of the upper NMOS transistor helps in tuning the frequency response and maximizing gain at the desired operating frequency. The inter-stage capacitor ensures proper signal transfer between stages while blocking DC components and aiding in impedance matching. The common-drain transistor at the output stage provides low output impedance, ensuring efficient signal transfer to the next stage or load, with its transconductance set to 30 mS for optimal output matching.[11] The bias voltage (0.6 V) and 10k resistor set the operating point of the transistors, ensuring they function correctly within their active

regions. This configuration results in a high-gain, low-noise figure amplifier, suitable for navigation applications. The LNA's design is further validated through post-layout simulations, confirming its practicality and readiness for tape-out, with DRC-free and LVS-verified results.

Table 1. Design parameters of realized LNA

Transistors		Passive devices			
M1	540 µm/0.18 µm	L1	14 nH	C3	1.5 pF
M2	540 µm/0.18 µm	L2	986 pH	R1	5 kΩ
M3	15 µm/0.18 µm	L3	6.6 nH	R2	10 kΩ
M4	5 µm/0.18µm	C1	15 pF	R3	1 kΩ
		C2	1.5 pF		

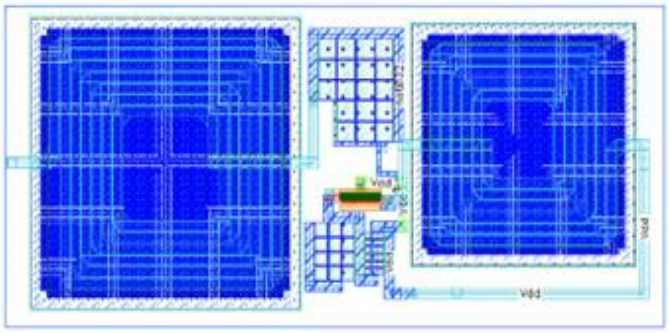


Fig. 2. Layout of realized LNA

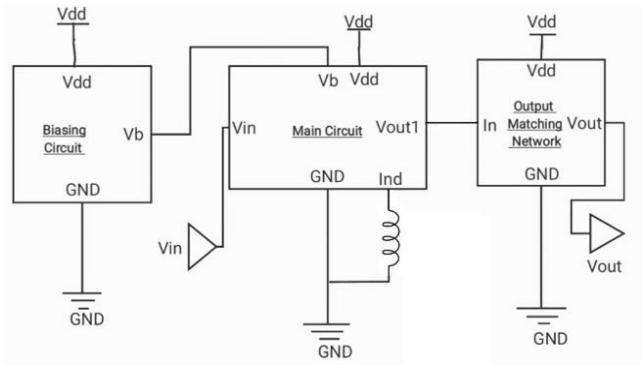


Fig. 3. Test-bench of realized LNA

4 Results

The designed LNA is implemented and simulated using Cadence software. Key performance metrics of pre-layout are summarized below:

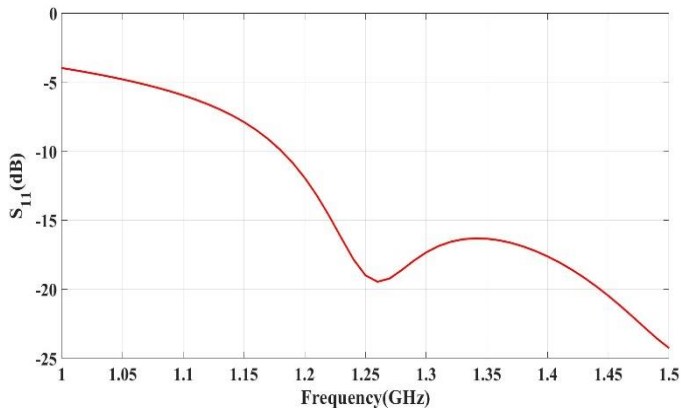
Gain: 33 dB
Noise figure: 1.4 dB
Input reflection coefficient S_{11}: –13 dB
Output reflection coefficient S_{22}: –12 dB
Operating frequency: 1.2 GHz
Power dissipation:
$P_{total}=V_{DD}\times I_D=1.8\text{ V}\times 24.8\text{ mA}=44.64\text{ mW}$

4.1 S-parameters analysis

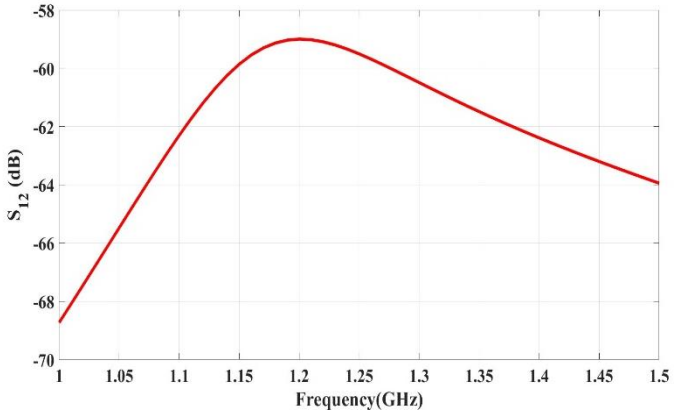
The *S*-parameters for both pre-layout and post-layout simulations have been analyzed. These parameters include S_{11} (input reflection coefficient), S_{12} (reverse isolation), S_{21} (forward gain), and S_{22} (output reflection coefficient). Additionally, results for different process corners (FF, SS, SF, FS) have been evaluated.

4.2 S_{11} (input reflection coefficient)

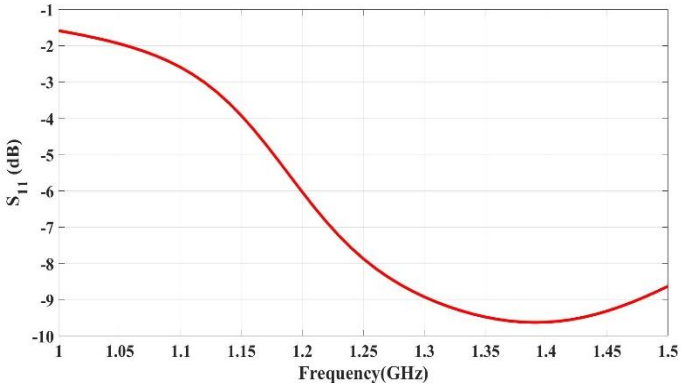
Figure 4a: The pre-layout S_{11} result shows a reflection coefficient consistently below –10 dB across the target frequency range. This indicates excellent input matching, ensuring minimal signal reflection and efficient power transfer into the amplifier. Figure 4b: Post-layout S_{11} analysis shows a slight degradation in input matching, particularly at higher frequencies. Despite this, S_{11} remains below –8 dB at 1.2 GHz, which is still accept able for the intended application, ensuring reliable operation after considering layout-induced parasitic. Figure 4c: The pre-layout process corners analysis indicates that S_{11} varies slightly across different process conditions (FF, SS, SF, FS), yet remains within acceptable limits. This demonstrates the design's robustness to variations in manufacturing processes. Figure 4d: The post-layout process corners result exhibits similar behavior to the pre-layout process corners, with minor variations in S_{11}. As mentioned in equation (5), the input impedance is dependent on the transconductance henceforth it is adjusted so that the input matching is done for 50 Ω impedance.



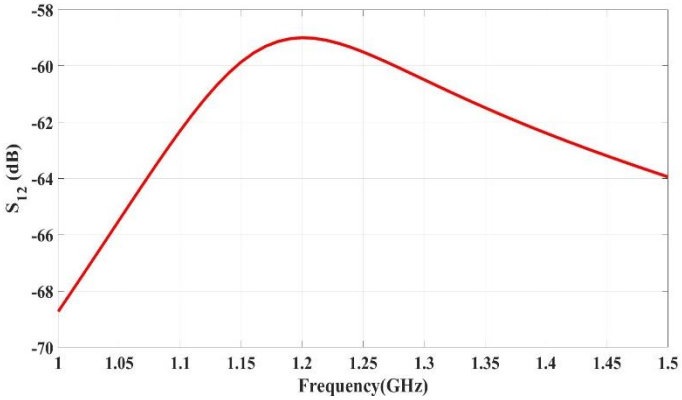
(a) Pre-layout S_{11} of realized LNA



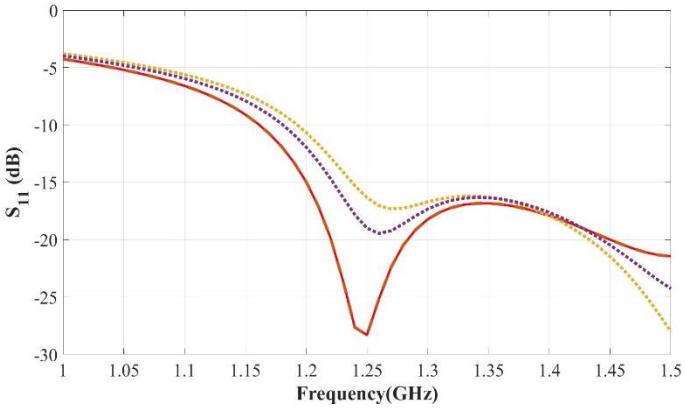
(a) Pre-layout S_{12} of realized LNA



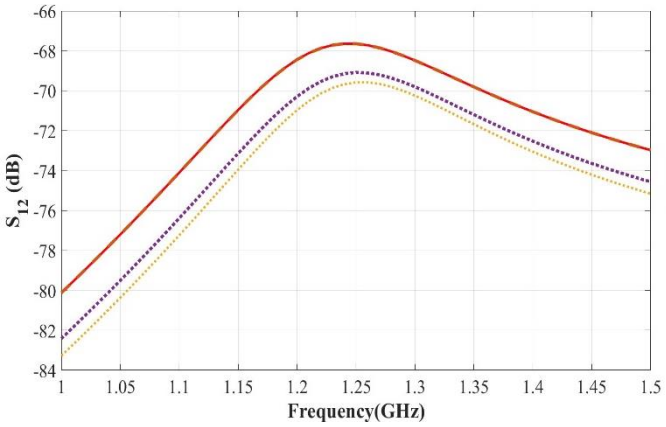
(b) Post-layout S_{11} of realized LNA



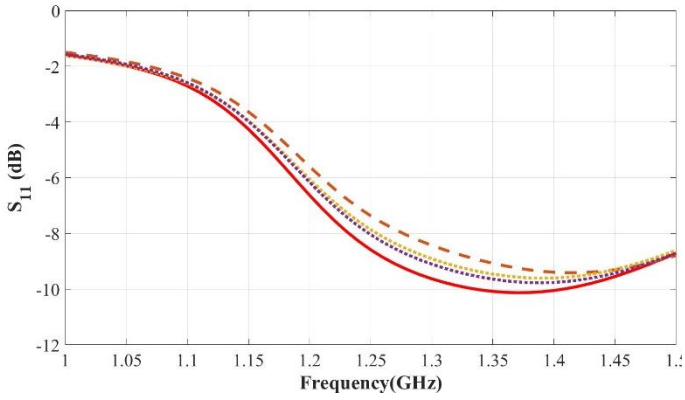
(b) Post-layout S_{12} of realized LNA



(c) Pre-layout process corners S_{11} of realized LNA

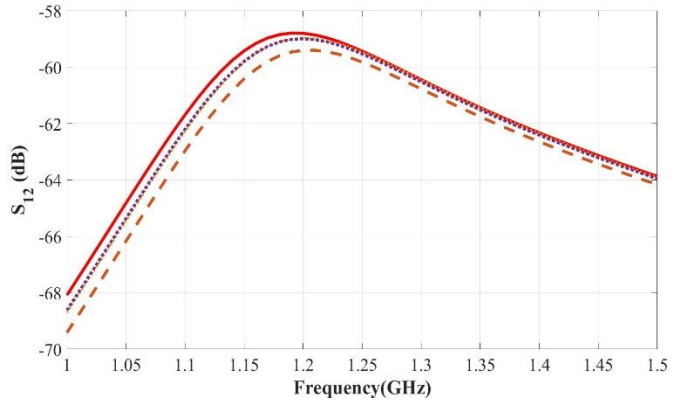


(c) Pre-layout process corners S_{12} of realized LNA



(d) Post-layout process corners S_{12} of realized LNA

Fig. 4. S_{11} (input reflection coefficient) results



(d) Post-layout process corners S_{12} of realized LNA

Fig. 5. S_{12} (reverse isolation) results

4.3 S_{12} (reverse isolation)

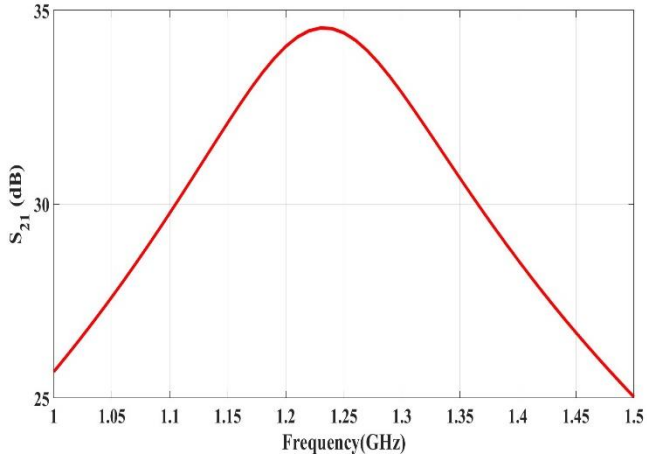
Figure 5a: The pre-layout S_{12} result shows reverse isolation consistently below –70 dB across the target frequency range, indicating excellent isolation between the output and input, with minimal feedback. Figure 5b: Post-layout S_{12} analysis also shows excellent reverse isolation, remaining below –55 dB, though slight variations are observed compared to pre-layout results. This ensures minimal feedback from output to input even after accounting for layout-induced effects. Figure 5c: The pre-layout process corners analysis demonstrates that S_{12} remains below –30 dB across different process conditions (FF, SS, SF, FS), indicating stable reverse isolation despite manufacturing varia-tions. Figure 5d: The post- layout process corners result shows that S_{12} remains consistent with pre-layout findings, maintaining excellent reverse isolation across various process conditions. As mentioned in equation (6), the output matching can be done by adjusting the transconductance and transistor sizing.

4.4 S_{21} (forward gain)

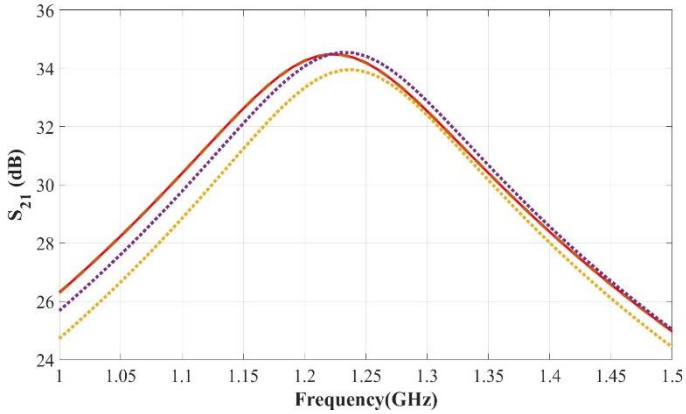
Figure 6a: The pre-layout S_{21} result demonstrates a gain of approximately 33.5 dB at 1.2 GHz, meeting the design specifications. This indicates the amplifier provides a strong amplification of the input signal before layout effects are considered. Figure 6b: Post-layout S_{21} showsa slight reduction in gain to about 19.5 dB, which is attributed to layout-induced parasitic. Despite this, the gain remains close to the design target, demonstrating good performance after layout adjustments. Figure 6c: The pre-layout process corners analysis shows that S_{21} maintains consistent gain across different process conditions (FF, SS, SF, FS), indicating robust performance before layout. Figure 6d: The post-layout process corners result shows that S_{21} continues to meet the design specifications across various process conditions, confirming the amplifier's robustness to process variations even after layout completion. The gain of realized LNA has been increased as noted from equation (3).

4.5 S_{22} (output reflection coefficient)

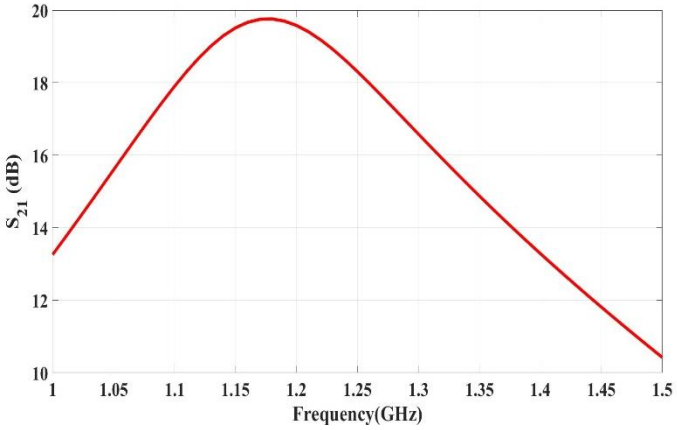
Figure 7a: Post-layout S_{22} shows a slight degradation in output matching, but re- mains below -10 dB, ensuring acceptable performance after accounting for layout effects. Figure 7b: The pre-layout process corners analysis indicates that S_{22} varies slightly across different process conditions, but remains within acceptablelimits, highlighting the design's robustness before layout. Figure 7c: The post-layout process corners result shows that S_{22} maintains performance across various process conditions, confirming that the design is resilient to process variations even after layout.



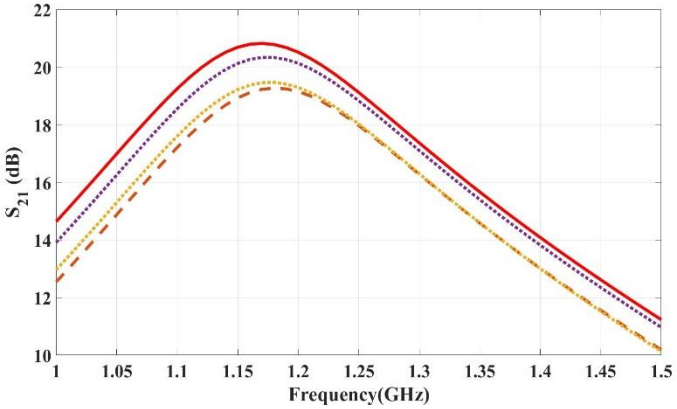
(a) Pre-layout S_{21} of realized LNA



(b) Post-layout S_{21} of realized LNA

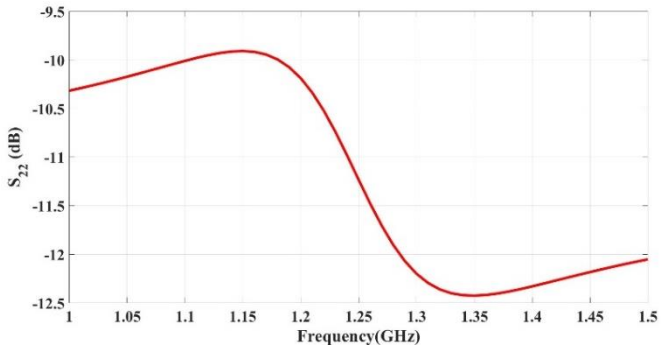


(c) Pre-layout process corners S_{21} of realized LNA

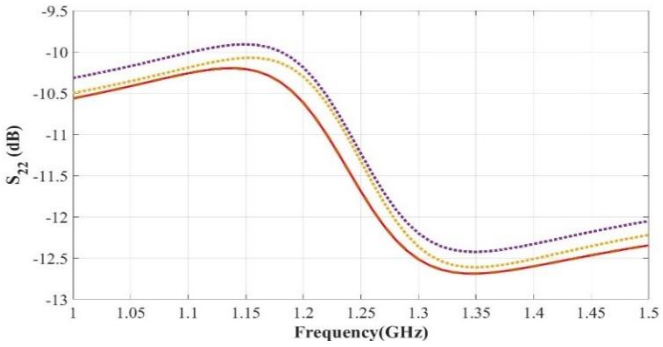


(d) Post-layout process corners S_{21} of realized LNA

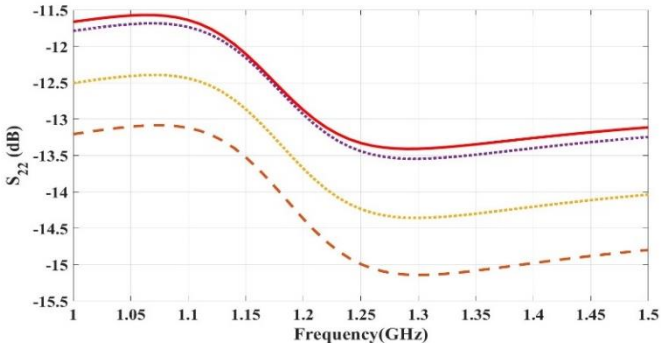
Fig. 6. S_{21} (forward gain) results



(a) Pre-layout S_{22} of realized LNA



(b) Pre-layout process corners S_{22} of realized LNA



(c) Post-layout process corners S_{22} of realized LNA

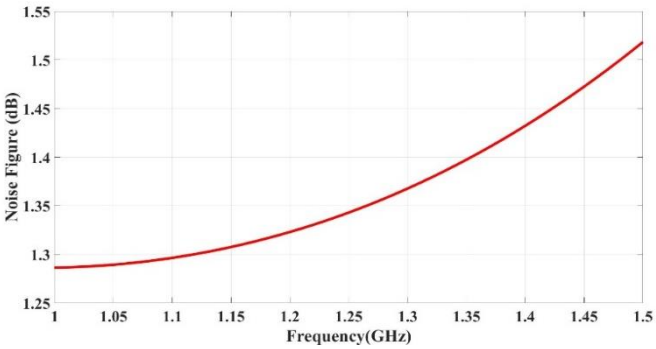
Fig. 7. S_{22} (output reflection coefficient) results

Table 2. Pre-layout corners analysis

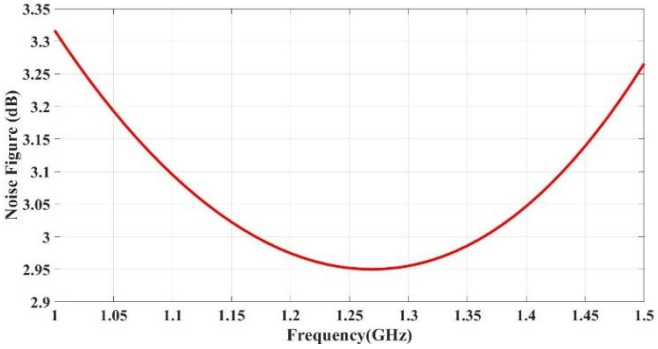
Corners	$S11$	$S12$	$S21$	$S22$	NF
Normal	–10.9 dB	–71 dB	33.1 dB	–11 dB	1.33 dB
Fast–Fast	–15.4 dB	–69 dB	33.7 dB	–12.6 dB	1.32 dB
Slow–Slow	–11.9 dB	–73 dB	32.7 dB	–12.8 dB	1.36 dB
Fast–Slow	–16.7 dB	–70 dB	33.6 dB	–12.18 dB	1.33 dB
Slow–Fast	–15.2 dB	–71 dB	33 dB	–12.4 dB	1.35 dB

5 Noise figure analysis

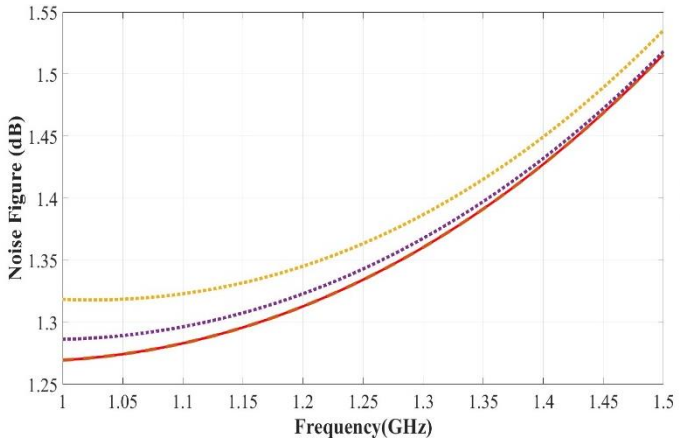
Figure 8a: The pre-layout noise figure resultshows a minimum noise figure of 1.3 dB at 1.2 GHz, which meets the design specifications for a GPS application. This indicates that the amplifier is designed to add minimal noiseto the signal before considering layout effects. Figure 8b: Post-layout noise figure analysis reveals a slight increase to 1.4 dB at 1.2 GHz. This increase is due to layout-induced parasitics and other variations but remains within an acceptable range for the intended application, demonstrating the design's performance after layout adjustments. Figure8c: The pre-layout process corners analysis shows that the noise figure varies slightly across different process conditions (FF, SS, SF, FS). Despite these variations, the noise figure remains within acceptable limits, highlighting the design's robustness before layout. Figure 8d: The post-layout process corners result shows similar behavior to the pre-layout process corners,with some variations in the noise figure across different process conditions. The noise figure remains within an acceptable range, confirming the design's robustness to process variations even after layout completion. The results demonstrate that the LNA design maintains robust performance across different process corners, ensuring reliability and consistency in various operating conditions.



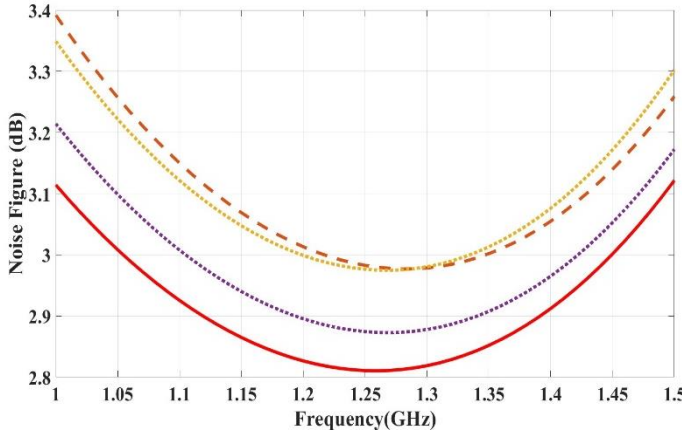
(a) Pre-layout noise figure of realized LNA



(b) Post-layout noise figure of realized LNA



(c) Pre-Layout Process Corners Noise Figure of realized LNA



(d) Post-layout process corners noise figure of realized LNA

Fig. 8. Noise figure results

6 IIP3 analysis (third-order intercept point

Figure 9: The IIP3result shows the amplifier's linearity performance with a measured IIP3 value of –10 dBm at 1.2 GHz. This measurement indicates that the amplifier can handle strong input signals with minimal distortion, which is essential for high-performance applications requiring linearity. After considering the parasitic effects introduced during layout.The layout has been verified to be Design Rule Check (DRC) free and Layout Versus Schematic (LVS) verified, ensuring that the physical design complies with manufacturing constraints and accurately reflects the intended circuit design. These verifications indicate that the LNA is ready for practical implementation and tape-out in a real foundry environment. Byaddressing all practical aspects needed for tape-out, this work provides a robust solution for the development of efficient andreliable navigation systems. The methodologies and results discussed in this paper contribute significantly to the field of RF front-end design for navigation applications

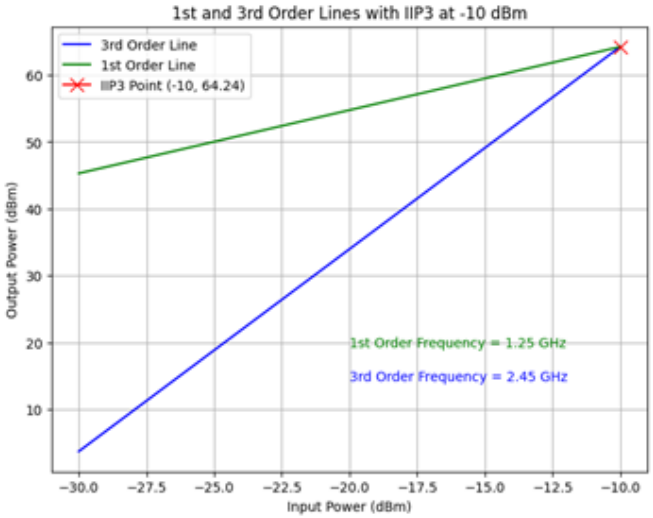


Fig. 9. IIP3 result at 1.2 GHz

7 Conclusion

The designed CMOS LNA for navigation application, using a common-source inductive degeneration configuration with cascode topology, enhances gain and reduces noise figure, making it suitable for high-performance RF front-ends. Validated through extensive Cadence simulations, the LNA achieves significant improvements in gain, noise figure, input reflection (S_{11}), output reflection (S_{22}), and IIP3. Post-layout simulations confirm that the design maintains performance, and DRC/LVS verifications ensure compliance with manufacturing constraints. Importantly, the LNA is matched to a 50-ohm termination at both input and output ports, facilitating optimal power transfer and integration with standard RF systems. This work provides a robust solution for efficient navigation system development and is ready for practical implementation.

Table 3. Comparison of this work with other references

Specification	[6]	[7]	[8]	[9]	[12]	[13]	[14]	[15]	This work
Technology (nm)	130	180	MIC	65	90	180	28	0.1InP	180
Frequency (GHz)	3.5-5.8	5	1.1-2.4	1.2-1.8	1-13.8	0.1-6	0.2-2	0.3-1.5	1.2
S_{11}(dB)	–13.1	–12.2	–15.8	–	<–11.7	<–11	<–15	>8	–6.1
S_{12}(dB)	–32	–	–	–	–	–	–	–	–59
IIP3 (dB)	–5.4	–	–	3	–13	–16	1.26	–20	–10
Noise figure (dB)	4.2	2.22	3	3.6	3.8	2.3	3.5	N. A	2.9
Power supply (V)	1.2	2.14	3	1.2	1	1.5	1	N. A	1.8
Gain (dB)	11	25.3	20.1	14-24	14.9	19	18.5	34	19.5
Power (mW)	9.36	–	108	–	7.8	7.35	4.1	255	44.64

References

[1] B. Leung, *VLSI for Wireless Communications*, Peasrson Education, Inc 1995 Edition.

[2] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, 1998.

[3] B. Razavi, *RF Microelectronics* 2007 Preview Edition.

[4] D. Kalra, V. Goyal, M. Srivastava, "Design and performance analysis of low power LNA with variable gain current reuse technique," *Analog Integrated Circuits and Signal Processing*, vol. 108, no. 2, pp. 351–361, 2021. doi:10.1007/s10470-021-01855-6.

[5] B. Razavi, "*CMOS technology characterization for analog and RF design*," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, pp. 268-276, 1999, doi: 10.1109/4.748177

[6] A. Zokaei, A. Amirabadi "A 0.13 μm dual-band common-gate LNA using active post distortion for mobile WiMAX," *Journal of Microelectronics*, vol. 45, no. 7, pp. 921–929, 2014. doi: 10.1016/j.mejo.2014.03.012.

[7] R. Kumar, M. Kumar, V. M. Srivastava, "Design and noise optimization of RF low noise amplifier for IEEE standard 802.11a WLAN," *International Journal of VLSI Design & Communication Systems*, vol. 3, no. 2, pp. 165, 2012, doi: 10.5121/vlsic.2012.3214.

[8] A. Aneja, X. J. Li, and P. H. J. Chong, "Design and analysis of a 1.1 and 2.4 GHz concurrent dual-band low noise amplifier for multiband radios," *AEU - International Journal of Electronics and Communications*, vol. 134, pp. 153654, 2021, doi: 10.1016/j.aeue.2021.153654.

[9] J. Zhu, H. Krishnaswamy, P. R. Kinget," *Field-Programmable LNAs With Interferer-Reflecting Loop for In- put Linearity Enhancement,"* IEEE Journal of Solid-State Circuits, vol. 50, no. 2, pp. 556-572, 2015. doi: 10.1109/JSSC.2014.2364835

[10] M. J. Alali, A. S. Tukkee, and M. K. Zarkani, "Design of a low noise amplifier for L-band GPS applications," *IOP Conference Series: Materials Science and Engineering*, vol. 671, no. 1, pp. 012056, 2020, doi: 10.1088/1757-899x/671/1/012056

[11] N. Yadav, A. Pandey and V. Nath, "Design of CMOS low noise amplifier for 1.57GHz," *2016 International Conference on Microelectronics, Computing and Communications (MicroCom)*, Durgapur, India, pp. 1-5, 2016 doi: 10.1109/MicroCom.2016.7522438.

[12] A. F. Khavari and K. Mafinezhad, "A New UWB LNA with 15 dB Gain in 90 nm CMOS with Current Reuse Topology," Electrical Engineering (ICEE), *Iranian Conference*, pp. 184-189, 2018 doi: 10.1109/ICEE.2018.8472556.

[13] F.S Bidabadi, S.V Mir-Moghtadaei , "An Ultra-Wideband 0.1–6.1 GHz Low Noise Amplifier in 180 nm CMOS Technology", *Journal of Circuits, Systems and Computers*, vol. 30, no. 6, pp. 2150104, 2021 doi: 10.1142/S0218126621501048

[14] A. Bozorg, R. B. Staszewski, "A 20 MHz–2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 1, pp. 42-50, 2022, doi: 10.1109/TCSI.2021.3092960.

[15] M. Lai, V. Mackay, D. Wulf, P. Shmerko, L. Belostotski, "0.3–1.5-GHz LNA With Wideband Noise and Power Matching for Radio Astronomy," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 8, pp. 1163-1166, 2023, doi: 10.1109/LMWT.2023.3272211

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