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DISTORTION ANALYSIS FOR PROGRAMMABLE ANALOG SIGNALS GENERATED USING FPGA

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Abstract. Practical applications in electrical engineering often deal with analog signals, but there are employed also digital circuits and microcontrollers. Sometimes it is easier or cheaper to improvise DA and AD converters instead of using dedicated ones. This paper is a comparative analysis of how accurate the analog signals can be generated from digital systems, like Field Programmable Gate Arrays (FPGAs) using only additional passive circuits. For this analysis, different FPGAs families were tested. Two alternatives of generating analog signals were considered in this study: PWM and R2R network. The analysis has been performed for a common frequency band, from 100 Hz to 30 kHz, using a virtual instrument for building an automated test system. At 10 kHz the PWM module obtains better THD values, reaching even 0.013% and at 30 kHz the R2R module obtains better THD values, reaching even 0.222%.

Keywords: waveform generator, PWM signal, low pass filter, digital to analog converter, R2R ladder network, virtual instrument, total harmonic distortion.

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1. Introduction

Among the specifications of an analog signal, the Total Harmonic Distortion (THD) is one of the most significant dynamic parameters for instrumentation and audio applications (Lin and Luo, 2012). The Eqs. (1) and (2) relate the calculation formulas of this parameter. In practice, THD is a measure of the content in harmonics of a sinusoidal signal. The THD measurement can be done using filters to split the signal into two parts: a signal with all of the harmonics filtered out, leaving just the fundamental frequency (V_1) and a signal with the fundamental frequency filtered out leaving all of the harmonics (V_2 to V_n).

$$\mathrm{THD} = 100 \cdot \frac{\sqrt{V_2{}^2 + V_3{}^2 + \cdots + V_n{}^2}}{V_1} \ [\%] \tag{1}$$

$$\mathrm{THD} = 100 \cdot \frac{\sqrt{V_2{}^2 + V_3{}^2 + \cdots + V_n{}^2}}{\sqrt{V_1{}^2 + V_2{}^2 + V_3{}^2 + \cdots + V_n{}^2}} \ [\%] \tag{2}$$

First equation is the percentage value of this parameter, where V_2 to V_n are the RMS voltage of each harmonic and V_1 is the RMS voltage of the fundamental frequency. The second equation uses the total RMS voltage of the signal in the denominator but both equations give close results for THD values below 10%.

The THD is 0% when a sinusoidal waveform has no harmonics components, the case of an ideal sine wave. If the THD is greater than 0%, then harmonics components which distort the signal are present (Roderick, 2021). The proposed system uses the NI USB 6251 board with 16-bit DAC resolution to test the performance of the systems being studied. Digital signal reproduction is based on sampling and Nyquist theorems. For a DAC the sampling frequency must be at least twice the value of the highest frequency from the generated signal spectrum (Gaddy and Kawai, 2000).

One of the most common DAC configurations is the R2R resistor ladder network. It uses resistors of only two different values, and their ratio is 2:1 (Zumbahlen, 2008). For this type of DAC two implementations are studied: 8-Bit and 10-Bit. For quick and simple applications the voltage output is the most suitable one, as long as in most cases the load has high impedance. Many DACs are able to supply a full-scale current of about 20 mA. Since a TTL digital output can sink 20mA, such DAC might have the same ability (Zet *et al*., 2020).

An automated test system, that does not require human intervention except for the start of the acquisition process, has been developed to drive the FPGA where the tested DAC is located. Digital electronic engineers know that

memories or address decoders can be used to implement any combinational logic function. While the memory can be written and the user can program any bytes in each location, the truth table itself of a logic function can be stored in consecutive locations (Zet and Foşalău, 2019). Once the circuit is designed and tested, it can be uploaded into the FPGA and it works. If other improvements are necessary, the design can be changed with no hardware modifications, just by uploading the new design (Lewis, 2012).

2. Generating and testing the analog signals

2.1. The hardware structure of the test system

In the present paper we proposed to perform a study on the obtainable accuracy of the analog signals generated using digital circuits. The proposed system includes the FPGA module, programmed to function as a signal generator, the additional modules that will process the analog signal and the data acquisition board that will display on the computer the results of acquisition process.

There are 2 ways of generating analog signals without a specialized DA converter: through a PWM signal at a digital output pin and a passive RC filter, with the name Low Pass Filter or using a R2R network, with the name R2R module, driven directly by the digital output pins, which can be found in Fig. 1. The analog output of Low Pass Filter or of R2R module, called $V_{out-nbit}$ in the Eq. (3), is connected to the analog input of the data acquisition board.

The generated analog signals are acquired using a NI USB-6251 board, analyzed and processed with a virtual instrument. It has 16-bit ADC resolution, maximum sampling frequency of 1.25 MS/s and the input voltage domain from ±0.1V to ±10V in several ranges. Both analog signals (PWM and R2R) are acquired using two analog inputs and sampled at the maximum frequency. The test is automated, running from the minimum frequency to the maximum one, ruled by a virtual instrument developed in LabView, which uses a single ended non referenced (NRSE) input configuration. It programs the current signal frequency generated by the FPGA, it acquires a window from the two generated signals, it process the acquired data and save the results in file. The frequency is programmed using a serial synchronous interface with 3 digital IOs of the DAQ card. The digital levels of the DAQ card are TTL compatible, while some FPGAs have different level (3.3V). In order to solve the problem, a level adapter has been used to translate the logic levels.

The FPGA board is programmed depending on the additional module. So, the "out" output of the "pwm" block (see Fig. 4) will be used for Low Pass Filter and the "sin[7..0]" outputs of "sinus signal" block (see Fig. 4) will be used to drive the R2R module.

Fig. 1 shows the block diagram of the test system.

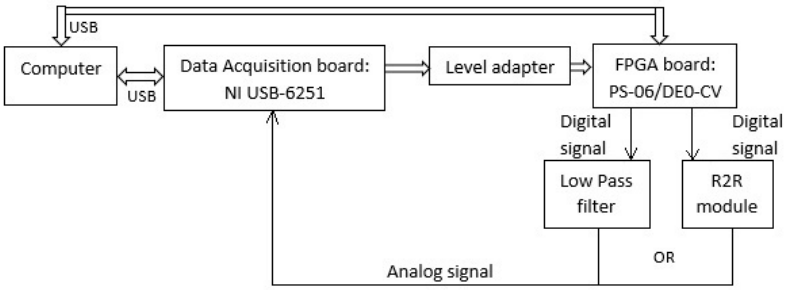


Fig. 1 – Hardware system overview.

2.2. The digital hardware architecture of the signal generator

The analog signals are generated using two methods: a PWM signal generated using a digital memory (which is part of the PWM block) and a low pass filter oraR2R ladder network. The digital PWM signal is filtered with an analog Low Pass Filter (LPF) in order to remove the high frequency components existing in the PWM signal and to keep only the fundamental frequency. The digital memory containing the sinus samples was created in Quartus and is named "sinus signal" in Fig. 4. A number of 32 samples (one period), with sample values in the range 0… 255, were used to create a sinusoidal signal with 8 bit of resolution (Fig. 2) and a number of 32 samples, with sample values in the range 0…1023, were used to create a sinusoidal signal for 10 bit of resolution. The sinusoidal signal is generated with both positive half cycle.

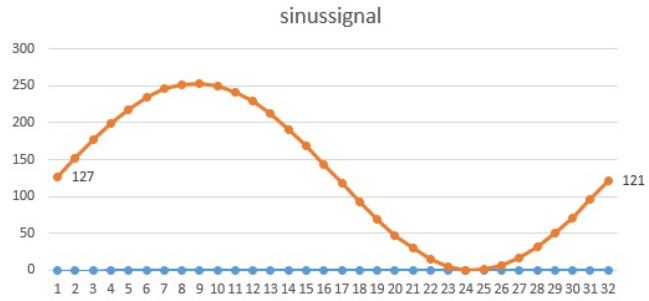


Fig. 2 – Sinusoidal signal.

In Fig. 2, on the horizontal axis are marked the sample number used for the construction of the signal and on the vertical axis are their corresponding code. The PWM generated signal can be seen in Fig. 3 (Quartus simulation). More precisely, the output “out” is available the output of “pwm” block from the Fig. 4.

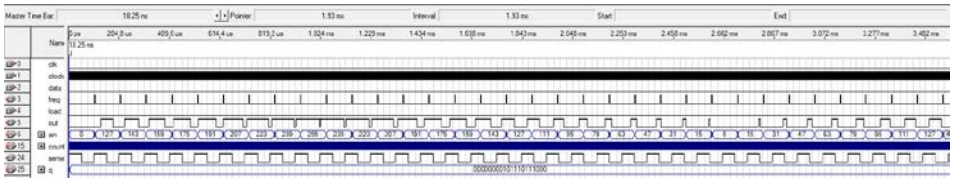


Fig. 3 – PWM generated signal.

In the PWM technique, the sinusoidal sampled values are compared with the "high-frequency" triangular sequence in real time to determine switching states for each pole in the inverter (Kim, 2017). In this paper the PWM signal was digitally generated using a memory to create the sinusoidal signal, a counter to create the triangular signal and a digital comparator, as shown in the Fig. 4.

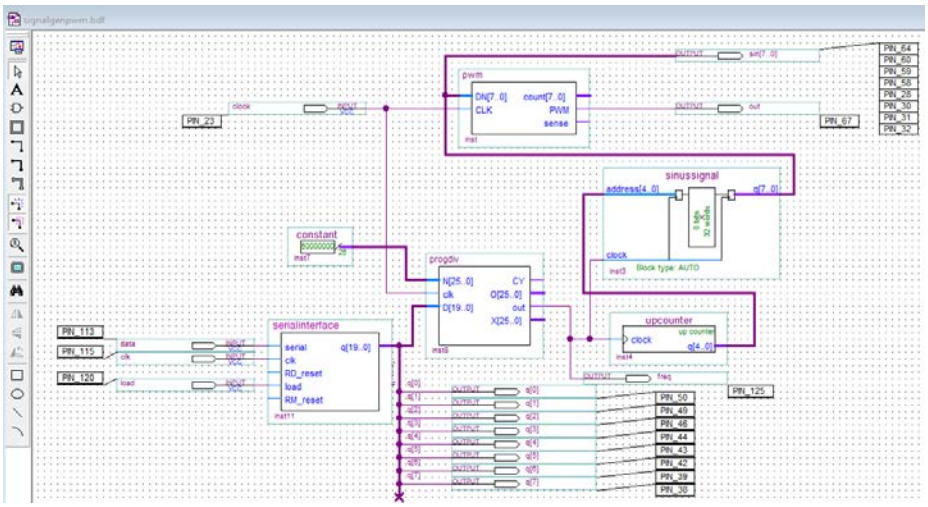


Fig. 4 – The schematicdiagram file in Quartus II.

For this approach, the memory contains the samples of a sinus waveform, but it can be replaced with other waveforms samples for further studies or applications. The number of samples per period has been chosen 32 in order to have a good waveform shape and a higher possible frequency. A larger number of samples will diminished the maximum achievable frequency, while a smaller number will affect the shape of the signal. The PWM period is kept constant, 512 times smaller than the master clock. For a clock frequency of 50 MHz the PWM period is about 10.3 μs, meaning its frequency is 97 kHz. The sinus maximum frequency is around 30 kHz.

The PWM signal is created by comparing the digital word representing the signal sample with a triangular digital sequence generated by a digital up-

down counter. A digital comparator decides the state of the PWM signal according to the relative state between the two values. If the digital words, changing periodically with the sampling frequency, are consecutive samples of the signal, the comparator will modulate the "pwm" output (see Fig. 4) according to it (Zet *et al.*, 2020).

The schematic diagram has five blocks named: "serialinterface", "progdiv", "upcounter", "sinussignal" and "pwm". The "test" block performs the serial loading of 20 bits which represents the value of the frequency programmed automatically by the virtual instrument. Each bit is loaded on the positive edge of the clkinput and the load input confirms the frequency value.The "progdiv" block divides the frequency of the quartz oscillator available on the FPGA development board. The oscillator frequency value is entered as a 20 bit constant. The divided signal represents the clock for the "upcounter" block which generates the address for the memory containing the sinusoidal signal ("sinussignal" block).The "pwm" block performs the process of comparing the sinusoidal sequence of samples with the triangular one generated by an up-down counter.

After assigning the pins, the FPGA is programmed using the USB blaster and the virtual instrument can analyze the generated analog signals.

The R2R resistor ladder based DAC is a simple, accurate and inexpensive way to create analog voltages from digital systems. This module directly converts a parallel digital word into an analog voltage. Each digital input (d_0... d_7 or d_0 … d_9) adds its own weighted contribution to the analog output ($V_{out\text{-}8bit}$ or $V_{out\text{-}10bit}$) as the Fig. 5 shows.

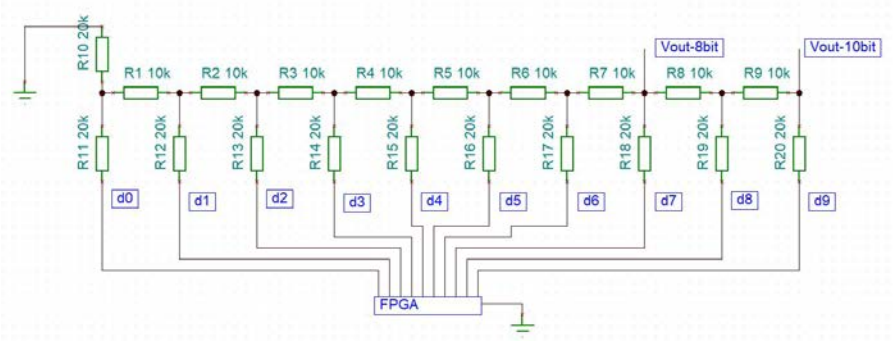


Fig. 5 – R2R module.

Using the Thevenin equivalents technique we can use the Eq. (3) to calculate the contribution of each bit to the output.

$$V_{\text{out-nbit}} = \frac{V_{d_0}}{2^n} + \frac{V_{d_1}}{2^{n-1}} + \frac{V_{d_2}}{2^{n-2}} + \cdots + \frac{V_{d_{n-1}}}{2^1} \text{ [V]} \quad (3)$$

were *n* represent the number of bits of resolution. For this analysis *n* can have the value 8 or 10. The digital inputs are connected to the FPGA using "sin[7..0]"

outputs of "sinussignal" block (see Fig. 4) and the analog output is connected to the data acquisition board. The R2R module no longer requires the "pwm" block in Quartus program but the number of resistors increases.

The PWM generated signal will result much smoother than the R2R generated one, due to the filter, but it suffers of amplitude and distortion variation with the signal frequency.

Several FPGA based boards from different families were considered for this analysis. Three of them belong to the Cyclone IV family (EP4CE6E22C8N), other three belong to Cyclone V family (5CEBA4F23C7N) and other three belong to Cyclone II family (EP2C5T144C8N). In the Table 1 are presented some specifications of these FPGAs.

Table 1

FPGA based boards

Board name	Chip of ALTERA	Master clock	Voltage output
EP2C5 MiniBoard	*EP2C5T144C8N*	*50 MHz*	*3.3 V*
PS-06	*EP4CE6E22C8N*	*50 MHz*	*3.3 V*
DE0-CV	*5CEBA4F23C7N*	*50 MHz*	*5V*

2.3. The virtual instrument used for testing the analog signals

Distortion analysis for programmable analog signals uses a virtual instrument (VI) in order to test the generator and to program the generated signal frequency. The block diagram of the instrument is found in Fig. 6.

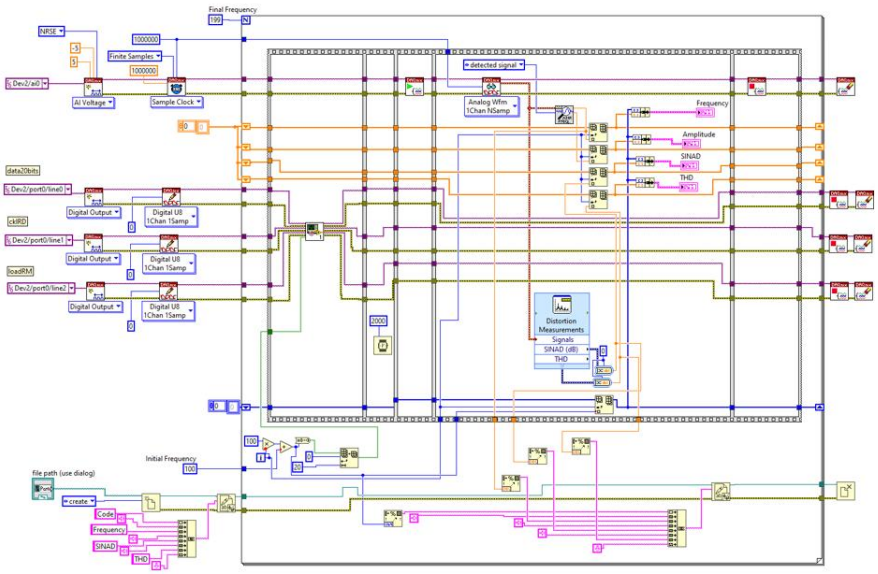


Fig. 6 – Block diagram.

According to the block diagram, the VI uses an analog input and 3 digital IOs of the DAQ card. The frequency is programmed serially, using a sub VI named Test1.vi and a signal processing function is used to calculate the THD parameter. The generated analog signal is processed using distortion measurement VI. The VI is creating, at the end of the acquisition process, a text file with information of interest for the current analysis, such as the value of the programmed frequency, the code used for programmed frequency and the THD parameter.

3. Experimental results

Once the device is programmed, the virtual instrument is started and automatically programs the FPGA to generate the sinusoidal signals with a desired starting frequency, with a desired step, until it reaches the maximum frequency. For example, the tests were performed from 100 Hz to 30 kHz with 100 Hz steps. Both outputs (the PWM and the R2R one) are active, except that the PWM output can support at full resolution only 10 kHz. The tests were performed with signals generated with resolutions of 8 bits and 10 bits for both converters.

The graphs below show the evolution of the THD parameter for the FPGAs presented in Table1. The three devices in the same family were marked as D1 THD [%], D2 THD [%], D3 THD [%]. The diagrams in the Fig. 7 show the evolution of the THD parameter in case of using the PWM module with 8-bit resolution for all families presented in the table1. On the X axis of the diagrams are the values of the generated signal frequency [Hz] and on the Y axis are the percentage THD values [%].

THD values slightly decrease as the frequency increases. The THD value starts for all three families around 0.25% reaching the value of 0.09% when the generated frequency is 10 kHz.

The diagrams in Fig. 8 show the evolution of the THD parameter in case of using the PWM module with 10-bit resolution. Increasing the resolution involves some updates of Quartus program and also a new PWM module. In this case the THD value starts around 0.08% reaching the minim value of 0.0125% when the generated frequency is 8.9 kHz after which the value starts to increase again until 0.019% when the generated frequency is 10kHz.

The diagrams in Fig. 9 show the evolution of the THD parameter in case of using the R2R module with 8-bit resolution for same families. The change of the module will not change of the THD evolution. So, using R2R module, THD values decrease as the frequency increases. Reaching frequencies of 30 kHz, a THD value of 0.35% can be obtained experimentally.

The diagrams in fig. 10 show the evolution of the THD parameter in case of using the R2R module with 10-bit resolution for all three families.

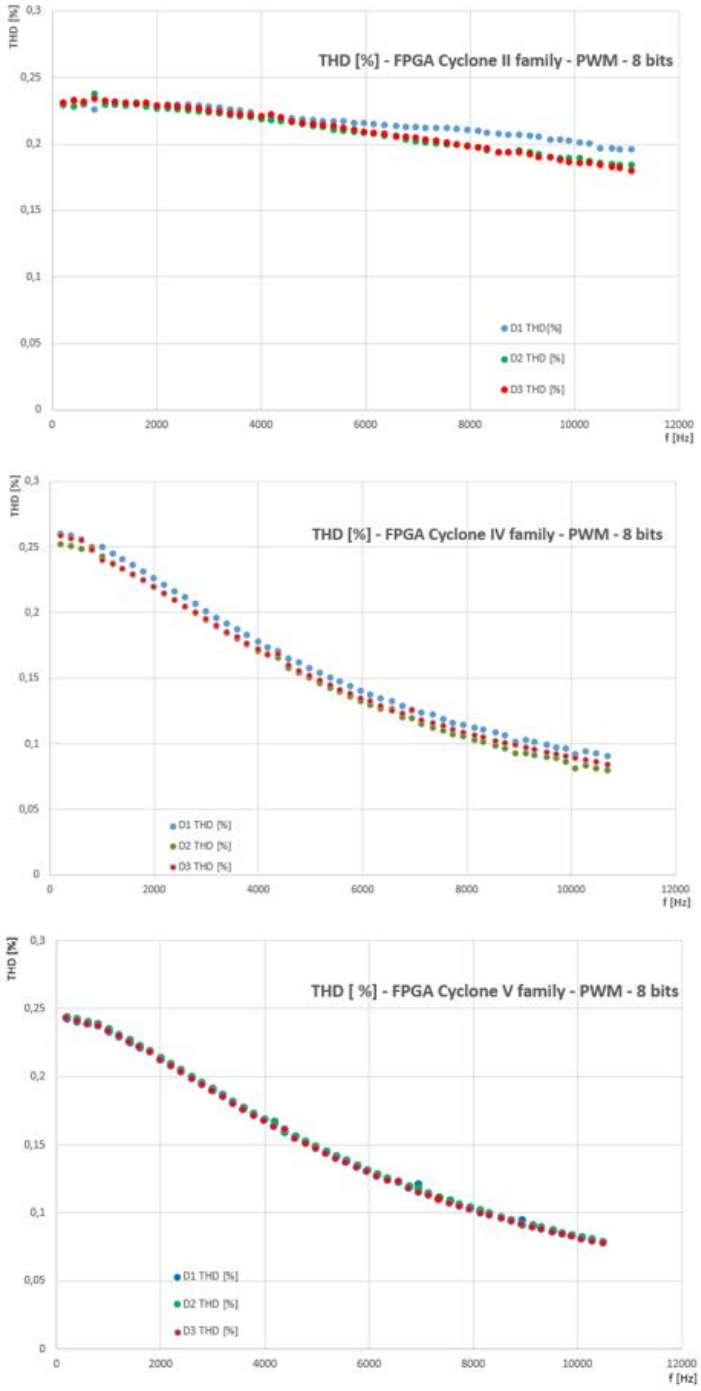


Fig. 7 – PWM module – 8-bit resolution.

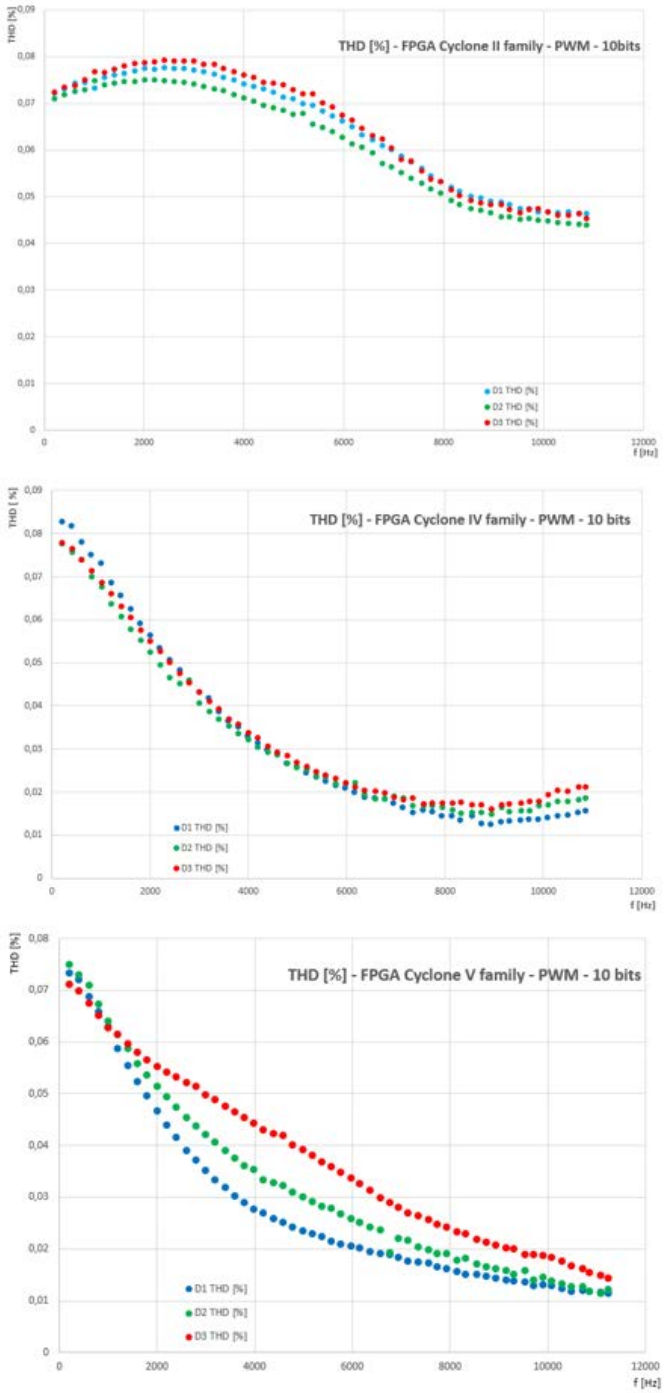


Fig. 8 – PWM module – 10-bit resolution.

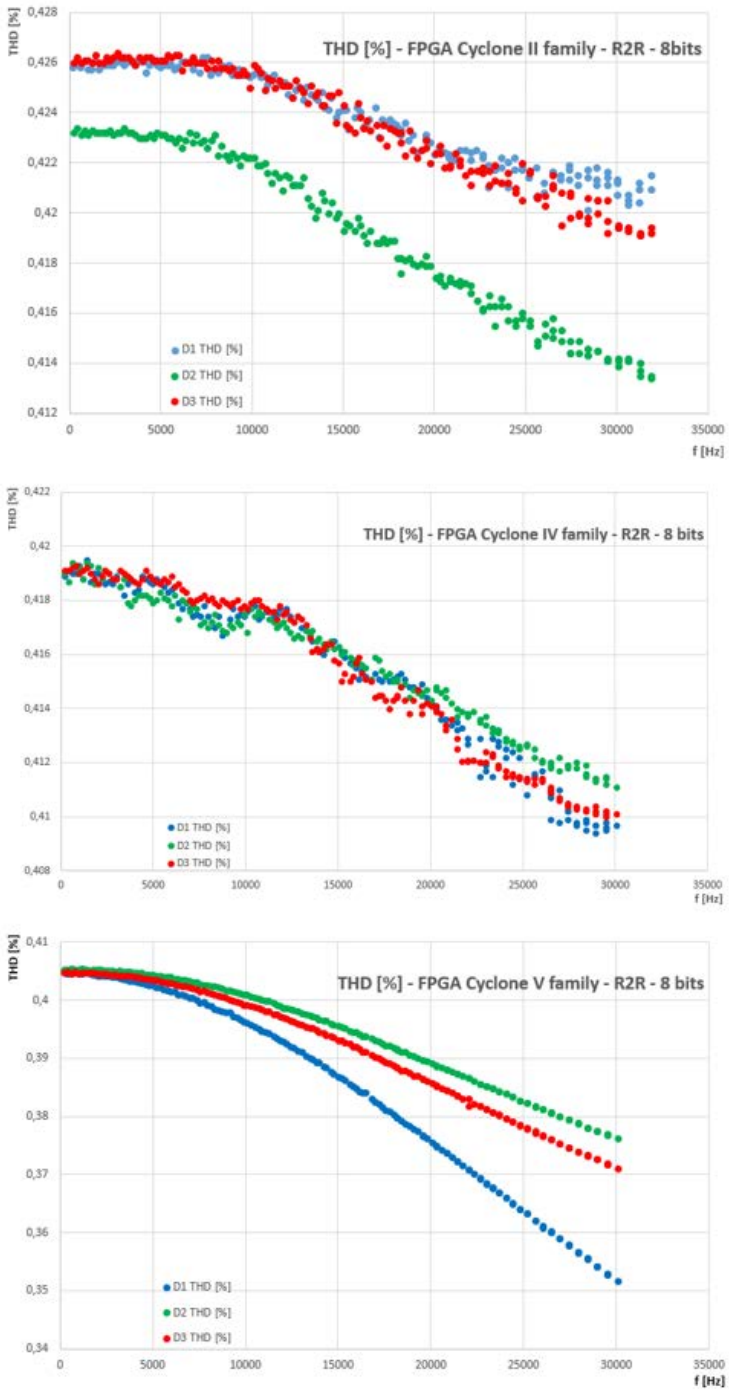


Fig. 9 – R2R module – 8-bit resolution.

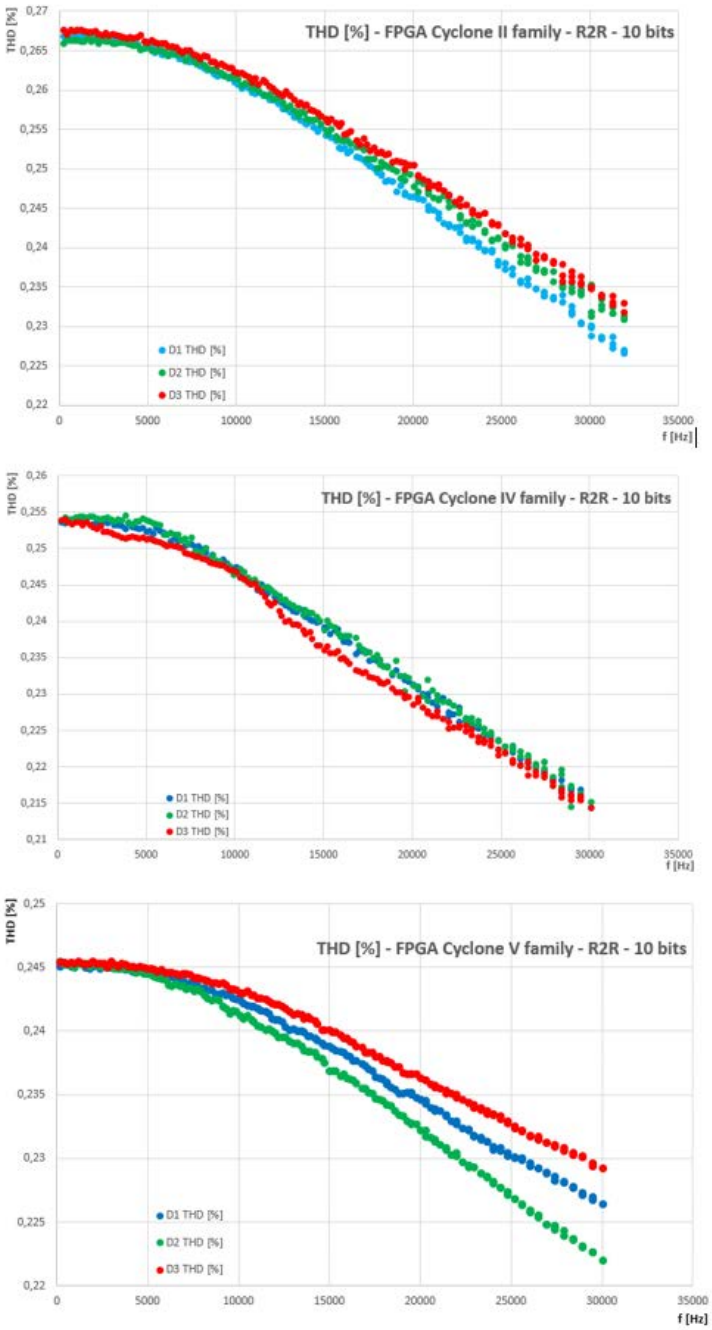


Fig. 10 – R2R module – 10-bit resolution.

Another more detailed analysis was done for the Cyclone V family FPGAs because they have good stability in the measurement process. At a lower frequency, up to 10 kHz, the PWM module obtains better THD values, reaching even 0.013% for 10-bit resolution. When the frequency increases the low pass filter can no longer perform the filtering process and the results are no longer conclusive. The comparison between the 8 and 10-bit measurement process is illustrated in Fig. 11.

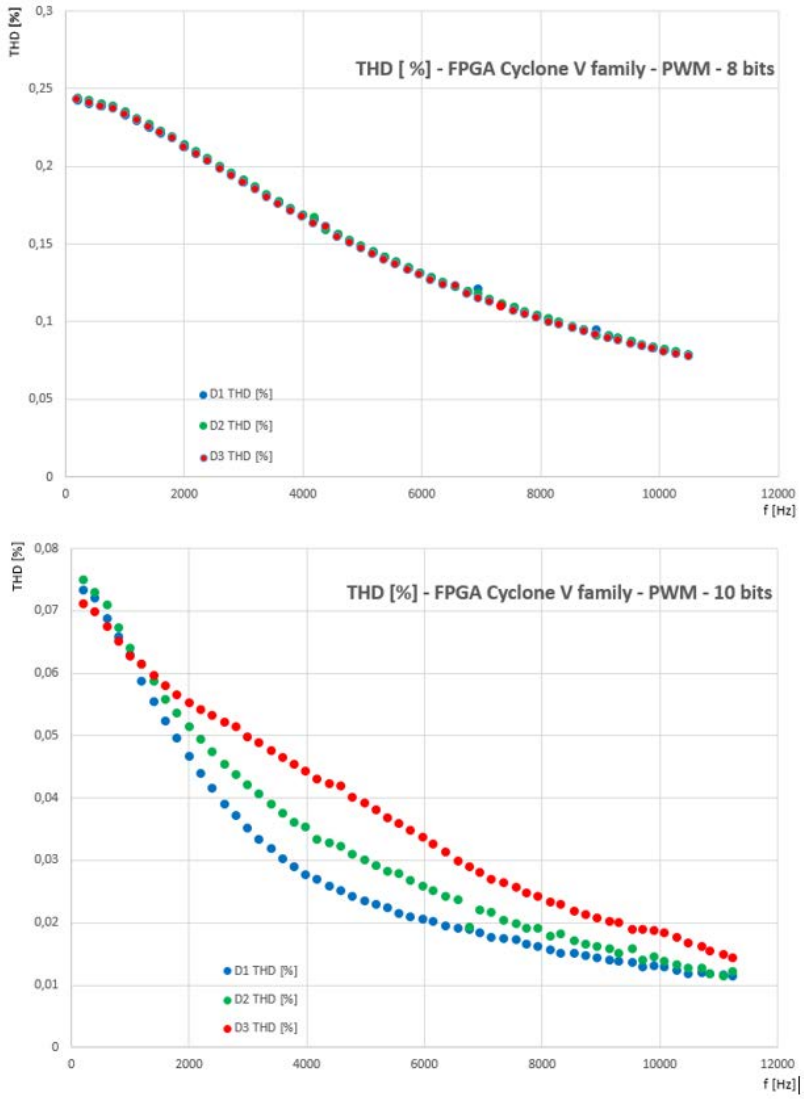


Fig. 11 – PWM module comparison 8 and 10-bit resolution.

At frequencies higher than 10 kHz, the R2R module obtains better THD values, reaching even 0.222%, measured at 30 kHz. The comparison between the 8 and 10-bit measurement process is illustrated in Fig. 12.

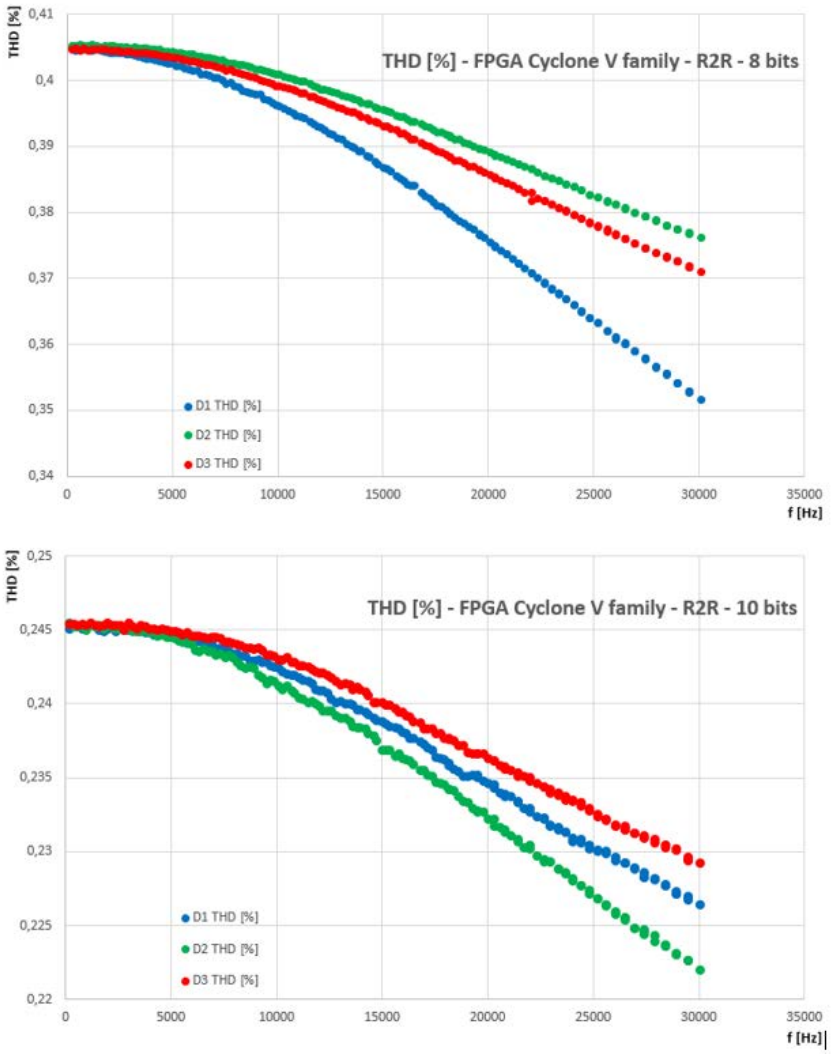


Fig. 12 – R2R module comparison 8 and 10-bit resolution.

4. Conclusions

For the clear dissemination of the measurement results, a second table was built. Table 2 presents the THD values for two different frequencies of generated signal, such as 1 kHz and 10 kHz.

Table 2
Measurement results

FPGA family	Frequency [Hz]	Module	Resolution [bit]	THD [%]
Cyclone II	*1000*	*PWM*	*8*	*0.230*
	10000	*PWM*	*8*	*0.186*
Cyclone IV	*1000*	*PWM*	*8*	*0.240*
	10000	*PWM*	*8*	*0.081*
Cyclone V	*1000*	*PWM*	*8*	*0.233*
	10000	*PWM*	*8*	*0.081*
Cyclone II	*1000*	*PWM*	*10*	*0.073*
	10000	*PWM*	*10*	*0.045*
Cyclone IV	*1000*	*PWM*	*10*	*0.067*
	10000	*PWM*	*10*	*0.014*
Cyclone V	*1000*	*PWM*	*10*	*0.062*
	10000	*PWM*	*10*	*0.013*
Cyclone II	*1000*	*R2R*	*8*	*0.423*
	10000	*R2R*	*8*	*0.422*
Cyclone IV	*1000*	*R2R*	*8*	*0.419*
	10000	*R2R*	*8*	*0.416*
Cyclone V	*1000*	*R2R*	*8*	*0.404*
	10000	*R2R*	*8*	*0.396*
Cyclone II	*1000*	*R2R*	*10*	*0.266*
	10000	*R2R*	*10*	*0.260*
Cyclone IV	*1000*	*R2R*	*10*	*0.253*
	10000	*R2R*	*10*	*0.246*
Cyclone V	*1000*	*R2R*	*10*	*0.245*
	10000	*R2R*	*10*	*0.241*

At the frequency of 10 kHz, the minimum value of THD (0.013%) is that of the 10-bit PWM module, connected to a Cyclone V FPGA. At the frequency of 30 kHz, the minimum value of THD (0.214%) is that of the 10-bit R2R module, connected to a Cyclone IV FPGA as shown in the Table 3.

Table 3
Minimum values of THD [%]

FPGA family	Frequency [Hz]	Module	Resolution [bit]	THD [%]
Cyclone II	*30000*	*R2R*	*10*	*0.229*
Cyclone IV	*30000*	*R2R*	*10*	*0.214*
Cyclone V	*30000*	*R2R*	*10*	*0.222*

Table 4
Standard deviation of THD

FPGA family	THD mean [%]	Module	Resolution [bit]	Standard deviation [%]
Cyclone II	*0.2456*	*R2R*	*10*	*0.0158*
Cyclone IV	*0.2378*	*R2R*	*10*	*0.0124*
Cyclone V	*0.2376*	*R2R*	*10*	*0.0060*

Another approach to the measurement process is to calculate the standard deviation for the THD values. The standard deviation is a parameter that measures the dispersion of a dataset relative to its mean and is calculated as the square root of the variance. The standard deviation values for all three FPGAs family are shown in the Table 4 and the Cyclone V has the minimum standard deviation but all of them show a good reproducibility of the generated signals.

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ANALIZA DISTORSIUNILOR SEMNALELOR ANALOGICE PROGRAMABILE FOLOSIND UN FPGA

(Rezumat)

În ingineria electrică, aplicațiile practice folosesc frecvent semnale analogice dar sunt implicate și circuite numerice și microcontrolere. Uneori este mai ușor și mai ieftin să construiești convertoare AD și DA decât să folosești astfel de convertoare dedicate. Această lucrare este o analiză comparativă a preciziei semnalelor analogice generate cu ajutorul sistemelor digitale precum FPGA-urile, utilizând doar circuite pasive suplimentare. În acest sens s-au folosit două metode de generare a semnalului, două rezoluții diferite și nouă plăci de dezvoltare ce utilizează câte un FPGA din trei familii diferite. Analiza a fost efectuată pentru o bandă de frecvență comună, de la 100 Hz până la 30 kHz, folosind un instrument virtual pentru construirea unui sistem automat de testare. La 10 kHz, modulul PWM generează valori ale parametrului THD mai bune decât modulul R2R, ajungând chiar și la 0,013% iar la 30 kHz modulul R2R generează valori THD mai bune, ajungând chiar și la 0,222%.