J.Natn.Sci.Foundation Sri Lanka 2024 52 (3): 401 - 412
DOI: http://dx.doi.org/10.4038/jnsfsr.v52i3.11867

RESEARCH ARTICLE

Communication Engineering

An efficient and improved algorithm for generating an equivalent planar architecture of the data vortex switch

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Submitted: 28 September 2023; Revised: 28 August 2024; Accepted: 02 September 2024

Abstract: The data vortex (DV) switch was originally designed as an all optical interconnection network for high performance computing (HPC) applications. It was highly scalable with low latency and high throughput, compared to traditional switches used for optical packet switching (OPS) and HPC applications. The equivalent planar (chained MIN) model of the DV, proposed in previous literature, is a planar diagrammatic conversion of a 3-D model of the DV network. In this paper, we will focus on exploring a new, efficient and improved generalized algorithm that enables the arrangement of routing pathways to be implemented as an equivalent planar architecture (EPA, chained MIN) of a DV to find all possible routes between each source and target node pair. The original 3-D architecture of any size can be converted to a planar structure more simply by using the new generalized equivalent planar architecture (EPA) algorithm. To verify the proposed EPA algorithm, it was tested with different input traffic loads and network sizes while keeping the active angle 'A' constant. Network performance parameters, including injection rate (throughput) and latency (mean hops), obtained from simulation results are also provided to confirm the validity of the proposed EPA algorithm. This new algorithm is versatile, simpler and can be applied to networks of various sizes.

Keywords: Data vortex, equivalent planar architecture algorithm, high performance computing, optical buffering, optical interconnections, optical packet switching.

INTRODUCTION

High-performance computing systems (HPCSs) show that future higher generation supercomputers will require a large number of processors. The trend of increasing processor numbers to achieve better system performance highlights the importance of the high bandwidth (BW) interconnection system. A moderate system that causes multi-cycle delays on each inter-processor or processor to memory message can become a significant barrier in a parallel framework. To help mitigate this potential issue, lower latency optical fiber systems can replace electrical wire net-works. Delay is additionally reduced by implementing dense wavelength division multiplexing (DWDM) (Glabowski *et al*., 2020), which makes messages broad in the frequency domain (FD) and narrow in the time domain (TD). However, a significant obstacle to utilizing multistage optical DWDM systems is the lack of random access optical memory. This requires converting messages from an optical to electrical (O/E) structure within the system for storage purposes, and then converting them back from electrical to optical (E/O) structure later. This limits the switching speed while also increasing power consumption (Chen, 2019; Jokar *et al*., 2020). To avoid this costly transformation at each

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node of network conflict, buffering can be completely eliminated by using a deflection routing strategy. This creates a clear pathway for all-optical end to end communication throughout the system maintaining data flow and effectively bypassing any data drops or stops within the network. This eliminates message congestion within the network except for that experienced at the ingress nodes when a message is injected (Hawkins & Wills, 2006). Optical pathway interconnection systems utilizing dense wavelength division multiplexing can significantly improve supercomputer performance. A detailed study indicates that the lack of efficient optical buffering in optical packet switching (OPS) networks requires the exploration of new topologies and routing systems (Hawkins *et al*., 2007).

As the number of nodes in the network increases, the need for internode communication grows exponentially. Hence, it is essential to design an efficient interconnection network (Halla *et al*., 2021). Storing a large amount of data in data centres (DCs) and exchanging global data traffic require a large number of servers for large data centre networks (DCNs) to manage inter-server traffic. This has imposed the need for an ultra-high capacity interconnection network with fast switching speeds, at each switching node (Glick, 2017; Proietti *et al*., 2018; Andreades *et al*., 2019; Lallas, 2019).

The data vortex network is built on a multistage Banyan network architecture with a concentric cylinder structure and a distributed deflection routing control scheme to optimize packet switching and resolve contention. This innovative approach enhances the efficiency, scalability, and performance of the network (Duro *et al*., 2021).

Likewise, as internet traffic continues to grow exponentially, data centres must scale their networks to handle higher volumes of data efficiently. This necessitates high-performance networks capable of rapid data transmission and processing (Sangeetha *et al*., 2023). To meet the increasing demands for high-speed and long-distance communications, data centres are turning to fiber interconnections and optical switching technologies. Fiber optics provide the necessary bandwidth and scalability, while optical switches enable faster, more efficient data routing with reduced latency (Zhao *et al*., 2023).

The increasing volume of traffic necessitates lower latency interconnection networks for future next-generation DCNs. This also calls for the investigation of new modified topologies to increase the transmission capacities by increasing the bisection bandwidth of DCNs. It is also crucial that large traffic loads flow seamlessly from the optical layer (Soto, 2018; Minakhmetor, 2019; Minakhmetor *et al*., 2020). The rapid expansion of cloud services has led to a significant increase in the number of servers within data centres. High server density generates substantial intra-data centre traffic, requiring network topologies that can efficiently manage and route this traffic while minimizing latency and bottlenecks (Castillo, 2022).

Fortunately, the data vortex switch was originally designed as an all optical interconnection network for HPC applications (Reed, 1999). It was highly scalable, with low latency and narrow latency distribution compared to traditional switches used for OPS HPC applications. Later, the Data Vortex switch was investigated in references (Yang *et al*.,2001; Yang & Bergman, 2002a; Yang & Bergman, 2002b; Lu *et al*., 2003; Papadimitriou *et al*., 2003; Shacham *et al*., 2005; Shacham & Bergman, 2007). For the first time, the equivalent chained planar (MIN) model, which is a planar diagrammatic conversion of a 3-D model DV network was presented (Sharma *et al*., 2004; Sharma *et al*., 2006; Sharma *et al*., 2007a). This planar representation of DV from 3-D was very useful for studying fault tolerance, terminal reliability, network reliability of DV, and comparison with other MIN models, which were not considered previously (Sharma *et al*., 2007a).

The augmented data vortex (ADV) network was proposed to enhance fault tolerance, terminal reliability, injection rate, latency and latency distribution of DV networks (Sharma *et al*., 2007a; Sharma *et al*., 2007b). Furthermore, the hardware planar layout of the Data Vortex was developed by Q. Yang as described in reference (Yang, 2012). A reverse DV architecture was proposed by Sangeetha *et al*., (2013) and a bidirectional DV architecture (Sangeetha *et al*., 2014). To ensure good quality of service (QoS) in OPS interconnection networks, a modular data vortex with hybrid switching was proposed in DV networks (Yang., 2014). The Data Vortex switch design is not only suitable for traditional HPCS, but also effective for asymmetrical access patterns and complex data analytics (Gioiosa *et al*., 2016). It is also suitable for sporadic applications (Gioiosa *et al*., 2017). After a detailed analysis it was observed that the DV not only has an inherent ability to overcome the limitations of earlier photonic technologies, but is also a versatile switch suitable for multiple applications using all optical packet switching.

For the simulations or analytics discussed in the literature above, the first step is to generate the interconnections of the 3-D DV switch. Additionally, Sharma (2007a), demonstrates that the equivalent planar prototype (EPA) architecture of 3-D DV is beneficial for fault tolerance and reliability analysis when compared to other MINs, QoS implementations etc.

In the above context, this paper aims to present an improved, generalized and efficient algorithm for generating the equivalent planar architecture (EPA) of the 3-D data vortex architecture. This will be achieved by utilizing the unique features of the C++ language to establish all potential interconnections between each source-target node pair. Earlier, an algorithm (Sharma *et al.*, 2004) was proposed to identify all possible routes in the data vortex switch, which also generated the EPA of a DV switch for the first time, albeit with limited versatility. This architecture has potential applications in various areas, such as survivability, congestion control and quality of service (QoS) applications. By utilizing the EPA, the creation of backup paths can be strategically planned, for use in the event of a network failure. The proposed algorithm can also assess fault tolerance by evaluating different links and node failures. Additionally, the performance of the planar architecture such as injection rate and latency is evaluated through numerical simulation written in C++.

The proposed EPA algorithm offers a significantly more adaptable configuration for various network levels, and research confirms that it provides routing performance comparable to the original structure. Due to the adaptability of the new planar design, future studies may investigate further improvements in routing resources and execution. The generalized algorithm facilitates smooth and fault free interconnections with high scalability.

MATERIALS AND METHODS

Original data vortex architecture

The original DV switch architecture was designed by Yang *et al*. (2001), supporting all optical OPS applications by using fewer switching and logic functions and avoiding the need for internal buffering in the network. In this 3-D design, the authors utilized two techniques to eliminate packet conflict and minimize the number of logic decisions required. These techniques, 'synchronous packet clocking' and 'distributed control signalling' are useful to route data payload traffic easily in the optical network. A detailed explanation of the original architecture can be found in (Yang *et al*., 2001; Yang & Bergman, 2002a; Yang & Bergman, 2002b; Lu *et al*., 2003; Papadimitriou *et al*., 2003; Shacham *et al*., 2005; Shacham & Bergman, 2007).

In the design of the original DV, it was assumed that all packets were of similar size and had better timing alignment at the entry point from the input terminal. To manage synchronous slotted function, the routing pathways were properly designed. The routing nodes existed on a rich collection of concentric cylinders. The cylindrical design was defined by two dimensions: the height parameter 'H' corresponded to the number of nodes lying across the cylinder height and, the angle parameter 'A' should be an odd number less than 10. A lot of work has been done by researchers at Columbia University and Georgia Tech. and their simulation results show that the DV switch architecture achieves better performance when the angle parameter is a small odd number less than 10 (Dong *et al*., 2008).The angle corresponds to the count of nodes across the circumference. 'H×A' represents the total count of nodes in each cylinder. The total count of cylinders can be calculated by '$C=1+\log_2 H$'. The total count of nodes in the entire architecture of the switch is 'C×H×A' with 'H×A' I/O ports.

Figure 1 shows a 3-D architecture for an A=3, H=4, C=3 DV switch fabric. Each square point represents a routing node. Each node (square point) is addressed by coordinates (a,c,h), where '$0 \leq a < A$', '$0 \leq h < H$' and '$0 \leq c < C$'. All the packets ingress at the c=0 cylinder level (outermost level) and exit at the $c=\log_2 H$ level (innermost level). Each packet adopts a self-routing scheme. At each cylinder level, the d_i bit of the payload header (binary) is compared with the d_i bit of node height. Here, 'i' is the current cylinder level. Suppose if a packet ingresses from c=0 (outermost) cylinder level then i is 0 (zero). At each level, packets are progressed in a synchronized way and in a parallel manner.

The mapping arrangement can be understood from the given example of an H=4 switch design (shown in Figure 1). The dashed-line pathways between adjacent cylinders maintain a consistent height as they are solely used to forward the packets. Conflict prevention, and therefore the required reduction in processing at the nodes, is achieved through independent control bits. Control messages are exchanged between nodes before a packet arrives at a given node to establish the correct routing option within the network.

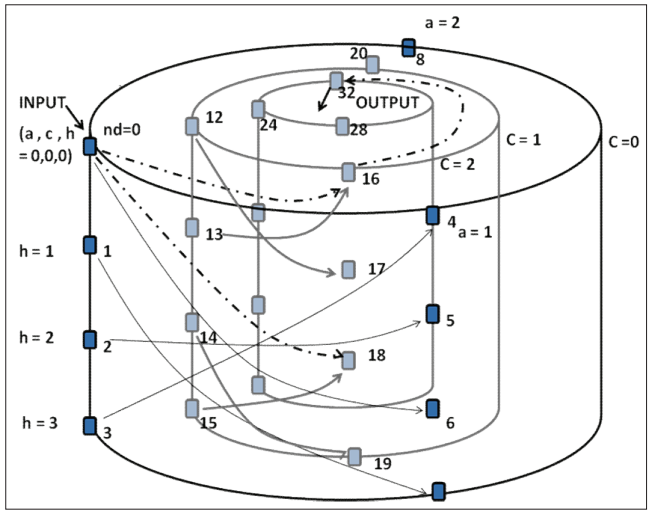

Figure 1: Interconnection arrangement of the original DV switch with adjacent cylinders for A=3, C=3, H=4 (Yang *et al*., 2001)

Equivalent planar architecture (EPA) of DV

In the EPA architecture of DV, each three-dimensional cylinder level corresponds to the respective layer as shown in Figure 2 (Sharma *et al*., 2007a). Thus, layer-0 represents the c=0 cylinder level (outermost cylinder) and layer M represents the cylinder level c=$\log_2$H (innermost cylinder). In each layer of the EPA, we have 2^c subsections or rings. The total count of layers (L) should be equal to $\log_2$H+1 (equal to the total count of cylinders). In the EPA structure the I/O node count is also A×H. The total node count in a switch is A×C×H. The interconnection arrangement for each layer is the same, as given in Figure 1, for a distinct level of cylinders. The data packet enters from the input node of the outermost layer, i.e., layer 0, and exits from the output node from the innermost layer i.e., from layer $\log_2$H. The interconnection links between the layers cross in a binary tree fashion. In this type of arrangement, the next most significant bit (MSB) of the header address is fixed before the packet advances to the next adjacent layer. Interconnection links between layers forward packets to the correct destination.

Suppose we have an EPA design with A=3, H=4, and L=3 where a node is represented by (a,c,h). Every node has 2 input and 2 output connections. In the case of inputs, one input connects from the outer adjacent layer and another input connects from the current layer. In the case of outputs, one output goes to the adjacent inner layer and another output to the current layer.

The interconnection arrangement and self- routing scheme to forward the packets are the same as in the original DV. In the EPA, every node (a,c,h) and its 2 output connecting nodes are transformed into their equivalent representations in decimal form by the following expressions (Sharma *et al*.,2004):

$$ndNode = H \times a + (A \times H) \times c + h \quad ...(1)$$

To find out the node on the current layer, represented by 'sndNode', which is interconnected to 'ndNode', the interconnection pattern shown in Figure 1 is as follows:

$$sndNode = H \times nxa + (A \times H) \times c + nxh \quad ...(2)$$

To find 'nxa', the expression is

$$nxa = (a+1)\%A \quad ...(3)$$

and 'nxh' can be found by the interconnection arrangement described in previous section.

To find the node on the next adjacent layer, 'índNode' is connected to 'ndNode' and the expression is

$$indNode = H \times nxa + (A \times H) \times (c+1) + h \quad ...(4)$$

Example: Suppose the node to be taken as (a=1, c=0, h=3), with A=3, H=4, L=3.

Then, nxa=2. nxh=0, given values are substituted in equation (1), (2) and (4)

ndNode = 4×1+(3×4)×0+3=7
sndNode =4×2+(3×4)×0+0=8
indNode=4×2+(3×4)×(0+1)+3=23

In a similar way, the remaining decimal values of interconnecting nodes can be found for the rest of the nodes.

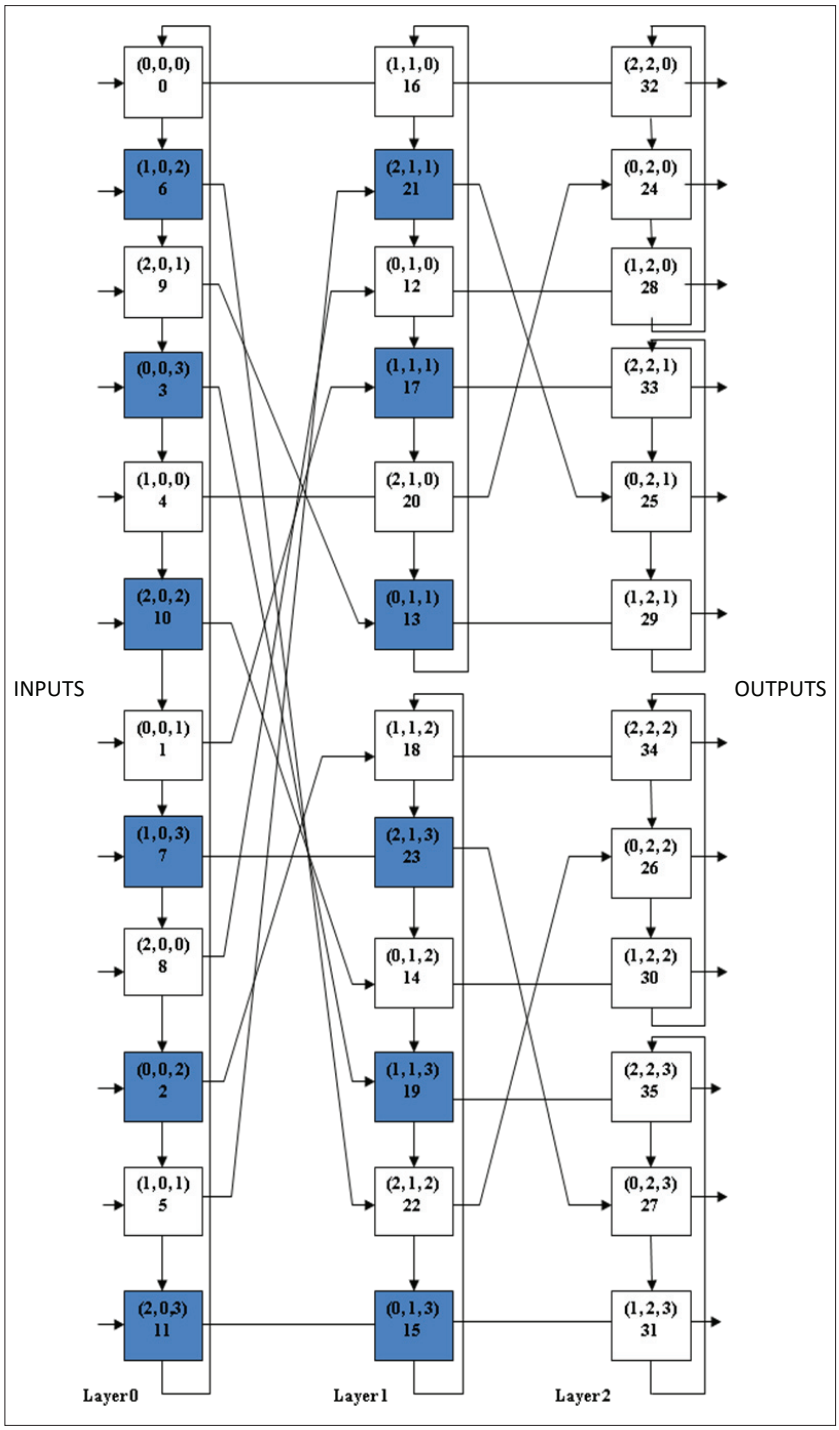

Figure 2: Equivalent planar architecture (EPA) for 3-D original DV architecture of size A=3, L=3, H=4 (Sharma *et al*., 2007a)

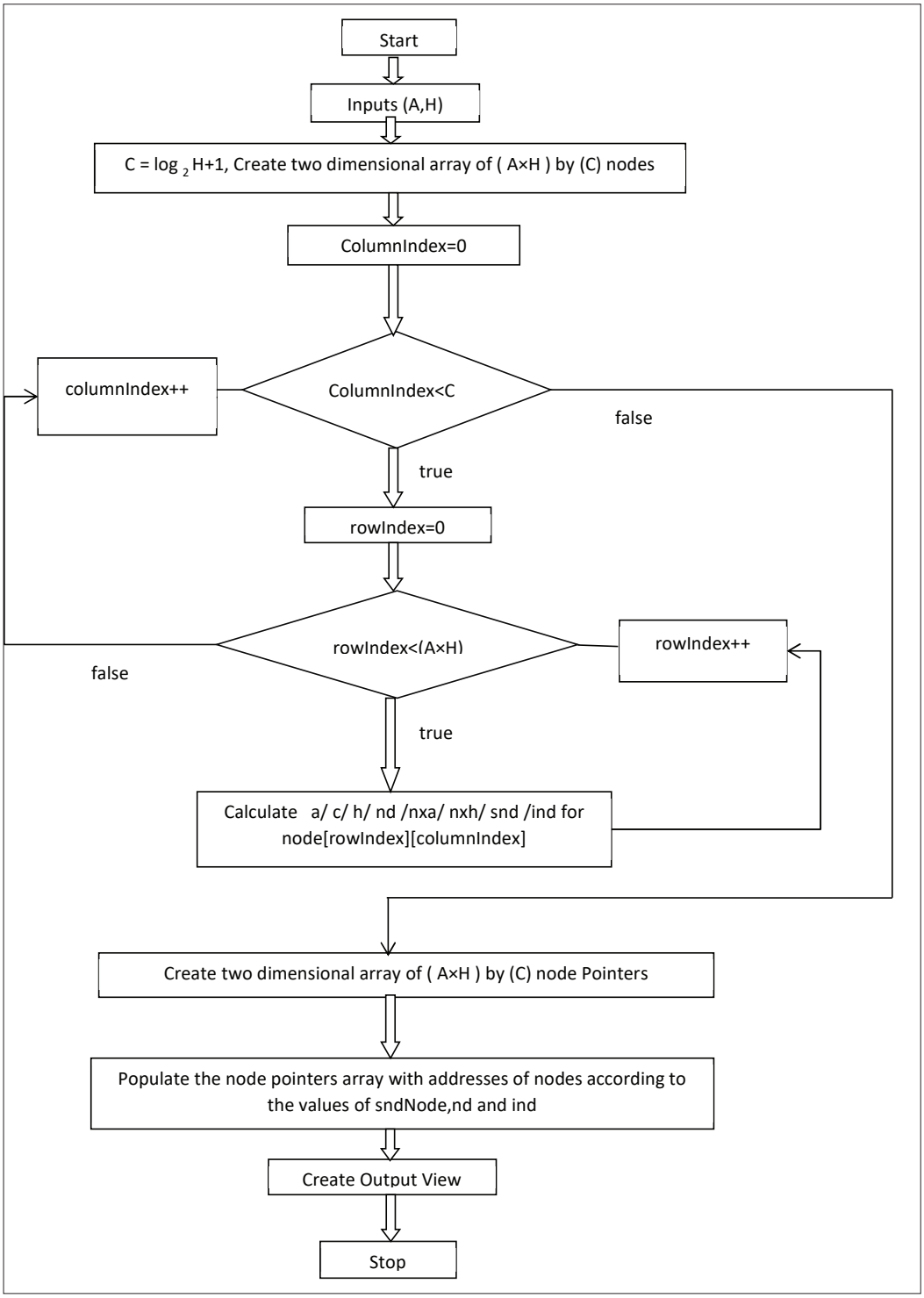

Figure 3: Flow chart of the proposed generalized equivalent planar architecture algorithm of DV (EPAA-DV)

Flow chart and advantages of proposed EPA

The flow chart of the algorithm is described in Figure 3.The steps of the EPAA-DV algorithm are given below:

Step 1: Initialize the angle A, and height H as inputs.
Step 2: Initialize the columnindex, let columnindex=0.
Step 3: If (columnindex<C), go to step 4,
Else, go to step 9,
Step 4: Initialize rowindex, let rowindex=0,
Step 5: If (rowindex<(A×H)), go to step 6,
Else, columnindex++ and go to step 3,
Step 6: Calculate a, c, h, ndNode, nxa, nxh, sndNode, indNode,
for [rowindex] [columnindex],
Step 7: rowindex++ , Go to step 5
Else, columnindex++ and go to step 3,
Step 8: End,
Step 9: Create two dimensional array of (A×H) by C node pointer
Step 10: Populate the node pointer array with address of nodes according to
the values of snd, nd, ind.
Step 11 : Create output view.
Step 12 : End.

1. The main advantage of a generalised EPA algorithm is that it can generate an equivalent planar architecture layout of 3-D, DV for any given size such as A and H.
2. The EPA algorithm simplifies the generation of interconnections of the original DV network in a fault-free and efficient manner, and hence it is easy to compare its topology with other similar types of MINs.
3. Here the 3-dimensional structure is converted into a planar architecture with multiple layers of routing levels making new construction and integration fast and easy with the help of this algorithm.
4. Since a new architecture is designed equivalent to the original DV network, the routing performance such as latency and throughput, is similar to that of the original DV network under similar system working conditions.
5. The proposed EPAA-DV algorithm is an improvement over the earlier algorithm as it is based on C++ language. An artificial simulation environment has been developed using threading, design of classes, file sharing, arrays and all other features of the C++ language. A programme in C++ language has been developed that automatically evaluates the nodes and represents all the nodes in a planar view with respect to each layer.

Proposed equivalent planar architecture algorithm (EPAA) performance analysis

The goal of our study is to explore the key performance parameters of an equivalent planar architecture of DV, generated using the new algorithm, which includes latency of switch and injection rate (IR). This will be done through numerical simulations based on an event simulator written in C++ environment. The statistics will be collected over 1000 clock cycles after the initial transient period. To transmit the data packets from source to target a uniform random traffic model will be used. In random traffic, the time slot of each packet injection is independent of other time slot injections. The amount of input traffic is identified by a parameter named the load parameter defined as the fraction of time a new packet injection is attempted. A load parameter of 0.5 indicates that a new packet injection is attempted at every other time slot. To simplify the investigation, only the height details of output ports are coded as the packet target address. All accessible angles accept the switched data packets at the output ports. The network performance of the equivalent planar architecture of DV will be investigated under different loads and for different switch sizes with the main performance evaluation parameters being latency and IR.

Table 1 shows different network arrangements of the Data Vortex switch for comparison. The following network arrangements labelled L, M, N and O are compared. Each network supports a different number of inputs and outputs. In network 'M' the number of switches used is between that of network 'L' and 'N'. All of the network architectures use the same active angle A=5.

Table 1: Different network arrangements of the DV Switch

Network Name	'A'	'H'	Total Nodes
L	5	4	60
M	5	8	160
N	5	16	400
O	5	32	3160

Latency

The latency of a switching architecture is defined as the mean number of hops travelled by packets to reach the target.

Figure 4a shows the latency presented as a function of the switch size with A=5 for various loads. From the figure and Table 2, it is observed that the latency of the switch is low for small switch sizes and light loads, which is likely due to low traffic density. The planar DV showed almost a similar performance as reported by Reed (1999).

Due to the low traffic volume in a small switch, the likelihood of deflection is also reduced. In Figure 4a and Table 2, at full load 1.0, the switch requires 5 hops to reach its target for H=4, however, for H=32, it needs 15 hops. The reason is evident since with a small switch size there is less traffic congestion, and the probability of deflection is low. As the switch size increases the latency also increases but the behaviour of the planar switch remains consistent with the findings of Yang *et al*., (2001).

Injection rate

The injection rate (IR) is defined as the ratio of successfully injected packets into the first layer of the switch over the total number of injection trials.

In Figure 4.1(b), the IR is plotted as a function of input loads for different switch heights with angle A=5. From the figure and Table 3, it can be observed that as the load increases the IR decreases, while for small loads the IR is good.

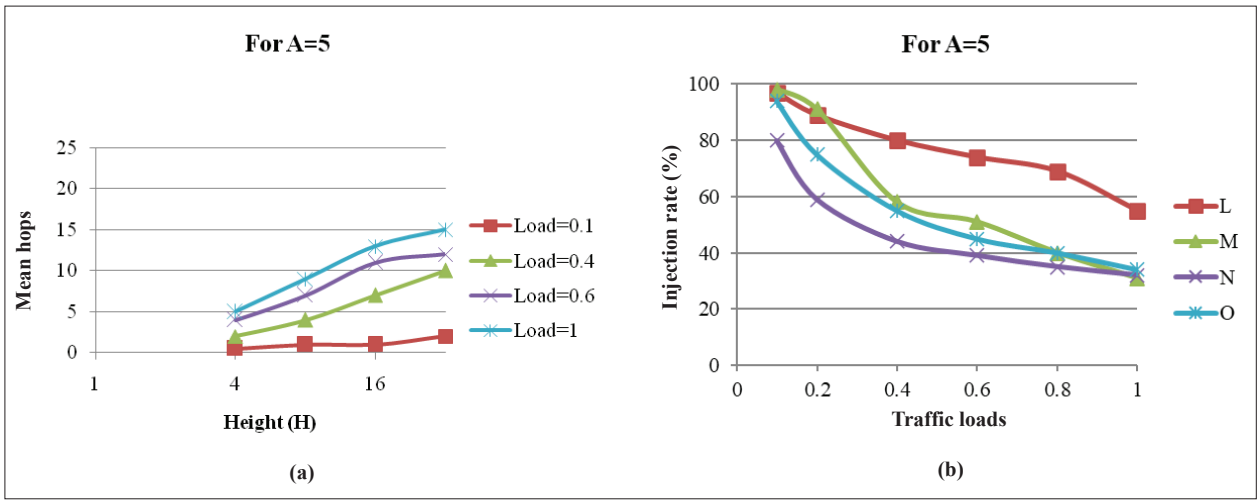

Figure 4: **(a)** Latency performance comparison for varying loads on different network arrangements of the DV
(b) Injection rate performance comparison for varying traffic loads on different network arrangements of DV

Table 2: Latency (mean hops) performance under varying input traffic loads for different arrangements of DV

Network arrangements	Traffic loads			
latency	0.1	0.4	0.6	1
Network L	0.5	2	4	5
Network M	1	4	7	9
Network N	1	7	11	13
Network O	2	10	12	15

Table 3: Injection rate (IR) performances for varying input traffic loads on different network arrangements of DV

Network arrangements	Traffic loads					
injection rate (%)	0.1	0.2	0.4	0.6	0.8	1
Network L	97	89	80	74	69	55
Network M	98	91	58	51	40	31
Network N	80	59	44	39	35	32
Network O	94	75	55	45	40	34

RESULTS AND DISCUSSION

The proposed EPA algorithm (see Figure 3) was utilized to identify all potential interconnections of the DV and validate the routes between any source-target pair. As mentioned earlier, the packet enters from the input node at layer 0 and exits from the output node at layer $\log_2 H$. As the packet moves from outer layers to the inner layer it updates the next most significant bit (MSB) of the header address before advancing to the next adjacent layer. It also maintains a consistent height during this process. However, if the destined inner layer interconnection link is blocked due to a header mismatch or the priority of another node, then the packet deflects within the current layer from ndNode (nd) to sndNode (snd). For example, in Figure 2, the Equivalent Planar Architecture is illustrated for a planar switch size of 'A'=3 and 'H'=4.

To confirm the routing of the DV, let's consider a packet entering from the node address (2,0,1) or nd = 9 (from equation 1). The number of header bits count can be obtained using the formula $\log_2 H$. Here, with H=4 the frame has 2 bits header (binary). This indicates the destination address is 1, which was inserted into the packet upon injection at the input link of the input node at the 0^{th} layer level. To verify the routing process only one packet was injected. In Figure 2, it is shown that the packet entered the inner layer 1 at node address (2,0,1) and by comparing the MSB of the packet's header bit with the corresponding MSB of the node's height it progresses into the next adjacent layer indNode (ind) =13 (from equation 4) or (0,1,1). Again the same step for header decoding is repeated and the packet enters the next adjacent layer, which is layer 1 at node (1,2,1). In this example, layer 2 is the last or innermost layer. It is assumed that if the packet's header address matches the targeted node height of the last layer then the packet will exit successfully from that node if the output link is free. This can be seen in Figure 5, which shows the same routing path as explained above.

Verification of routing of the planar DV by EPA Algorithm for planar switch size A=3 and H=4

1.	nd=0 a=0,c=0,h=0 nxa=1 nxh=2 snd=6 ind=16	nd=16 a=1,c=1,h=0 nxa=2 nxh=1 snd=21 ind=32	nd=32 a=2,c=2,h=0 nxa=0 nxh=0 snd=24 ind=36
2.	nd=6 a=1,c=0,h=2 nxa=2 nxh=1 snd=9 ind=22	nd=21 a=2,c=1,h=1 nxa=0 nxh=0 snd=12 ind=25	nd=24 a=0,c=2,h=0 nxa=1 nxh=0 snd=28 ind=40
3.	nd=9 a=2,c=0,h=1 nxa=0 nxh=3 snd=3 ind=13	nd=12 a=0,c=1,h=0 nxa=1 nxh=1 snd=17 ind=28	nd=28 a=1,c=2,h=0 nxa=2 nxh=0 snd=32 ind=44
4.	nd=3 a=0,c=0,h=3 nxa=1 nxh=0 snd=4 ind=19	nd=17 a=1,c=1,h=1 nxa=2 nxh=0 snd=20 ind=33	nd=33 a=2,c=2,h=1 nxa=0 nxh=1 snd=25 ind=37
5.	nd=4 a=1,c=0,h=0 nxa=2 nxh=2 snd=10 ind=20	nd=20 a=2,c=1,h=0 nxa=0 nxh=1 snd=13 ind=24	nd=25 a=0,c=2,h=1 nxa=1 nxh=1 snd=29 ind=41
6.	nd=10 a=2,c=0,h=2 nxa=0 nxh=1 snd=1 ind=14	nd=13 a=0,c=1,h=1 nxa=1 nxh=0 snd=16 ind=29	nd=29 a=1,c=2,h=1 nxa=2 nxh=1 snd=33 ind=45
7.	nd=1 a=0,c=0,h=1 nxa=1 nxh=3 snd=7 ind=17	nd=18 a=1,c=1,h=2 nxa=2 nxh=3 snd=23 ind=34	nd=34 a=2,c=2,h=2 nxa=0 nxh=2 snd=26 ind=38
8.	nd=7 a=1,c=0,h=3 nxa=2 nxh=0 snd=8 ind=23	nd=23 a=2,c=1,h=3 nxa=0 nxh=2 snd=14 ind=27	nd=26 a=0,c=2,h=2 nxa=1 nxh=2 snd=30 ind=42
9.	nd=8 a=2,c=0,h=0 nxa=0 nxh=2 snd=2 ind=12	nd=14 a=0,c=1,h=2 nxa=1 nxh=3 snd=19 ind=30	nd=30 a=1,c=2,h=2 nxa=2 nxh=2 snd=34 ind=46
10.	nd=2 a=0,c=0,h=2 nxa=1 nxh=1 snd=5 ind=18	nd=19 a=1,c=1,h=3 nxa=2 nxh=2 snd=22 ind=35	nd=35 a=2,c=2,h=3 nxa=0 nxh=3 snd=27 ind=39

11.	nd=5 a=1,c=0,h=1 nxa=2 nxh=3 snd=11 ind=21	nd=22 a=2,c=1,h=2 nxa=0 nxh=3 snd=15 ind=26	nd=27 a=0,c=2,h=3 nxa=1 nxh=3 snd=31 ind=43
12.	nd=11 a=2,c=0,h=3 nxa=0 nxh=0 snd=0 ind=15	nd=15 a=0,c=1,h=3 nxa=1 nxh=2 snd=18 ind=31	nd=31 a=1,c=2,h=3 nxa=2 nxh=3 snd=35 ind=47

Flow is as follows:

Data Fed: 64321 in Node 9 on Layer 1 where c=0

The binary form of 64321 is 1111101101000001
Number of header bits 2

nd=9 a=2,c=0,h=1 nxa=0 nxh=3 snd=3 ind=13
nd=13 a=0,c=1,h=1 nxa=1 nxh=0 snd=16 ind=29
nd=29 a=1,c=2,h=1 nxa=2 nxh=1 snd=33 ind=45

Finally, 64321 reached its destination after 2 hops.

Figure 5: Verification of routing path using the EPA algorithm

CONCLUSION

In this paper an efficient and improved generalized equivalent planar architecture algorithm for data vortex has been developed. The main advantage of this algorithm is that it is able to identify all possible connections between every node-pair in the data vortex network and enable the design of circuits in equivalent planar model for any given size in simpler and more versatile way as compared to the methods used in earlier literature. In addition, simulations were conducted to analyze the performance of the proposed EPA algorithm by including different network sizes with a wide dynamic range of varying input traffic loads to validate the results. Two performance parameters, latency of switching architecture and injection rate, were studied. Their behaviour was found to be similar which validated the routing behaviour to be similar to the original DV but easier to study in terms of fault tolerance. Based on these results, the proposed algorithm can be considered as a strong candidate for large scale systems, parallel computing and HPCS applications. The EPA algorithm is versatile and can easily adapt to the diverse needs of next generation HPCS and large Data Centre Networks application.

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