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Experimental Analysis of GaN-Based Half-Bridge LLC Resonant Converter with Enhanced Efficiency through Resonant Tank Optimization

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Abstract: The increasing demand for compact, efficient, and cost-effective power conversion systems across sectors such as renewable energy, industrial automation, and telecommunications has highlighted the need for high-performance DC-DC converters. This paper presents the design, implementation, and experimental validation of a 500 W half-bridge LLC resonant DC-DC converter for 63-75 V input and a regulated 14.5 V output. A key feature of the design is resonant-tank optimization to maintain inductive-region operation and allow soft switching, with experimental evaluation of the soft-switching margin that identifies where ZVS degrades near high-load operation. The incorporation of GaN FETs allows 100 kHz operation with peak efficiency above 90%, and a controlled GaN-versus-MOSFET comparison on the same platform under identical conditions shows a load-dependent efficiency improvement that increases toward higher output power, ranging from approximately 1% to 10%. Practical high-frequency hardware effects, including gate-drive and auxiliary-winding oscillations, are characterized and mitigated using a simple decoupling-and-gate-tuning approach. In addition, an adaptive protection framework is integrated, including configured input over- and under-voltage thresholds and multi-level over-current protection, to provide safe operation. Experimental validation through efficiency measurements and dynamic-load testing confirms stable behaviour over the tested operating range.

Keywords: GaN FETs, LLC Topology, Resonant Tank, Zero Voltage Switching

1. Introduction

The increasing demand for high-efficiency and compact power conversion systems is driven by the rapid growth of modern applications in areas such as industrial automation, renewable energy systems, high-speed communication infrastructures, and robotic platforms [1-4]. These emerging domains impose stringent requirements on DC-DC converters, including high power density, reduced EMI, improved thermal performance, and the capability to operate at higher switching frequencies while maintaining efficiency and system reliability.

Conventional converter topologies such as buck, synchronous buck, push-pull, and flyback have been widely used for voltage regulation and power conversion, but their performance is often constrained in high-frequency, high-efficiency operation due to increased switching losses, higher device stress, and limited control of electromagnetic emissions [5-7]. In contrast, the LLC resonant converter allows soft switching over a wide load range through a resonant tank, reducing switching losses and thermal stress while improving EMI performance and power density. Although GaN-based LLC converters have been increasingly reported, many studies primarily highlight device-level advantages or high-frequency operation, with comparatively limited experimental focus on resonant-tank tuning to sustain inductive-region operation across practical line and load variations and the resulting stability challenges in GaN prototypes.

Motivated by these gaps, this paper presents the design and experimental validation of a 500 W half-bridge LLC resonant DC-DC

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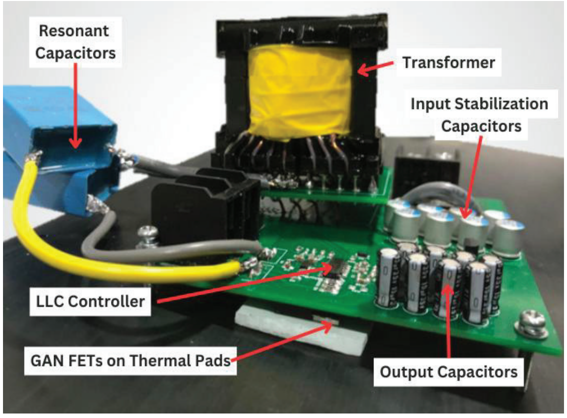

Figure 1 - Complete Hardware Assembly of the LLC Resonant Converter with Integrated Components

converter optimized for high efficiency and compact implementation. As illustrated in Fig. 1, the converter operates from 63-75 V with a nominal input of 72 V and delivers a regulated 14.5 V output at up to 40 A. The power stage utilizes Gallium Nitride (GaN) field-effect transistors (FETs) instead of silicon MOSFETs to reduce switching and conduction loss, controlling lower gate charge and output capacitance to support 100 kHz operation with over 90% efficiency under nominal conditions.

The primary contributions of this work are summarized as follows:

1. Designed and implemented a 500 W GaN FET-based half-bridge LLC resonant converter and experimentally quantified an approximately 1-10% efficiency improvement relative to a comparable MOSFET-based implementation under identical operating conditions.
2. Developed a resonant-tank parameter selection methodology that maintains inductive-region operation over the specified load range to allow consistent ZVS and high efficiency, while integrating adaptive over-voltage, under-voltage, over-current, and over-temperature protection.
3. Validated the system through experiments, including efficiency benchmarking, experimental characterization and suppression of gate-drive oscillations, and a controlled comparison of GaN versus MOSFET switching behaviour under dynamic-load conditions.

The remainder of the paper is as follows: Section 2 provides a literature review, focusing on the comparative analysis of LLC resonant converter topologies and the evaluation of their advantages and limitations. Section 3 details the design of the LLC resonant converter, including design specifications, circuit topology, operating principles, and resonant tank parameter selection. Section 4 discusses the implementation aspects, such as design considerations, high-frequency layout optimization, and advanced protection mechanisms. In Section 5, experimental results are presented, including a performance comparison between GaN FETs and MOSFETs, gate oscillation mitigation strategies, and efficiency enhancement at maximum power. Finally, Section 6 concludes the paper with a summary of the findings.

2. Literature Review on Various Converter Topologies and Their Comparative Analysis

This section provides a comprehensive literature review and comparative analysis of various LLC resonant converter topologies. The discussion highlights the key design characteristics, operational advantages, and limitations of each converter architecture.

2.1 Comparative Analysis of Common DC-DC Converter Families

Hard-switched step-down converters, particularly conventional buck and synchronous buck topologies, are widely adopted due to their simplicity, high maturity, and good efficiency at low-to-medium power levels. However, when higher switching frequencies and large conversion ratios are required, their performance is increasingly limited by switching loss, higher device stress, and increased EMI, which typically requires additional filtering and careful layout to maintain acceptable conducted and radiated emissions [8-12]. GaN devices can reduce switching energy and support faster transitions, improving efficiency in hard-switched implementations, but they do not eliminate the fundamental EMI and loss mechanisms associated with hard commutation, especially under high di/dt conditions [13].

Quasi-resonant and soft-switching variants reduce switching loss by shaping transitions and facilitating ZVS over specific operating conditions, but they often introduce increased control sensitivity to component tolerances and operating point variation, which can affect transient response and robustness under wide load changes [14]. For isolated conversion, flyback topologies are cost-effective and suitable for low power, but discontinuous operation can increase ripple and EMI, and efficiency can degrade as power increases due to higher peak currents and transformer-related losses [5,15-17]. Phase-shifted full-bridge converters are widely used at higher power because primary-side ZVS can be achieved over part of the operating range, but practical implementations may suffer from circulating current and secondary-side oscillations, which can reduce effective ZVS range and increase design complexity for wide input and load operation [18].

2.2 Advantages and Limitations of LLC Resonant Converter Architectures

LLC resonant converters are considerably used for high-efficiency isolated conversion because the resonant tank allows soft switching, which reduces switching loss and EMI and supports high-frequency operation with improved power density [19-21]. Primary-side switches can achieve ZVS over a wide region when the converter is operated on the inductive side of the resonant characteristic, and secondary-side rectifiers can experience reduced switching stress under favourable operating conditions, improving thermal performance and efficiency. These benefits make LLC converters attractive for applications requiring compact hardware and reduced filtering compared to hard-switched alternatives.

Among LLC architectures, the half-bridge LLC provides a cost-effective structure with fewer switches and simpler gate driving, while maintaining isolation and soft-switching capability, which makes it well-suited for low-to-medium power ranges [22-23]. Its main drawbacks are higher primary current stress and increased sensitivity to parasitic elements, particularly at high-load, which can lead to ringing, increased EMI, and reduced soft-switching margin if layout and gate-drive design are not carefully controlled. Full-bridge LLC converters reduce current stress and can improve conduction performance at higher power, but they require four primary switches and additional gate-drive complexity, increasing cost and implementation effort [24,25].

Three-level LLC variants reduce device voltage stress and can be beneficial in higher input-voltage applications, but they introduce additional components and more demanding timing requirements, including coordination of multiple dead times, which increases control complexity [26-29]. Multiphase LLC architectures reduce output ripple and distribute current among phases, facilitating smaller output capacitors and potentially improved transient response. However, they significantly increase system complexity due to phase management and current sharing requirements, especially when maintaining efficiency over a wide load range [30,31]. Bidirectional LLC converters provide power flow reversal for energy storage and electric-vehicle applications but require more complex control and are typically unnecessary for unidirectional regulation scenarios [32-33].

2.3 Research Gap and Design Motivation

Although GaN-based LLC converters have been reported with improved switching performance, many studies primarily emphasize device-level benefits and high-frequency capability, while providing limited experimental discussion on maintaining inductive-region operation with adequate soft-switching margin under practical line and high-load conditions. In addition, implementation-driven effects in GaN hardware, such as load-dependent gate-drive ringing and noise coupling into auxiliary sensing paths, are not consistently reported alongside mitigation strategies. Motivated by these gaps, our work adopts a half-bridge LLC topology suitable for the targeted 500 W power level and focuses on resonant-tank selection intended to maintain inductive operation, followed by experimental evaluation of efficiency trends, soft-switching behaviour near maximum load, and practical mitigation of parasitic-driven oscillations in the implemented prototype.

3. LLC Resonant Converter Design

This section focuses on the detailed design of the LLC resonant converter, including the design objectives and specifications, circuit topology, and operational principles. It addresses the crucial aspects of resonant tank design, providing an analysis of the gain curve and its impact on the selection of parameters.

3.1 Design Objectives and Specifications

The primary objective of this work is to design and experimentally validate a compact, cost-effective 500 W isolated step-down DC-DC converter that achieves greater than 90% conversion efficiency while converting a 72 V

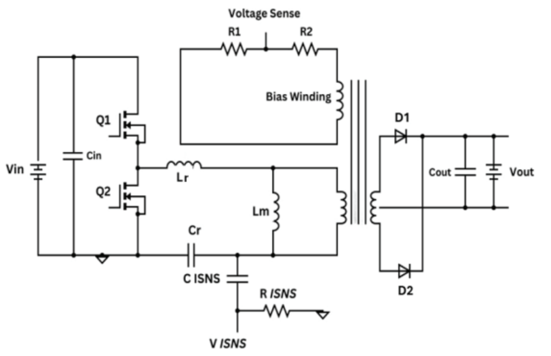

Figure 2 - Overview of the Half-Bridge LLC Converter Topology

DC bus to a regulated low-voltage output suitable for charging a 12 V battery system. The converter is designed to satisfy the full electrical specifications and operating limits summarized in Table 1, including the required input-voltage range, regulated output level, and maximum output current.

A second objective is to improve high-frequency conversion performance by implementing the power stage with GaN FETs and quantifying the efficiency benefit relative to a comparable silicon MOSFET-based implementation. This evaluation is conducted under identical operating conditions and comparable device ratings to confirm that the reported efficiency improvement reflects device technology impact rather than differences in topology or test setup.

A third objective is to demonstrate that the proposed design approach is practically realizable through real hardware validation. Accordingly, the selected half-bridge LLC resonant topology and resonant-tank design are implemented on a prototype and validated via efficiency benchmarking across load conditions and dynamic-load testing, providing that the stated efficiency target and GaN-versus-MOSFET performance claims are supported by experimental measurements rather than simulation-only results.

3.2 Circuit Topology and Operating Principles

The detailed circuit topology of the system is illustrated in Fig.2. The operation of the system initiates with the activation of switch Q1, which marks the beginning of the power conversion. When Q1 turns on, current flows through the resonant inductor (L_r), magnetizing inductance (L_m), and resonant capacitor (C_r). As the current passes through L_m, the magnetizing inductance starts to build up, storing energy in the form of a magnetic field in the primary winding of the transformer. At the same time, C_r and L_r enter a resonant state, establishing an oscillatory energy transfer between the inductance and the capacitor. This resonant condition leads to an increase in the primary current, which is critical for the power transfer process.

During this resonant oscillation, diode D1 becomes forward biased and conducts. The conduction of D1 allows the current to flow from the secondary transformer to the load, effectively delivering power. This phase of operation continues until the resonant cycle reaches its natural conclusion, where the energy stored in L_r and C_r is depleted. At this point, only the magnetizing current remains circulating within the transformer primary. As the primary current decreases toward zero and the L_m reaches its saturation point, switch Q1 is turned off, initiating a brief dead time between the switching transitions. During this dead time, no power is transferred, and the magnetizing current begins to stabilize. During the same time, the parasitic capacitance of switch Q2 is discharged, allowing the circuit to prepare for the next phase of operation. The dead time is necessary to allow the current in the transformer to settle and ensure that switching losses are minimized when Q2 is turned on.

Once the dead time concludes, Q2 is activated. With Q2 now conducting, C_r begins to discharge, releasing the energy stored in it. The discharge of C_r initiates the next resonant cycle, where the polarity of the magnetizing inductance current is reversed. This polarity reversal causes a shift in the primary current direction of the transformer, which also induces a corresponding reversal in the polarity of the secondary winding of the transformer. As the polarity of the secondary winding changes, diode D2 becomes forward biased and begins to conduct, allowing current

Table 1 - Converter Specifications

Parameter	Value
Input Voltage Range	63-75 V
Nominal Input Voltage	72 V
Maximum Input Current	≈8 A
Output Voltage	14.5 V
Maximum Output Current	40 A

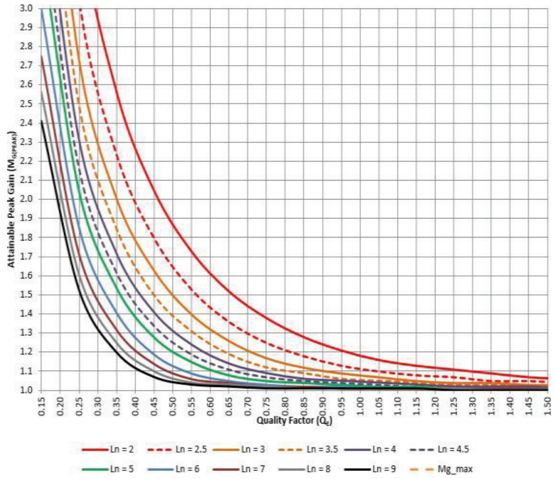

Figure 3 - Variation of Maximum Gain (M_g) and Quality Factor (Q_e) with Respect to Magnetizing to Resonant Inductance Ratio (L_n) [34]

to flow through the load in the opposite direction. This completes the energy transfer for the cycle and sets up the system for the next resonant cycle. This overall operation of the LLC resonant converter thus consists of alternating charging and discharging phases in which energy is efficiently transferred from the high-voltage primary side to the low-voltage secondary side.

3.3 Resonant Tank Design and Parameter selection

This section describes the methodology used to determine the transformer turns ratio and resonant tank parameters of the LLC converter. The procedure starts with gain-curve analysis to select normalized design variables, including the inductance ratio and quality factor, to meet the required gain range. Next, the nominal switching frequency is selected and used to calculate the resonant capacitor and resonant inductor values. Finally, inductive-region operation and ZVS considerations are addressed to provide soft-switching behaviour and reduced switching losses over the intended operating range.

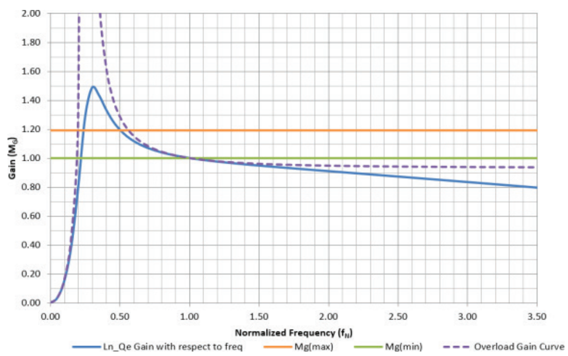

Figure 4 - LLC Gain Curve with the Selected Ln and Qe [34]

3.3.1 Gain curve analysis and parameter determination

The transformer turns ratio plays a crucial role in defining the voltage conversion characteristics of the LLC resonant converter. It is calculated based on the nominal input voltage ($V_{in,nom}$) and the nominal output voltage ($V_{out,nom}$). Since the LLC topology operates in a half-bridge configuration, the effective input to the transformer is half the input voltage. Consequently, the required transformer turns ratio n is calculated using Eq. 1.

$$n = V_{in\_nom}/(2*V_{out\_nom}) = 5/2 = 2.5 \quad \text{... (1)}$$

It is essential to define the minimum and maximum gain values (M_g) of the converter to ensure that the designed converter can regulate output voltage under varying operating conditions. These values are derived by considering additional voltage drops introduced by the rectifier diodes ($V_f \approx 0.5$ V) and other expected losses in the system ($V_{loss} \approx 0.5$ V). The gain at the minimum and maximum operating points is expressed by Eq. 2 and 3, respectively.

$$M_g(min) = n*(V_{out\_min}+V_f)/(V_{in\_max}/2) \approx 2.5*(14.5+0.5)/(75/2) = 1 \quad \text{... (2)}$$

$$M_g(max) = n*(V_{out\_max}+V_f+V_{loss})/(V_{in\_min}/2) \approx 2.5*(14.5+1)/(63/2) = 1.23 \quad \text{... (3)}$$

These gain values are used to guide the design of the resonant tank so that the converter can achieve the necessary voltage transformation under all expected load and line conditions. Next, the selection of key resonant tank parameters is performed. The magnetizing-to-resonant inductance ratio significantly influences the shape and width of the gain curve. A larger L_n value typically results in a flatter gain curve, improving regulation but limiting the gain range. In this design, an L_n value of 13.5 is selected based on the characteristics of the gain curve, as observed from Fig.3 and Fig.4, in accordance with the reference design guidelines [5]. The effective quality factor Q_e, which significantly affects the sharpness and peak of the gain curve, is determined using Eq. 4 and 5.

$$L_n = L_m/L_r = 13.5 \quad \text{... (4)}$$

$$Q_e = sqrt(L_r/C_r)/R_e = 0.207 \quad \text{... (5)}$$

The parameter R_e represents the equivalent load resistance as seen from the primary side of the transformer and is calculated based on the nominal load current and the transformer turns ratio, as shown in Eq. 6.

$$R_e = (8*n^2/\pi^2)*(V_{out\_nom}/I_{out\_nom})$$
$$= (8*2.5^2/\pi^2)*(14.5/40) = 1.8365\Omega \quad ... (6)$$

3.3.2 Selection of switching frequency and determination of resonant tank parameters with gain curve analysis

Before proceeding with the calculation of the resonant tank component parameters, it is crucial to first select a nominal switching frequency, which corresponds to the resonant frequency (f_r) of the LLC converter. In this design, the resonant frequency is chosen to be 100 kHz. The resonant frequency is a key design parameter, as it directly influences the operational characteristics of the converter, including the energy transfer efficiency and the selection of resonant tank components.

Once the resonant frequency is selected, the resonant tank parameters, which include the resonant capacitor (C_r), resonant inductor (L_r), and magnetizing inductance (L_m), can be determined using the following equations. The value of the resonant capacitor C_r is calculated using Eq. 7. This equation considers the quality factor of the resonant tank and the equivalent load resistance, ensuring that the capacitor is appropriately sized to operate at the chosen resonant frequency.

$$C_r = 1/(2\pi*Q_e*f_r*R_e) = 4.187\mu F \quad ... (7)$$

The resonant inductor L_r is subsequently calculated based on the selected resonant frequency and the previously determined value of the resonant capacitor C_r, as shown in Eq. 8. This equation ensures that the inductor value is consistent with the selected resonant frequency and capacitor, allowing the LLC converter to operate efficiently at the desired frequency. Finally, the magnetizing inductance L_m is calculated based on the magnetizing-to-resonant inductance ratio L_n, as shown in Eq. 9.

$$L_r = 1/((2\pi*f_r)2*C_r) = 619.78nH \quad ... (8)$$

$$L_m = L_n*L_r = 8.37\mu H \quad ... (9)$$

Fig.4 presents the LLC gain curve, which illustrates the voltage gain of the converter as a function of the normalized switching frequency. This curve is fundamental for understanding how the converter behaves at different frequencies. The normalized switching frequencies corresponding to both the maximum and minimum gains can be identified by analysing the gain curve. Specifically, the normalized switching frequency at the minimum gain is $f_n(M_{\min})$ = 52.0 kHz, and at the maximum gain, is $f_n(M_{\max})$ = 115.1 kHz. The range of normalized switching frequencies is crucial for ensuring that the converter operates efficiently and maintains optimal performance throughout its operating range.

3.3.3 Inductive region operation and ZVS considerations

In our design, the resonant tank is configured to operate primarily in the inductive region to support ZVS. The transformer turns ratio and resonant tank elements were selected such that voltage regulation is obtained by operating the converter at switching frequencies at or above the resonant frequency, maintaining operation on the inductive side of the gain characteristic. Under inductive operation, the resonant current lags the switch-node voltage, providing sufficient commutation current during the dead time to discharge the switch output capacitances and allow turn-on at a low drain-to-source voltage, reducing switching loss.

Capacitive-region operation is avoided because it causes the current to lead the voltage, increasing the likelihood of reverse current and hard turn-on of the complementary switch, which raises loss, EMI, and device stress. Accordingly, the tank is designed such that the required gain can be achieved without entering the capacitive region across the intended input-voltage and load range. However, the experimental results indicate that near maximum power the soft-switching margin reduces as RMS current and parasitic effects increase, and deviations from ideal ZVS may occur, highlighting the need for adequate margin in dead time, magnetics, and parasitic control for operation close to rated load.

4. Implementation Approaches and Optimization Techniques

This section focuses on the practical implementation of the LLC resonant converter, highlighting key design considerations to optimize performance and reliability.

4.1 Design Considerations

In designing the PCB for the resonant converter (Fig.5), several critical considerations were taken into account to ensure electrical performance, thermal reliability, and mechanical robustness. The

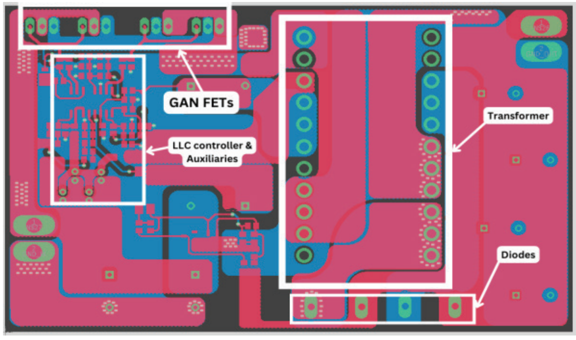

Figure 5 - Optimized PCB Layout for Minimizing Parasitic Effects and Improving Thermal Management

layout was developed using Altium Designer and utilizes a dual-layer copper structure with polygon pours on both sides. These pours are strategically connected with multiple vias to reduce resistive losses and to facilitate effective thermal dissipation, particularly for high secondary-side currents.

Key power components, such as GaN FETs, are thermally managed by placing them near the edge of the PCB, in direct contact with thermal pads coupled to the aluminium enclosure. This setup enhances heat transfer and maintains device temperatures within safe operating limits. In contrast, temperature-sensitive control elements, including the UCC256303 LLC resonant controller, are physically isolated from heat-generating elements like the transformer and power switches. This spatial separation prevents unintended triggering of internal thermal protection features and contributes to overall system stability. In addition, the design includes reverse polarity protection to safeguard the converter against accidental reverse connections. All power devices are appropriately derated according to ISO 16750-2 standards, ensuring reliable performance under typical automotive stress conditions.

4.2 High-Frequency Layout Optimization

In high-frequency resonant converters, particularly those using GaN devices, parasitic elements such as loop inductance and inter-trace capacitance become significant contributors to performance degradation. These parasitic result in voltage overshoots, ringing, and increased EMI, especially within the power and gate-drive loops. The PCB layout is planned to reduce loop area and parasitic inductance in the *dI/dt* switching paths to mitigate such issues. Critical power loops, including the primary switching loop and resonant current path, are routed with minimal physical area and direct connections using wide copper traces and solid polygon pours. Gate-drive signal integrity is preserved by employing tightly coupled signal-ground trace pairs with controlled impedance, particularly important for fast-switching GaN FETs that are sensitive to voltage and timing noise. Each driver circuit is provided with a dedicated return path to avoid common impedance coupling, thereby reducing gate ringing and false triggering. Low-ESL ceramic capacitors are placed as close as possible to the drain and source terminals of the GaN FETs to ensure stable operation of the GaN devices. This placement helps to provide localized energy storage, allowing the capacitors to quickly supply current during fast switching transitions.

Table 2 - Protection Limits Configured for the LLC Resonant Controller

Protection Parameter	Value
Over Temperature (OTP)	145°C
Input Over Voltage (INOVP)	75V
Input Under Voltage (INUVP)	63V

4.3 Advanced Protection Mechanisms for Enhanced Converter Reliability

This subsection details the protection features integrated into the converter to ensure safe, stable, and reliable operation under all conditions. The protection circuitry incorporates a wide range of mechanisms, including over- voltage, under-voltage, over-current, over-temperature, and reverse polarity protections. Each protection function is designed to detect abnormal conditions promptly and take immediate corrective action, such as disabling the power stage or initiating a safe shutdown, to prevent component damage and ensure long-term system durability.

4.3.1 Over-voltage and under-voltage protection

Both over-voltage protection (OVP) and under-voltage protection (UVP) mechanisms are integrated into the converter design to ensure safe operation and protect the power stage from abnormal conditions. The OVP circuit continuously monitors the output voltage using a bias winding that is magnetically coupled to the secondary side of the transformer. In this design, the turns ratio between the bias winding and the secondary winding is 3:2. Using this ratio, the nominal voltage of the bias winding can be calculated. Given the nominal output voltage of 14.5 V, the expected nominal bias winding voltage is 21.75 V, as indicated in Eq. 10.

$$V_{BiasWindingNom} = 14.5V*(3/2) = 21.75V \quad ... (10)$$

The controller interprets this voltage through its OVP sensing pin, which has a default trip threshold of 3.3 V. This threshold corresponds to 120% of the nominal value to ensure that the controller detects the nominal voltage properly, under standard operating conditions. Therefore, the expected nominal sensed voltage at the controller input is 2.75 V, as derived in Eq. 11.

$$V_{InputNom} = 3.3V/1.2 = 2.75V \quad ... (11)$$

In addition to output over-voltage protection, the input side of the converter is protected by implementing input over-voltage protection (INOVP) and input under-voltage protection (INUVP), as summarized in Table 2. These protection features are realized by sensing the input voltage through a resistor divider connected to a dedicated configuration pin. The divider is designed to trigger protective actions if the input voltage exceeds or drops below the predefined thresholds, thus maintaining safe and stable converter operation under varying supply conditions.

4.3.2 Over-current protection

The converter is equipped with a robust over-current protection (OCP) scheme that includes three distinct levels of protection to ensure safe operation under varying load conditions. This multi-tiered approach safeguards the system against both sudden current spikes and sustained overcurrent events by monitoring peak as well as average current levels. In this design, current sensing is carried out using a resonant current detection technique. Instead of employing a traditional current-sensing resistor in the main power path, which could introduce additional power losses, this method derives the resonant current from the voltage across the resonant capacitor. The sensing is implemented using a passive RC differentiator circuit composed of a capacitor C_{ISNS} and a resistor R_{ISNS} as shown in Fig.2. The output voltage of the differentiator, which corresponds to the rate of change of the input voltage, is described by Eq.12.

$$V_{ISNS}(t) = R_{ISNS}*C_{ISNS}*dV_{in}(t)/dt \quad ... (12)$$

Since the rate of voltage change across the resonant capacitor is proportional to the resonant current, the equation can be reformulated as Eq.13.

$$V_{ISNS}(t) = R_{ISNS}*I_{res}*(C_{ISNS}/C_r) \quad ... (13)$$

In this context, $V_{ISNS}(t)$ is the output voltage of the differentiator circuit, where I_{res} denotes the current through the resonant capacitor with capacitance C_r, and C_{ISNS} and R_{ISNS} are components of the sensing network.

The voltage signal V_{ISNS} is then compared with internally defined reference voltages by a comparator circuit to determine whether any of the current thresholds have been exceeded.

A summary of the three protection levels is provided in Table 3. These levels include:

- Peak Current Trip: Provides immediate protection when the input current exceeds 90 percent of its maximum allowable value. This level is designed to respond quickly to transient overcurrent conditions.
- High Threshold Trip: Introduces a delay of 2 milliseconds, allowing the system to tolerate brief current surges without triggering protection unnecessarily.
- Lower Threshold Trip: Activates if the current remains above a moderate threshold for 50 milliseconds. This level is intended to detect prolonged overloads that may indicate abnormal operation.

Table 3 - Summary of Current Protection Thresholds, Current Values, and Time Durations

Protection Threshold	Current Limit	Response Time
Peak Current Trip	7.2 A	Immediate
High Threshold Trip	6.5 A	2 ms
Lower Threshold Trip	5.3 A	50 ms

The corresponding voltage thresholds for each trip are calculated using Eq.13 to ensure that the comparators are triggered accurately under the defined conditions for the proper configuration of the protection levels.

4.3.3 Over-temperature protection

The selected controller is equipped with an integrated over-temperature protection (OTP) mechanism, which plays a critical role in safeguarding the converter from thermal damage. This protection is implemented using an internal temperature sensor and comparator circuit. When the measured temperature exceeds the predefined threshold, the controller disables operation, effectively shutting down the power stage to prevent any malfunction or permanent damage to the system.

This shutdown process is automatic and does not require any external intervention. However, the controller does not include a latch-off feature. As a result, once the temperature begins to decrease and falls below the threshold, the controller automatically attempts to restart. If the fault condition persists, the temperature may rise again, causing another shutdown. This cycle continues repeatedly until the root cause of the excessive heating is resolved or the ambient and system conditions return to a safe operating range.

4.3.4 Reverse polarity protection

The design incorporates reverse polarity protection to ensure that the converter operates safely even when the input voltage connections are reversed. Typically, reverse polarity protection is achieved using a diode, which prevents current from flowing when the input connections are incorrectly made. However, while this method provides a safety mechanism, diodes have an inherent drawback, as they introduce a forward voltage drop that results in power loss. This power loss can be particularly significant in high power systems where efficiency is critical. The forward voltage drop of the diode reduces the overall system performance, which is undesirable in a high-efficiency converter design.

Table 4 - Converter Performance Specifications: Output Current, Output Power, and Maximum Efficiency at Different Load Conditions

Output Current (A)	Output Power (W)	Maximum Efficiency (%)
1.21	17.52	82.96
6.28	90.80	84.11
9.55	136.28	90.07
17.50	251.66	92.56
29.64	424.90	88.59
35.26	497.52	88.25
39.48	548.11	86.89

Hence, an additional MOSFET switch is introduced into the reverse polarity protection circuit to mitigate the power loss associated with the diode. When the input voltage polarity is reversed, the MOSFET is activated to bypass the diode. This allows current to flow with minimal resistance and eliminates the forward voltage drop that would otherwise be introduced by the diode. As a result, the power loss is significantly reduced, and the overall system efficiency is improved. This approach ensures that the converter maintains its protective functionality while minimizing energy dissipation, thereby enhancing both efficiency and reliability.

5. Experimental Results and Discussion

This section presents the experimental results and a detailed discussion of the performance of the LLC resonant converter. It outlines the experimental setup and validation methodology, followed by a comparative analysis of GaN FETs versus MOSFETs in terms of performance.

5.1 Experimental Setup and Validation Methodology

The efficiency of the designed LLC converter was characterized over a range of load conditions using a programmable DC electronic load. Input and output voltages were recorded using precision multimeters, and currents were measured using calibrated current clamps, while overall efficiency was calculated from power analyser measurements. The measured output current, output power, and corresponding conversion efficiency for each operating point are summarized in Table 4.

As illustrated in Fig. 6, the converter efficiency improves as the output power increases from light load to the mid-load region, reaching a peak efficiency of 92.56% at approximately 250 W. Beyond this region, a gradual efficiency reduction is observed toward higher load levels. This behaviour is primarily attributed to increasing conduction losses at higher output currents due to resistive dissipation in the power path and interconnects, together with higher transformer winding and core losses as RMS current and flux density rise. In addition, the experimental waveforms

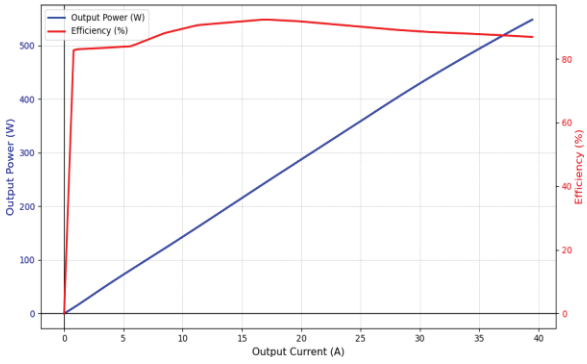

Figure 6 - Performance Characteristics of the LLC Resonant Converter: Output Power and Efficiency versus Output Current

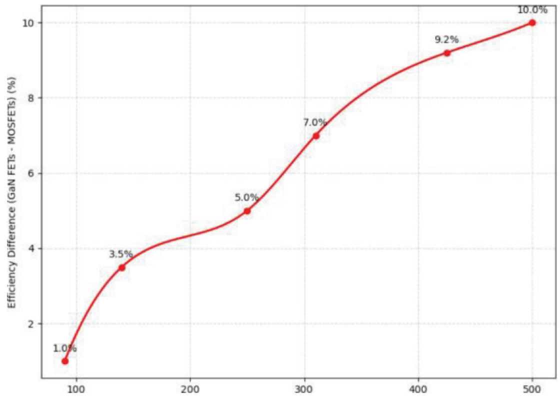

Figure 8 - Graph of the Efficiency Difference between GaN FETs and MOSFETs in Different Power Levels

indicate a reduced soft-switching margin at high-load, where the converter deviates from ideal ZVS behaviour, which increases switching-related losses and contributes to the measured efficiency roll-off near the upper end of the tested power range (Fig. 6).

5.2 Performance Comparison: GaN FETs vs. MOSFETs

This experiment compares the efficiency and performance of the converter using GaN FETs versus MOSFETs, where both devices have similar electrical ratings. Efficiency was measured under controlled conditions to ensure accurate results, including stable input voltage, varied load conditions, and regulated temperature using cooling. As shown in Fig.7, GaN FETs demonstrate higher efficiency than MOSFETs, especially at higher power levels. In the power range from 140W to 310W, the efficiency consistently exceeds 90%, reaching over 92% at 250W. This improved efficiency is attributed to the inherent characteristics of GaN FETs, including lower switching losses due to reduced output capacitance and faster transitions, higher switching frequencies enabled by greater electron mobility, and reduced conduction losses due to lower on-resistance, $R_{DS(on)}$.

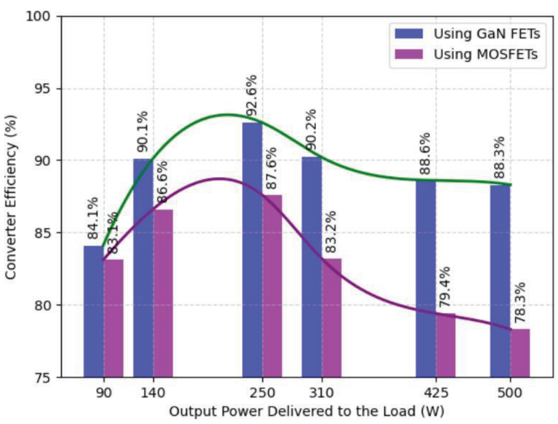

Figure 7 - Converter Efficiency Comparison Using GaN FETs and MOSFETs across Different Output Power Levels

Furthermore, the difference in efficiency between GaN FETs and MOSFETs increases with output power, highlighting the advantage of GaN FETs at higher power levels, as illustrated in Fig.8. The GaN FET-based converter demonstrated an efficiency improvement ranging from 1% at 90W to 10% at 500W. Beyond 250W, the MOSFET-based converter exhibits a significant decline in efficiency, indicating that GaN FETs are more effective for higher power level applications where efficiency is critical.

5.3 Mitigation of Oscillations in the Gate and Auxiliary Windings

In the initial testing phase, voltage spikes were observed at the gate-source junction of the GaN FETs. It was noted that the amplitude of these spikes increased with increasing power levels, as shown in Fig.9-Left. These voltage spikes can induce unwanted oscillations in the gate-drive signal, potentially leading to increased switching losses, EMI, and reduced device reliability. In addition to that, similar high-frequency oscillations were also observed in the auxiliary winding (Fig.9-Right), which is used for output-voltage protection sensing. These observations indicate that GaN-based LLC implementations are highly sensitive to parasitic inductance and coupling in both the gate-drive and sensing paths. Therefore, localized high-frequency decoupling and careful gate-network tuning are essential to maintain stable switching behaviour and reliable protection sensing as the operating power increases. The following actions were taken to address this issue, and the resulting improvements can be observed in Fig. 10.

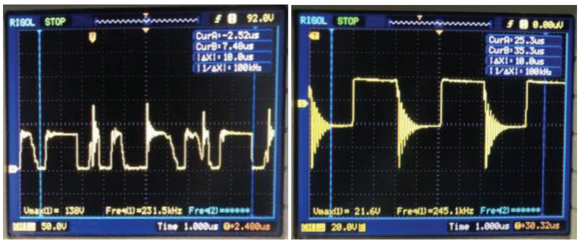

Figure 9 - Left: Initial Gate-Source Waveform Showing Significant Noise and High-Frequency Ringing Before Applying Any Filtering. Right: Auxiliary Winding Waveform Captured without Filtering During the Operation of the LLC Converter

1. **Bypass capacitors for noise filtering:** Bypass capacitors (0.1μF and 1μF) were added to the input side of the circuit to filter out high-frequency noise and stabilize the input voltage. These capacitors provide a low-impedance path for high-frequency currents, effectively shunting them away from the GaN FETs and reducing the noise that can couple into the gate-drive circuitry. Fig.10-Left shows that the addition of a 0.1 μF capacitor leads to a reduction in ripple, while Fig.10-Middle indicates that connecting both 0.1 μF and 1 μF capacitors in parallel at the input results in further suppression of ripple. These results indicate that localized high-frequency input decoupling should be placed as close as possible to the switching stage to reduce ringing and prevent noise coupling into the gate-drive loop, particularly at higher power levels.

2. **Gate resistor optimization for switching speed control:** The gate resistor is a critical component in controlling the charging and discharging rate of the gate capacitance in the switches, thereby directly influencing their switching behaviour. The gate resistance was reduced to 11Ω to achieve a desirable balance between the switching speed and the circuit stability, allowing better control over the switching transitions (Fig.10-Right). The switching transitions can be slowed down by carefully selecting an appropriate gate resistance value, which helps to suppress oscillations and minimize both switching losses and EMI. This demonstrates that gate resistance must be treated as a stability-critical tuning parameter in GaN-based LLC converters, requiring a deliberate trade-off between switching speed and damping to maintain clean transitions and controllable EMI.

Figure 11 - Efficiency Measurement of the LLC Resonant Converter at Various Output Power Levels, Performed with a Power Analyser

5.4 Efficiency Enhancement and Testing at Maximum Power

Efficiency measurements conducted at various load levels demonstrated a significant improvement from 84% to over 90%. As illustrated in Fig.11, the converter consistently maintains an efficiency exceeding 90% across a broad range of power levels. A significant factor contributing to the observed efficiency improvement was the use of higher value resistors in the voltage divider network, which reduced power dissipation while scaling down the voltage. This modification reduced power loss, as described by the relation $P_{loss}=V^2/R$ while preserving accurate voltage sensing. Furthermore, the gate resistance of the GaN FETs, which are responsible for power switching, was reduced. This reduction improves their switching speed and can potentially lead to a decrease in switching losses. Finally, the thermal management of the

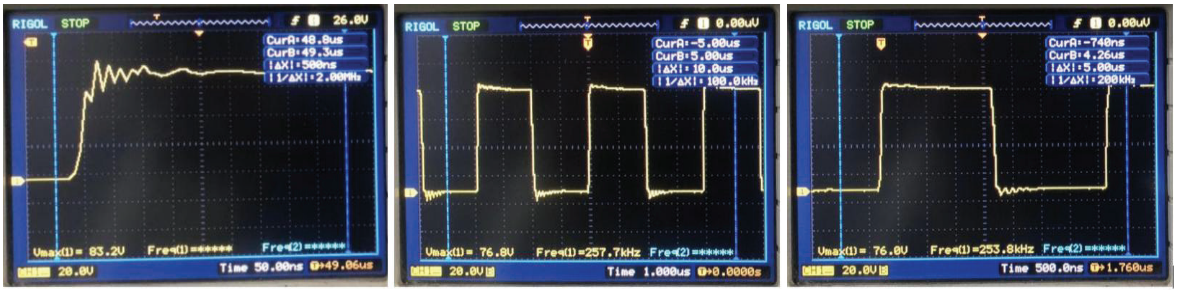

Figure 10 - Gate-Source Waveform Comparison Under Various Filtering and Gate Resistor Conditions. Left: Two 0.1 µF Capacitors in Parallel at the Input. Middle: Two 0.1 µF and One 1 µF Capacitors in Parallel at the Input. Right: Same Capacitor Setup with an Additional 11 Ω Gate Resistor

converter was improved by incorporating both forced air cooling and passive cooling (a metal enclosure acting as a heat sink). This combined cooling approach stabilized the operating temperature of the circuit board.

6. Conclusions

This paper presented the design and experimental validation of a 500 W half-bridge LLC resonant DC-DC converter using GaN FETs for 63-75 V input and a regulated 14.5 V output at up to 40 A. Experimental benchmarking at a nominal 100 kHz resonant frequency demonstrated peak efficiency above 90%, with the best measured value of 92.56% at approximately 250 W, and efficiency remaining above 90% over a mid-load region. In addition, the hardware prototype was validated under dynamic load conditions, confirming stable regulation and repeatable operation over the tested range. Beyond reporting efficiency figures commonly available in prior GaN-based LLC studies, the experimental results are used to expose practical design gaps related to high-load soft-switching margin and parasitic-driven stability limitations in real hardware.

A key outcome of the experimental study is that resonant-tank tuning allowed inductive-region operation over the measured operating range, supporting ZVS in typical and mid-load conditions and contributing to reduced switching loss. Practical high-frequency implementation effects were also observed, including gate-drive and auxiliary-winding oscillations that increased with load. These oscillations were mitigated through localized input bypassing and gate resistance adjustment, which improved waveform stability and reduced ringing in the measured signals. The integrated protection configuration, including input over- and under-voltage thresholds and multi-level over-current protection, further supported stable converter operation during transient and fault-related conditions.

A controlled device-level comparison on the same platform indicated that replacing silicon MOSFETs with GaN FETs improves conversion efficiency under the tested conditions, with the improvement increasing toward higher output power. However, the experimental results also highlight limitations at high-load. As the output power approached the upper end of the operating range (above approximately 480 W), efficiency decreased, and the converter exhibited reduced soft-switching margin due to increased conduction loss, higher transformer core and winding losses, and deviations from ideal ZVS behaviour. These observations indicate that ZVS cannot be assumed to be fully maintained under all extreme loading conditions without additional design margin, and they motivate further optimization of magnetic design, thermal management, and switching transition control for operation near maximum power.

Future work will focus on maintaining high-load soft-switching performance and improving end-range efficiency through adaptive frequency modulation and control refinement, further reduction of parasitic inductance through layout and packaging improvements, and optimized magnetics for lower core losses.

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