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Review of Existing Transformer-Less PV Inverter Topologies and Design a Modified Topology to Reduce Leakage Current

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Abstract: Transformer-less inverter is an attractive solution for grid connected photovoltaic systems. This type of inverter has a major problem of conducting leakage current during the switching. To overcome this problem, there are several inverter topologies which have been introduced to reduce the leakage current. Such existing topologies cannot reduce the leakage current completely because the common mode voltage cannot be kept constant. Common mode voltage is the average of the two output references. Therefore, this research has been conducted to compare the performance of existing transformer-less photovoltaic inverter topologies and design a modified topology to further reduce the leakage current.

Keywords: Transformer-less inverter, Leakage current, Common mode voltage

1. Introduction

Among all renewable energy sources, photovoltaic (PV) energy is generally rated as the most attractive and sustained source because it is available throughout the year. In the future, more than 45% of the needed power is anticipated to be generated by PV arrays. PV system, the electric power driven by the PV, must be efficiently consumed. Altered system structures can be used to enhance overall system efficiency.

PV arrays can deliver energy to stand-alone applications or utility grids. Delivering power to a utility grid is becoming an increasingly popular option. The cost of these systems depends on the PV module size. Therefore, to reduce the cost of the unit, the DC/AC inverter followed by a line transformer is used. The line transformer realizes the following goals:

(1) Galvanic separation between the PV array and the utility electricity network and consequently achieves individual protection and safety.
(2) Raises the voltage produced by the inverter to a suitable value to meet the utility grid voltage.

These transformers have many drawbacks including high system cost and decreased efficiency [4]. Also, the transformers are very large and heavy.

The leakage current is produced due to the alternation in the common mode (CM) voltage of the inverter. The variation of the CM voltage must be minimized to diminish the leakage current. Without a line transformer, leakage current forms through parasitic capacitances between the PV array and the ground. The leakage current results in radiated interfering problems and other severe safety issues; the current must be reduced to limited values.

To resolve the issue concerning leakage current, several solutions can be used. Conventional half-bridge inverters can be utilized, but the main problem involves DC voltage utilization at 50% and the significant number of PV arrays needed.

Conventional Full bridge inverters with bipolar or unipolar sinusoidal pulse width modulation (SPWM) can solve the problems created by half-bridge inverters. With bipolar SPWM, the current ripples in the filter inductors and switching losses are high while with unipolar SPWM the common mode voltage changes at switching frequency, something which results in high leakage current. Another approach to minimize leakage current is to employ transformer-less inverters. The basic idea of transformer-less inverters is to disconnect the DC side (PV array) from the AC side (inverter and grid) in freewheeling modes. Consequently, the CM voltage is kept nearly constant.

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Transformer-less PV systems demonstrate the advantages of lower cost, lower system size, and higher efficiency when compared to line transformer systems.

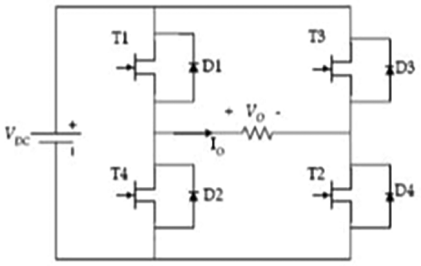
Several topologies have been developed including highly efficient and reliable inverter concept (HERIC) topology, such as H5 and H6 topologies. Various versions with modifications to those transformer-less inverters have been introduced. Each topology has its own benefits and drawbacks involving the ability to reduce leakage current, the number of switches and their total losses, and system efficiency and cost. Among these inverters, this research mainly discusses existing topologies and their features, faults and provide a solution to the existing problems by designing a modified topology.

2. Literature Review

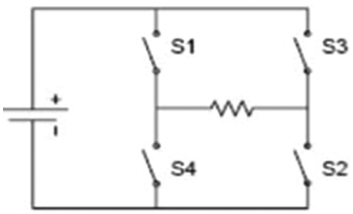
This section shows the circuit diagrams of full bridge inverter structure and how the leakage current issue arises in single phase full bridge inverter.

2.1 Single Phase Full Bridge Inverter Function

Full bridge inverter is the basic circuit to convert DC to AC. In this circuit, an AC output is synthesized from a DC input by closing and opening switches in an appropriate sequence. There are four different states depending on which switches are closed. Figure 1(a) shows the circuit diagram of a single phase full bridge inverter and Figure 1(b) shows the simplified version of the full bridge inverter, where I_0 is the output current and V_0 is the output voltage.

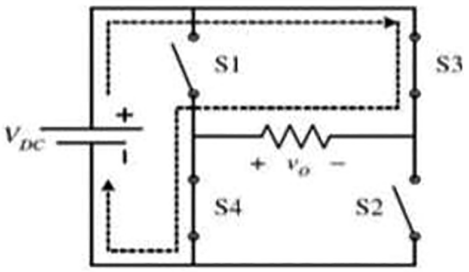


(a)



(b)

Figure 1 – Single Phase Full Bridge Inverter



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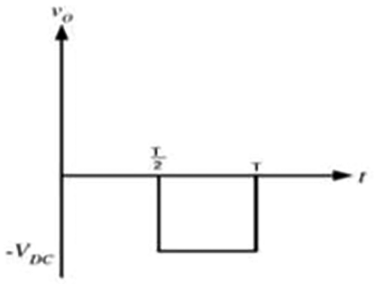

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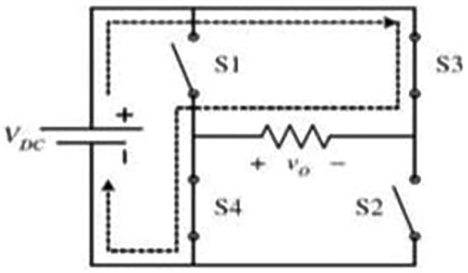
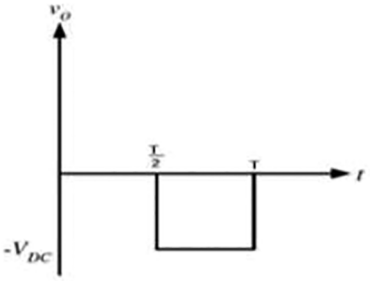
Figure 2 - Function when S1 & S2 On

The Output voltage waveforms of single phase full bridge inverter during each switching state are shown in Figures 2 and 3.



(a)



(b)

Figure 3 - Function when S3 & S4 On

2.2 The Occurrence of Leakage Current in Transformer-Less Inverter

The circuit diagram of full bridge inverter is shown in Figure 4. There are four IGBTs as switches.

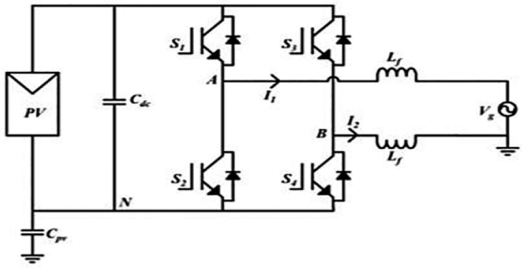


Figure 4 - Full Bridge Inverter

The common mode and differential mode voltage of the circuit in terms of V_{AN} and V_{BN} are shown in Eq. (1) and Eq. (2). Therefore, Figure 5 shows the simplified common mode circuit of the full bridge inverter with the total common mode voltage [7] shown in Eq. (3). V_{CM} is common mode voltage and V_{DM} is different mode voltage. V_{DM} is the difference between V_{AN} and V_{BN} and represents Eq.(2).

$$V_{CM} = (V_{AN} + V_{BN}) / 2 \quad \ldots(1)$$

$$V_{DM} = V_{AN} - V_{BN} \quad \ldots(2)$$

$$V_{CMV} = V_{CM} + V_{DM} (L_2 - L_1) / 2(L_2 + L_1) \quad \ldots(3)$$

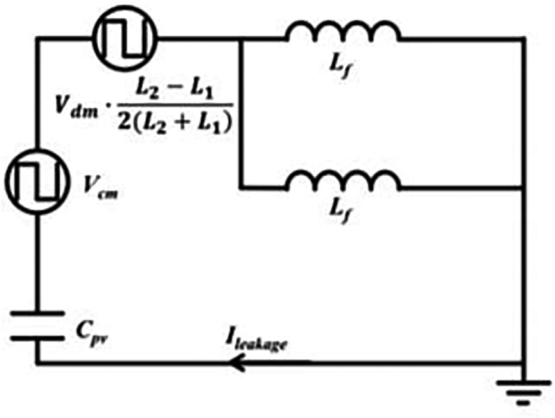


Figure 5 - Simplified Common Mode Voltage

By assuming the inductors used [8] in the filter have the same value, Eq. (3) can be further simplified to Eq. (4).

If there is a variation in the common mode voltage of the inverter, the leakage current will be induced according to Eq. (5) and the leakage current will flow through the parasitic capacitance [8] of PV array. Figure 6 shows the leakage current path of Transformer-less Inverter circuit.

$$V_{CMV} = V_{CM} = (V_{AN} + V_{BN})/2 \quad \ldots(4)$$

$$I_{Leakage} = C_{pv} \, dV_{cm}/dt \quad \ldots(5)$$

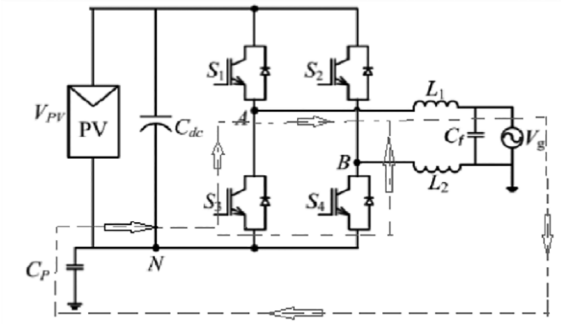


Figure 6 - Leakage Current Path of Transformer-Less PV Inverter

V_{AN} and V_{BN} vary when the IGBTs switch off the inverter. Both voltages will act as the varying voltage source. The variation of V_{AN} and V_{BN} in the inverter circuit induces a leakage current [9] V_{BN} in the inverter circuit which flows through C_{PV}. When compared to existing topologies, the H5 topology [6] has the best leakage current characteristics and HERIC and H6 topologies have medium range leakage current characteristics. Currently, a variety of topologies have been used to reduce leakage current. H5, H6, HERIC are a few of these. But, each topology has different kind of shortcomings. The main problem is that the common mode voltage (CMV) is not constant during the operation modes. SPWM signal is used for giving the input signal for IGBT s.

This research provides a solution for reducing the leakage current of HERIC topology by designing and implementing a modified topology.

3. Methodology

This section shows the steps to design the modified topology and how to verify it.

- Study the inverter function and how the leakage current has occurred
- Investigate the existing topologies used for reducing the leakage current

- Find the output leakage current and waveform of leakage current when providing the same input voltage to each topology by using simulation software
- Propose a new topology to further reduce the leakage current of transformer-less inverter

4. Design of the System

This section describes the modifications used in designing the new modified topology with the circuit diagrams and their functions.

4.1 Shortages and Issues of Existing Topologies

There are two methods to reduce leakage current:

- Separating PV array away from the grid (galvanic isolation method)
- Adding an extra clamp circuit

For the first method of separating the PV array away from the grid, some switches are added into existing topologies, such as H5, H6, HERIC. But the common mode voltage cannot be fully constant using the first method as freewheeling periods cannot be identified by the switching state, which means CMV is not constant. Therefore, a significant amount of leakage current occurs.

The proposed modified topology is derived from the conventional HERIC topology where parallel switches are used to replace series switches of the AC side. The HERIC topology reveals that the leakage current is in the medium range and CMV in not fully constant. Therefore, the proposed topology is improved by incorporating the clamped method technique to reduce leakage current.

To achieve constant CMV during the freewheeling period, the DC link capacitor is divided into two series capacitors to achieve the voltage divider. In the clamping method, an extra active switch is added to the proposed topology. This switch is known as a clamping switch and is placed between the midpoint of the bridge arms and the midpoint of the DC link capacitors according to Figure 7.

4.2 Proposed Modification to HERIC Topology

The proposed modified topology is based on the following improvements. From now on the new modified topology will be called an 'Optimized HERIC modified topology'.

- DC link capacitor is divided into two series capacitors to achieve the voltage divider
- Extra IGBT added to the HERIC topology and placed between the midpoint of the DC link capacitor and the midpoint of bridge arms
- Parallel IGBTs are used to replace the series Q5, Q6 IGBTs

4.3 Optimized HERIC Modified Topology

The optimized HERIC modified topology is derived from the conventional HERIC topology by adding an extra switch between DC link capacitors and bridge arms. The optimized HERIC modified topology is represented in Figure 7.

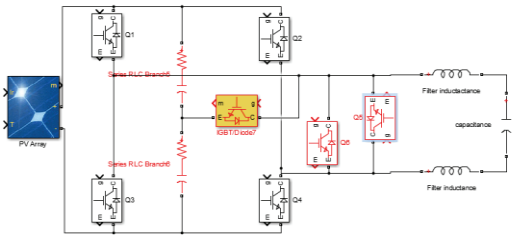


Figure 7 – Optimized HERIC Modified Topology

4.4 Working Principle of Optimized HERIC Modified Topology

Mode 01

Mode 01 is the active mode positive half cycle. In this mode, Q1 and Q4 switches are turned ON and other switchers are turned OFF. The current is flowing through Q1 and Q4 according to Figure 8.

The common mode voltage in mode 01 is calculated as follows:

$V_{CM} = (V_{AN} + V_{BN}) / 2$

$V_{AN} = V_{PV}$, $V_{BN} = 0$

Then, $V_{CM} = (V_{PV} + 0)/2 = V_{PV}/2$

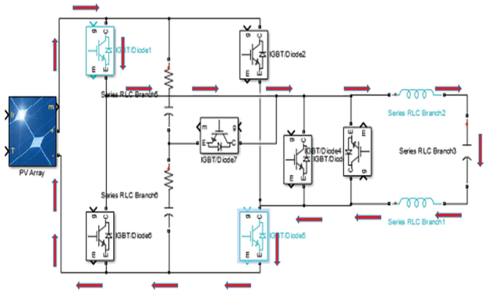


Figure 8 - Operation Mode 01 (Active Mode Positive Half Cycle)

Mode 02

Mode 02 is the freewheeling mode positive half cycle. In this mode, the Q6 switch is turned ON and other switchers are turned OFF. The current is flowing through Q6 according to Figure 9. The common mode voltage in mode 02 is calculated as follow,

$V_{CM} = (V_{AN} + V_{BN}) / 2$

$V_{AN} = ½ V_{PV}$, $V_{BN} = ½ V_{pv}$

Then, $V_{CM} = (½ V_{PV} + ½ V_{PV})/2 = V_{PV}/2$

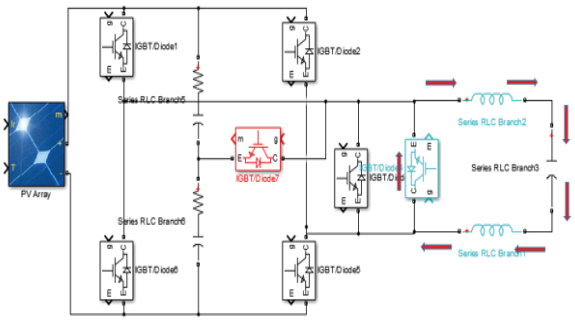


Figure 9 - Operation Mode 02 (Freewheeling Mode Positive Half Cycle)

Mode 03

Mode 03 is the active mode negative half cycle. In this mode, Q2 and Q3 switches are turned ON and other switchers are turned OFF. The current is flowing through Q2 and Q3 according to Figure 10.

The common mode voltage in mode 03 is calculated as follows,

$V_{CM} = (V_{AN} + V_{BN}) / 2$

$V_{AN} = 0$, $V_{BN} = V_{PV}$

Then, $V_{CM} = (0+V_{PV})/2 = V_{PV}/2$

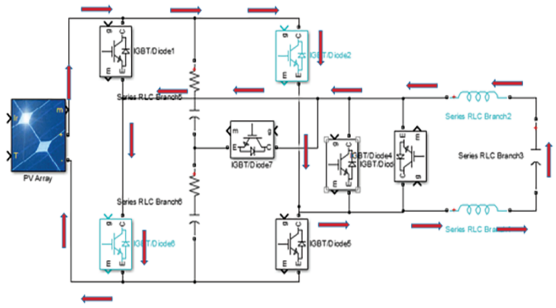


Figure 10 - Operation Mode 03 (Active Mode Negative Half Cycle)

Mode 04

Mode 04 is the freewheeling mode negative half cycle. In this mode, the Q5 switch is turned ON and other switchers are turned OFF. The current is flowing through Q5 according to Figure 11. The common mode voltage in mode 04 is calculated as follows,

$V_{CM} = (V_{AN} + V_{BN}) / 2$

$V_{AN} = ½ V_{PV}$, $V_{BN} = ½ V_{pv}$

Then, $VCM = (½ V_{PV} + ½ V_{PV})/2 = V_{PV}/2$

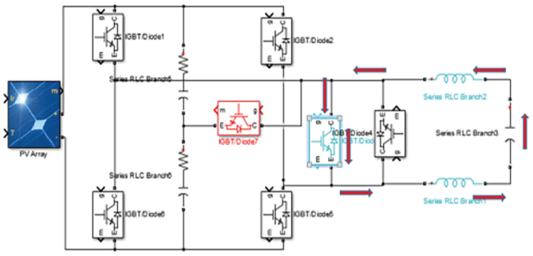


Figure 11 - Operation Mode 04 (Freewheeling Mode Negative Half Cycle)

5. Implementation of the System

In order to compare the H5, H6 and HERIC topologies, all simulations are carried out using MATLAB Simulink simulation software. A DC voltage source is used as the input to the inverter. The switching frequency is 10 kHz.

5.1 Simulation Block Diagram and Simulation Diagram of Optimized HERIC Modified Topology

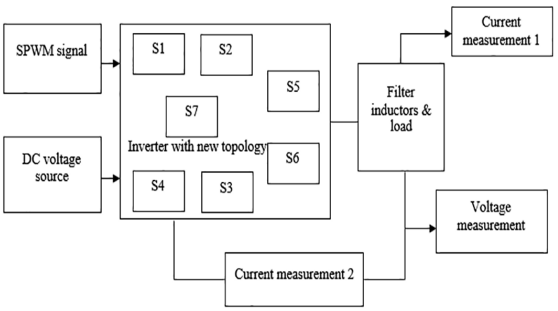


Figure 12 - Simulation Block Diagram of Optimized HERIC Modified Topology

- DC voltage source - Provide DC voltage as the PV array in the real application
- SPWM signal - Provide a SPWM signal for IGBTs
- IGBTs (S1, S2, S3, S4, S5, S6, S7) - IGBTs used as switching devices

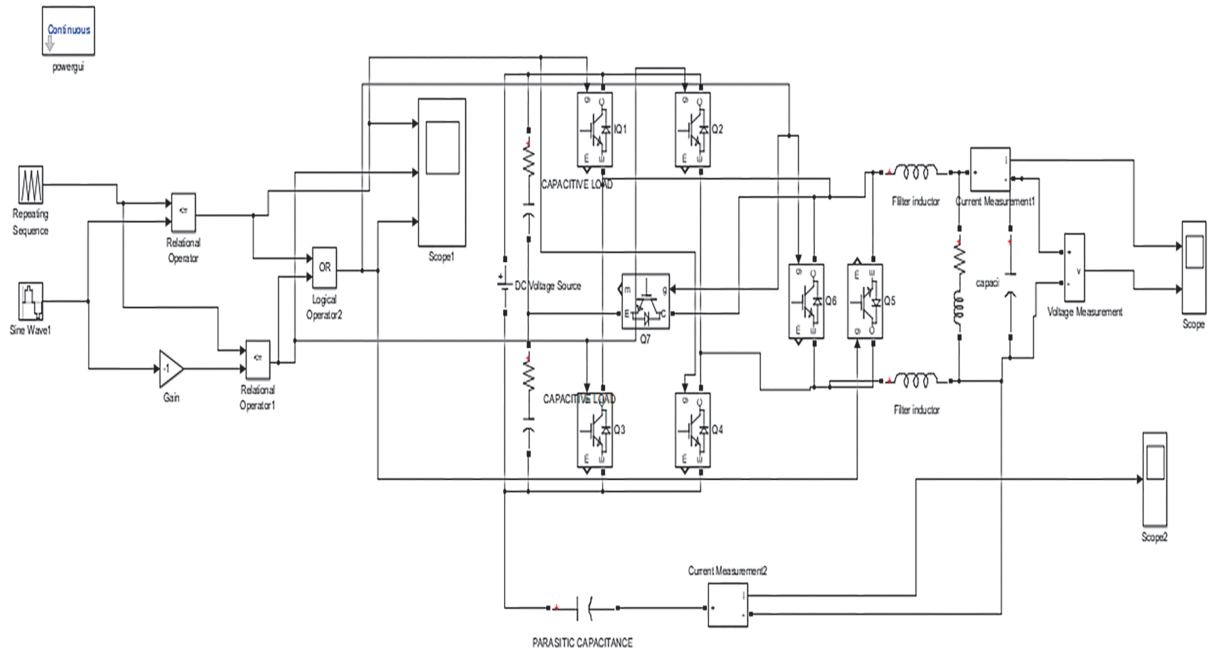


Figure 13 - Simulation Schematic Diagram of New Proposed Topology

- Filter inductors -Filter inductors are used for filtering output current
- Current measurement 1 -To observe the output current
- Current measurement 2 -To observe the leakage current passing through the parasitic capacitance
- Voltage measurement - To observe the output voltage

5.2 Simulation Specifications

The values of the components used in the H5, H6, HERIC and modified inverter circuits are presented in Table 1.

Table 1 – Simulation Specification

Parameter	Rating	Parameter	Rating
Input voltage range	230V – 500V	Filter inductance	55 H
Grid voltage	230V	Filter capacitance	470nF
Grid frequency	50 Hz	Switching frequency	10KHz

5.3 Input Signal of Proposed Topology

The harmonics in the inverter can be reduced using (SPWM) system [2]. The SPWM is used in which sine wave is the modulating wave and the triangular wave is the carrier wave. In the carrier based PWM techniques, the desired voltage reference waveform is referred to as modulating wave. In addition, a wave that is modulated with the modulating wave is referred to as a carrier wave. The carrier wave usually has a much higher frequency than the modulating wave. Figure 14 shows how to make SPWM signal. The SPWM signal is generated according to the magnitude at which the modulation signal intersects with the carrier signal.

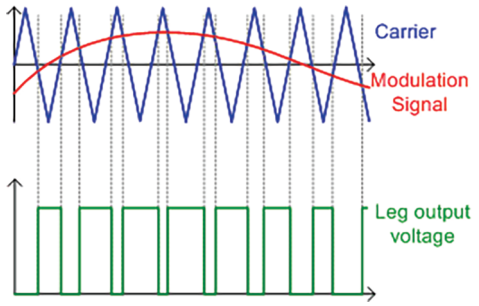


Figure 14 - Generation of SPWM Signal for IGBTs

5.4 Necessary Hardware and Related Instruments to Implement the Proposed Topology

This section presents the hardware needed to implement optimized HERIC modified topology, the types, and quantities.

5.4.1 Necessary Hardware

The necessary hardware of the proposed systems is given in Table 2.

Table 2 – Necessary Hardware of the Proposed Systems

Hardware	Quantity
IGBTs (FQA60N60)	7
Filter inductor (55mH)	2
Capacitors (0.47 µF)	3
(0.47 mF)	1
Resistors (1000 Ω)	1
(10 Ω)	2
Gate driver (IRS2453DS)	7

5.5 Driver Circuit Diagram of Optimized HERIC Modified Topology

A driver circuit is required for the IGBT to function. IRS2453D driver was selected for this purpose. The reason for choosing this IGBT driver is because it can maintain a voltage of about 625V and the switching speed is fast. Figure 15 represents the typical connection diagram of the driver circuit and IGBTs.

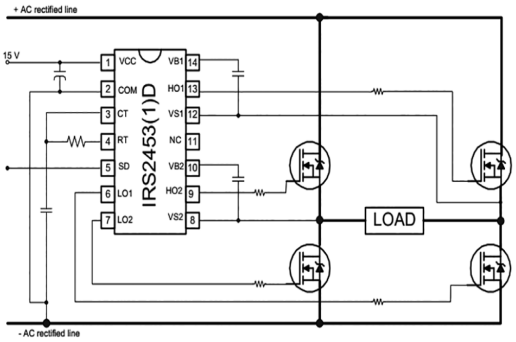


Figure 15 - Typical Connection Diagram of Gate Driver and IGBTs

6. Simulation Results

All simulations were carried out using MATLAB Simulink software. The simulation schematic diagram of the new proposed topology is shown in figure 13 and the simulation output waveform of input SPWM signal for IGBTs is shown in Figure 16.

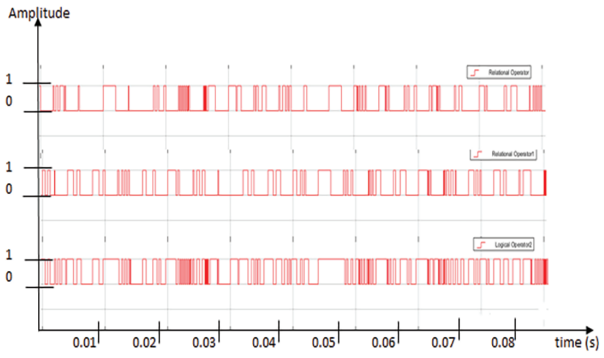


Figure 16 - Simulation Output Result of Input SPWM Signal

Leakage current results are obtained within a period of 10 millisecond and the maximum

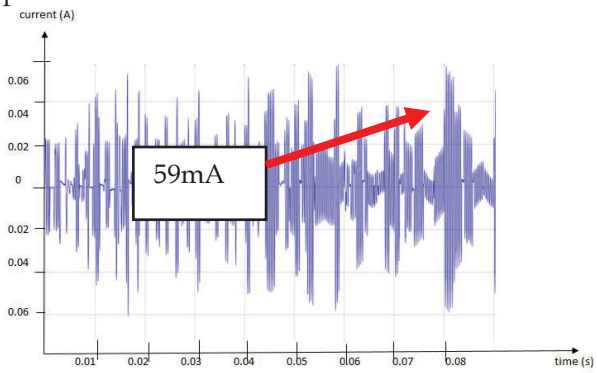


Figure 17 - Leakage Current Characteristic of H5 Topology

moments during that time are represented by the following figures. The leakage current characteristics of H5 topology and H6 topology are shown in Figure 17 and Figure 18 and H5 topology has a maximum leakage current of 59 mA.

The leakage current characteristic of HERIC topology is shown in Figure 19 and HERIC topology has a maximum leakage current of 95 mA.

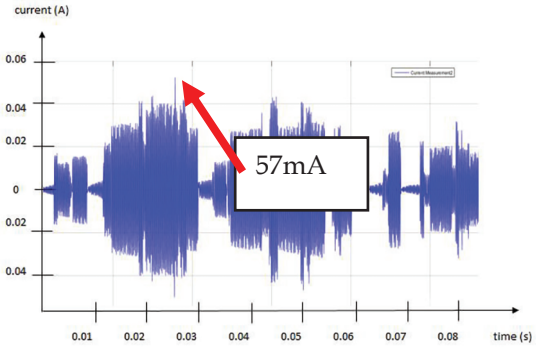


Figure 18 - Leakage Current Characteristic of H6 Topology

Figure 19 - Leakage Current of HERIC Topology

The simulation output voltage and current wave form of proposed topology are shown in Figure 20 and its leakage current characteristic is shown in Figure 21.

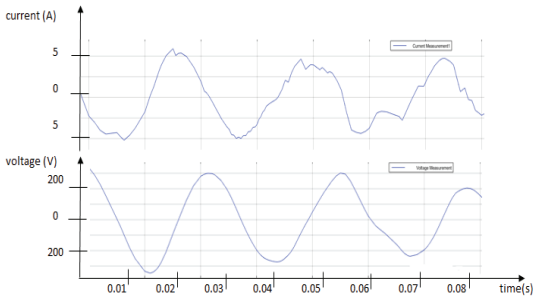


Figure 20 - Output Voltage and Current of Optimized HERIC Modified Topology

Optimized HERIC modified topology has maximum leakage current of 9mA. Optimized HERIC modified topology has a best leakage current value compared to other existing topologies.

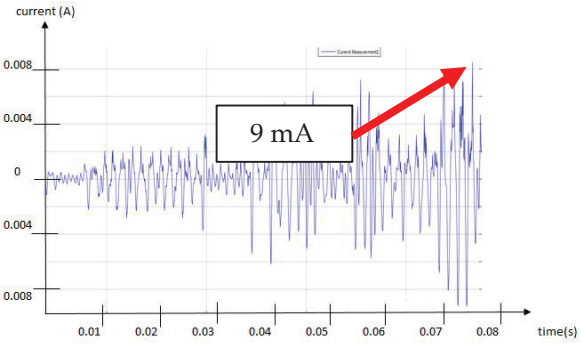


Figure 21 - Leakage Current Characteristic of Optimized HER IC Modified Topology

The maximum leakage current of topologies is shown in Table 3.

Table 3 - Maximum Leakage Current of Topologies

Type of topology	Maximum leakage current (mA)
H5	59
H6	57
HERIC	95
Optimized HERIC modified topology	09

According to the above leakage current values, the lowest leakage current value is in the optimized HERIC modified topology.

7. Conclusion and Future Works

Based on the results of simulations, the performance of the existing topologies and the optimized HERIC modified topology have been compared.

When measuring the leakage current, the leakage current passing through the parasitic capacitance was found by using multi meter and oscilloscope. The SPWM signal is used as an input signal for IGBTs. From these results a common problem was identified in every existing topology. The problem is that the common mode voltage cannot be kept constant. From the simulation it is observed that the modified topology can solve this problem by adding a clamping circuit to significantly reduce the leakage current.

Performance comparison results and simulated results indicate that the optimized HERIC modified topology can effectively reduce the leakage current to an acceptable level. The maximum leakage current is 300 mA, which is the standard leakage current [1]. The optimized HERIC modified topology has better performance as compared to the other existing topologies in terms of leakage current reduction.

Future improvements can be made in accordance with the optimized HERIC modified topology in many ways. Optimized HERIC modified topology can be enhanced by considering total harmonic distortion (THD). This can be the implementation by considering the MPPT technique and also comparison of the reactive power capability of topologies.

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