Materials Science-Poland
Volume 43 Issue 2 · pp. 143–152 · DOI: 10.2478/msp-2025-0025

Materials Science-Poland

Time-dependent gate breakdown reliability and gate leakage improvements in *p*-GaN MOS-HEMTs using Al_2O_3 gate dielectric

Research Article

Tsung-I Liao[1], Sheng-Po Chang[2]*, Shoou-Jinn Chang[3]

[1] *Program on Semiconductor Manufacturing Technology, Academy of Innovative Semiconductor and Sustainable Manufacturing, National Cheng Kung University, Tainan City 701, Taiwan*
[2] *Department of Microelectronics Engineering, National Kaohsiung University of Science and Technology, Kaohsiung City 81157, Taiwan*
[3] *Institute of Microelectronics & Department of Electrical Engineering, National Cheng Kung University, Tainan City 701, Taiwan*

Received 11 June 2025; Accepted 04 August 2025

Abstract: In this study, a 10 nm Al_2O_3 layer was deposited on the *p*-type gallium nitride (*p*-GaN) layer using thermal atomic layer deposition to form a metal–oxide–semiconductor high-electron mobility transistor (MOS-HEMT), designed to achieve lower gate leakage current. For comparison, a conventional *p*-GaN gate HEMT with an ohmic gate contact was employed. Transfer length method analysis of device resistance confirmed a reliable ohmic contact on the source/drain, with a low sheet resistance (R_{sh}) indicating a high-density two-dimensional electron gas in the access region, unaffected by the residual *p*-GaN etching process. To further explore the role of post-deposition annealing (PDA) in MOS-HEMTs, the characteristics of devices with and without PDA treatment were evaluated. Our conventional ohmic gate device exhibited excellent enhancement-mode (E-mode) characteristics, with all devices demonstrating low reverse gate leakage below 1×10^{-6} mA/mm. Compared to ohmic-gate HEMTs, PDA-treated devices showed reduced gate leakage and improved reliability, achieving a 10-year lifetime at 7.2 V through time-dependent gate breakdown analysis, despite reduced ON-state performance. We analyzed the differences among the three devices based on their respective gate leakage currents.

Keywords: *Enhancement-mode* • p-*GaN gate MOS-HEMT* • *Transfer length method* • *Post-deposition annealing*

1. Introduction

Gallium nitride (GaN), characterized by its wide bandgap and high-electron mobility, has become a standout material in the field of power devices [1–3]. Devices made using AlGaN/GaN high-electron mobility transistors (HEMTs) demonstrate a remarkable ability to reduce energy consumption during high-power operation [4,5]. By adopting a *p*-GaN gate structure, enhancement-mode (E-mode) device operation can be achieved, enabling extremely high conversion efficiency and further delivering high power density [6]. Its key advantage lies in providing better controllability during the epitaxial process compared to other approaches. This approach also represents one of the most commercially viable technologies available today [7]. However, a significant challenge associated with this technology is the ON-state gate time-dependent dielectric breakdown, which occurs when the gate-source voltage is high and sustained for a sufficiently long duration, leading to leakage issues [8–12]. This also tests the durability and reliability of E-mode *p*-GaN HEMTs. One potential solution to address this issue is to add an insulating layer on the *p*-GaN gate, and this modification can increase the threshold voltage (V_{th}) and reduce gate leakage [13–15]. Al_2O_3 was selected as the gate dielectric material due to its wide bandgap, high thermal stability, and excellent interface quality with GaN, which are critical for suppressing gate leakage and enhancing device reliability [16,17].

In previous studies, it has been shown that the residual *p*-GaN outside the gate region must be etched only after removing the oxide layer. To achieve this, conventional approaches often utilize inductively coupled plasma

* *E-mail: changsp@nkust.edu.tw*

Open Access. © 2025 Tsung-I Liao *et al.*, published by Sciendo
This work is licensed under the Creative Commons Attribution-NonCommercial-NoDerivs 4.0 License.

reactive ion etching (ICP-RIE) techniques [13,18,19]. Additionally, the transfer length method (TLM) has been widely employed to extract contact and sheet resistances, serving as an effective means to validate the formation of reliable source/drain ohmic contacts and to confirm the presence of a two-dimensional electron gas (2DEG) within the channel region [20].

In this work, we propose two process improvements for *p*-GaN gate-based E-mode HEMTs. First, we develop a self-aligned two-step etching process using two consecutive ICP-RIE recipes to separately remove the oxide and residual *p*-GaN layers outside the gate region, thus eliminating the need for an additional mask. Second, we assess the feasibility of this etching process by extracting the device's contact and sheet resistance via TLM. Furthermore, we deposit a 10 nm Al_2O_3 layer on the *p*-GaN using thermal atomic layer deposition (ALD) to fabricate a metal–oxide–semiconductor high-electron mobility transistor (MOS-HEMT) structure and compare its performance to that of a conventional *p*-GaN gate HEMT with an ohmic gate contact. To further evaluate the long-term reliability of the gate dielectric, we also perform time-dependent gate breakdown (TDGB) measurements [9,21]. Finally, the role of post-deposition annealing (PDA) in enhancing MOS-HEMT performance was investigated by comparing the DC characteristics and TDGB lifetime of devices with and without PDA treatment.

2. Experiment

The HEMTs we fabricated are based on a commercial GaN-on-Si substrate. This substrate is formed by heteroepitaxially growing an AlGaN/GaN structure on a 6-in. (111) silicon wafer using metal-organic chemical vapor deposition. It consists of a 1 µm carbon-doped GaN buffer layer, a 300 nm channel layer, a 1 nm AlN spacer layer, a 12.5 nm AlGaN barrier layer, and a 100 nm *p*-GaN layer. The fabrication process of the standard *p*-GaN gate HEMT with an ohmic-gate contact (Figure 1(a)) involves several steps. First, mesa isolation is performed using ICP-RIE. Next, the 100 nm *p*-GaN layer above the source and drain regions is removed by ICP-RIE. Following this, source/drain ohmic contacts are formed with a Ti/Al/Ti/Au (25/125/45/90 nm) metal stack, which is deposited and then annealed at 800°C for 1 min using a rapid thermal annealing system. The source-to-drain spacing (L_{SD}) is 10 µm. Subsequently, the gate metal, consisting of a Ni/Au (45/90 nm) stack, is deposited to act as a hard mask for further etching. The gate length (L_G) is 2 µm, and the gate width (W_G) is 100 µm. The residual *p*-GaN layer in regions outside the three electrodes is then etched using ICP-RIE to complete the device fabrication process. In addition to the standard ohmic gate contact device, we also fabricated another type of device, an MOS-HEMT (Figure 1(b)), which features an oxide layer between the gate metal and the *p*-GaN layer. The key difference lies in the fabrication process following the completion of the source/drain ohmic contacts. A 10 nm layer of Al_2O_3 was deposited using thermal ALD at 300°C. After ALD, PDA was performed at 600°C for 10 min in N_2 ambient to smoothen the oxide/*p*-GaN interface. To verify the necessity of the PDA process, we also fabricated an MOS-HEMT without PDA and measured its characteristics as a reference. Following patterning the gate, a two-step etching process was performed using different ICP recipes. In the first step, the Al_2O_3 layer was etched, followed by etching of the remaining *p*-GaN layer to complete the device fabrication process. Traditionally, Al_2O_3 is removed using HF wet etching, but this isotropic process often leads to imprecise linewidth

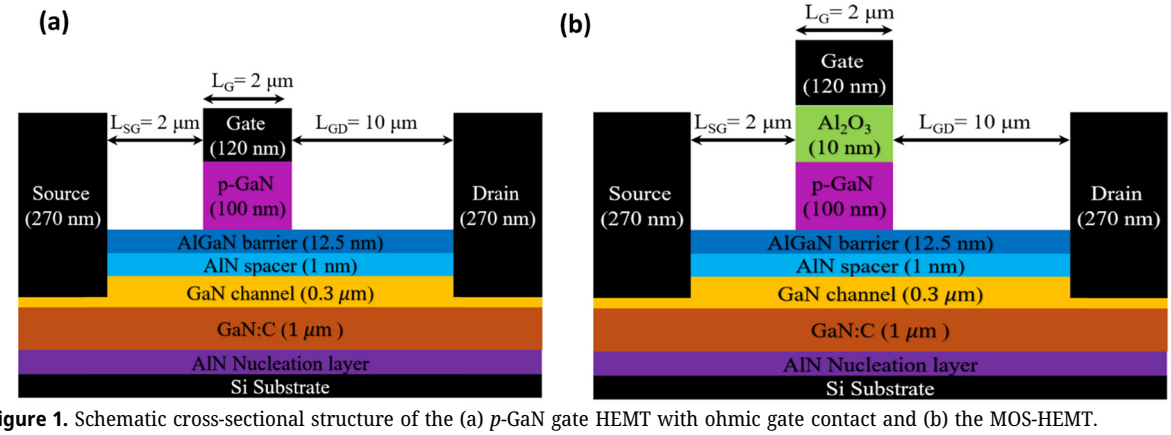

Figure 1. Schematic cross-sectional structure of the (a) *p*-GaN gate HEMT with ohmic gate contact and (b) the MOS-HEMT.

control and potential contamination issues. In contrast, ICP anisotropic etching allows for much more precise linewidth control, effectively addressing these problems. This approach is particularly advantageous for the future development of MOS-HEMTs with smaller gate linewidths. By adopting this method, one not only avoids the drawbacks associated with HF etching but also provides a more reliable fabrication process for improved device performance.

The residual *p*-GaN etching is difficult and critical to the entire HEMT process [19,22]. To address this, we developed a Cl_2/O_2/Ar etching recipe with a selectivity of about 1:10 between AlGaN and *p*-GaN. This selectivity allowed the AlGaN barrier to act as an etch-stop layer. As shown in Figure 2, the selective etching forms an oxidation layer on the AlGaN, preventing further etching. This etching recipe ensures that we achieve the expected device performance. We will also verify the sheet resistance in the access region of our device through TLM to ensure it is sufficiently low, confirming the successful completion of the etching process.

3. Results and discussion

Figure 3(a)–(c) shows the resistance of the *p*-GaN gate HEMT with ohmic gate contact and the MOS-HEMTs before and after PDA treatment, which are analyzed using the TLM pattern. The top-view image of the TLM pattern is shown in the inset of Figure 3(a). The results indicate that our devices have a reasonable ohmic contact on source/drain, with contact resistance (R_C) all below 5 Ω·mm and a low specific contact resistivity (ρ_C). Additionally, the low sheet resistance (R_{sh}) of ~1 kΩ/sq suggests that the access region has a high-density 2DEG, which was not diminished by our residual *p*-GaN etching process [23]. The consistency of the TLM results confirms that the MOS process does not affect the performance of the ungated region.

Figure 4(a)–(c) shows the *I*–*V* characteristics of the *p*-GaN gate HEMT with an ohmic gate contact. Specifically, Figure 4(a) demonstrates a V_{th} of 0.81 V and a subthreshold swing (SS) of 75.61 mV/dec. These results indicate that our standard ohmic gate device not only exhibits E-mode characteristics but also demonstrates excellent gate control.

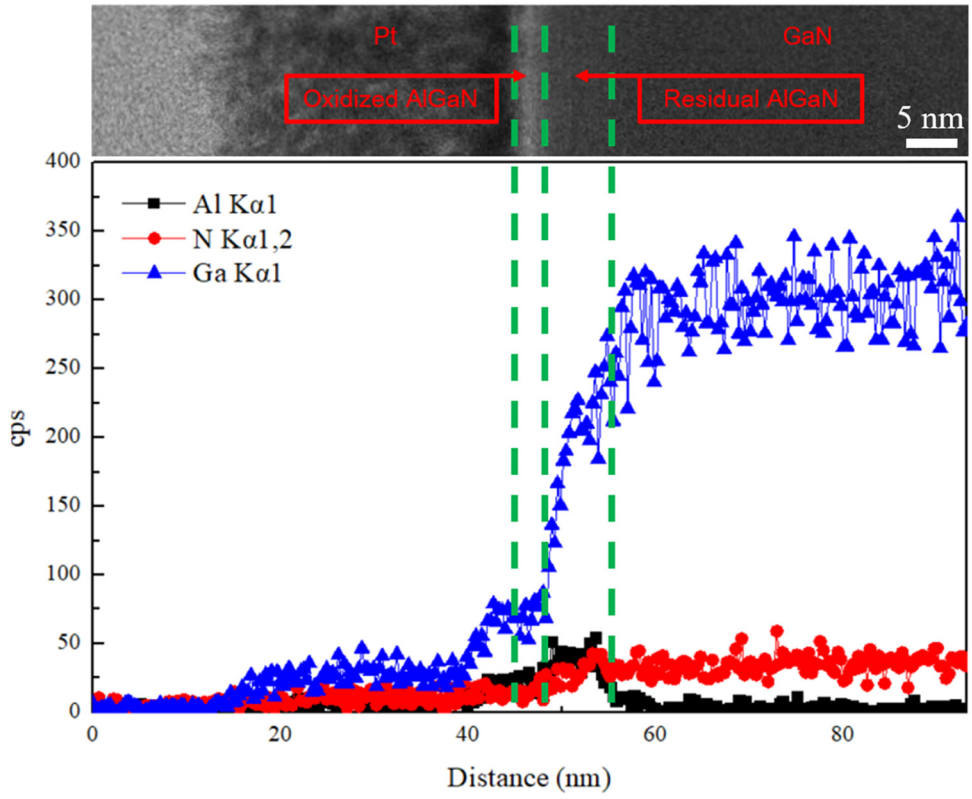

Figure 2. Cross-sectional TEM image of an over-etched substrate (containing oxidized [white]) and residual [light gray] AlGaN) by selective etching between *p*-GaN and AlGaN (top) and element distribution in the over-etched substrate generated from the EDS line scan (bottom).

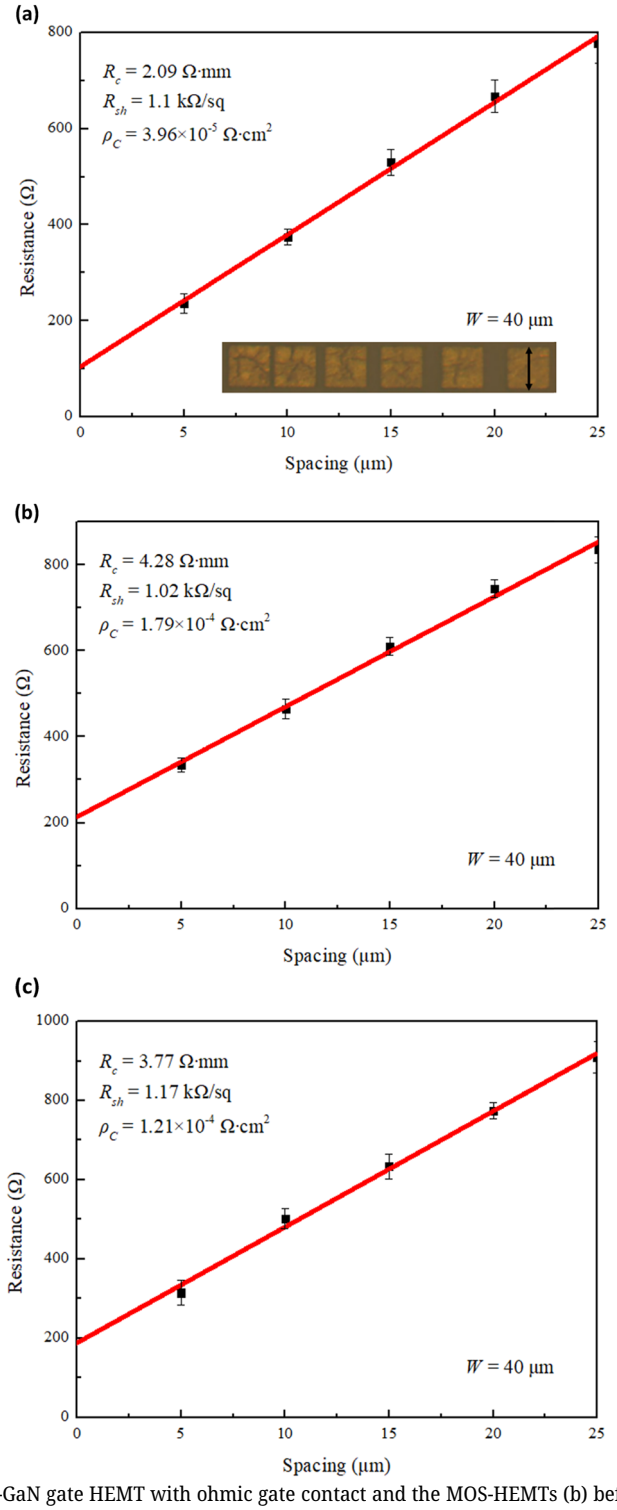

Figure 3. TLM results of (a) the *p*-GaN gate HEMT with ohmic gate contact and the MOS-HEMTs (b) before and (c) after PDA treatment.

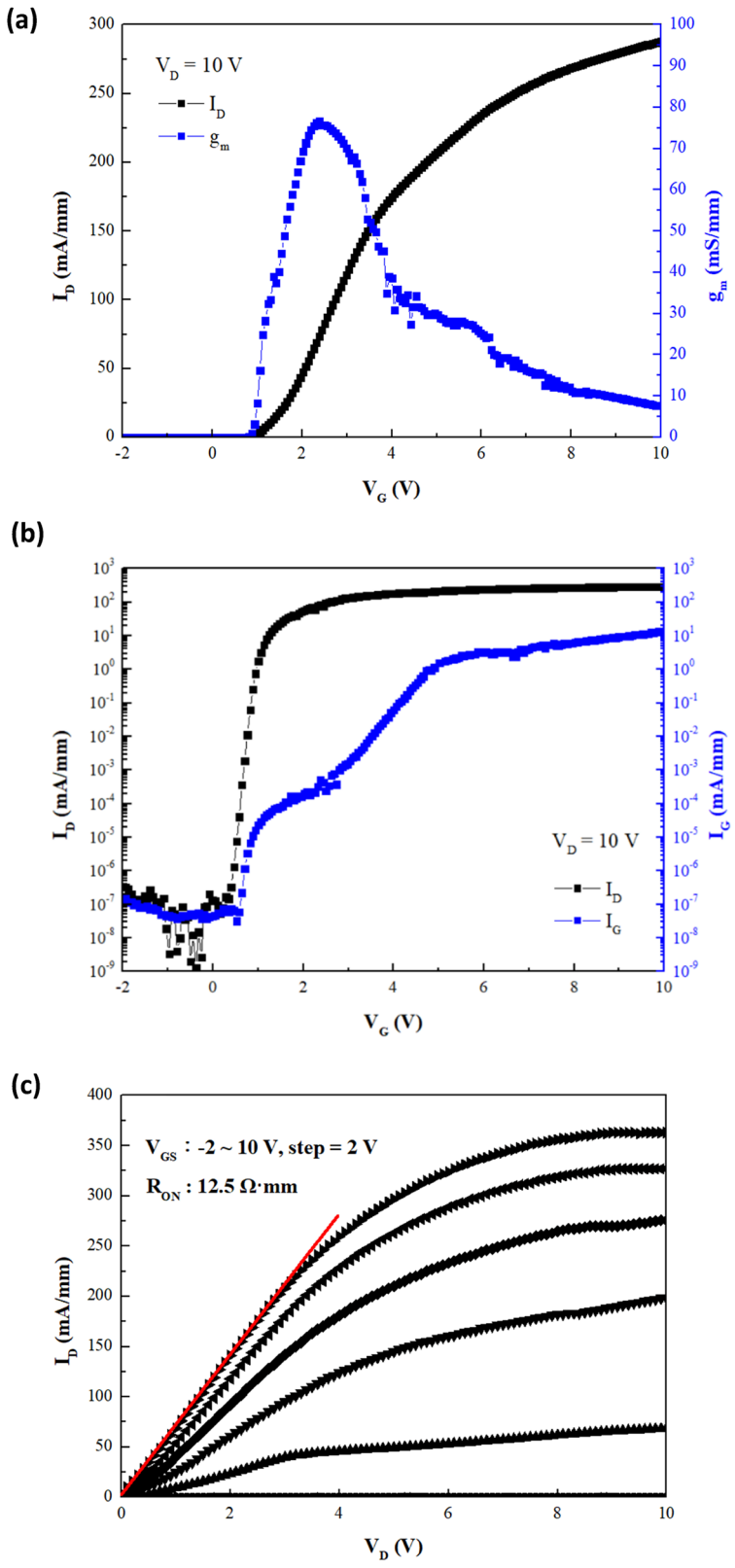

Figure 4. (a) Transfer characteristics of the HEMT with ohmic gate contact in linear scale: the left *Y*-axis shows the drain current, and the right *Y*-axis shows the transconductance. (b) Transfer characteristics in logarithmic scale: the left *Y*-axis shows the drain current, and the right *Y*-axis shows the gate leakage current. (c) Output characteristics of the device under different gate voltages.

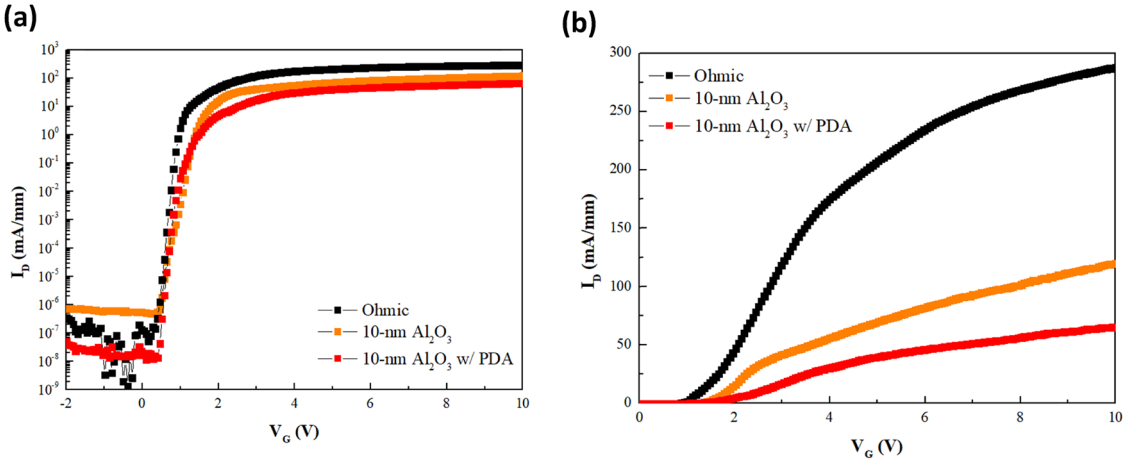

Figure 5. (a) Comparison of transfer characteristics among the three types of HEMTs in a log scale and (b) in a linear scale.

Notably, even without the assistance of an insulating layer structure, a remarkably low gate current of ~10^{-7} mA/mm is achieved. Additionally, Figure 4(b) shows a drain current of ~300 mA/mm, a maximum transconductance ($g_{m,\ max}$) of 76.64 mS/mm, and a field-effect mobility of 684 cm²/V s. Figure 4(c) presents the output characteristics, with a maximum drain current ($I_{D,max}$) of 350 mA/mm and a moderate ON-state resistance (R_{ON}) of 12.5 Ω mm at V_{GS} = 10 V. These superior characteristics are primarily attributed to two key factors: the effective preservation of the high-electron mobility 2DEG conduction channel beneath the remaining *p*-GaN layer during ICP selective etching and the adoption of ohmic contact source/drain metal. TLM measurements demonstrate low sheet resistance and contact resistance, further contributing to the excellent performance.

Figure 5(a) and (b) shows the *I*–*V* characteristics of transfer characteristics among the three types of HEMTs. Without PDA treatment, the MOS-HEMT shows degraded electrical characteristics compared to conventional HEMTs with ohmic gate contact. Notably, the OFF-state current of MOS-HEMT is higher than that of the conventional HEMT with an ohmic gate contact. This is due to the poor interface bonding between oxide and *p*-GaN, which facilitates the easier injection of carriers from the gate into the channel. Additionally, it increases the overall effective oxide thickness (i.e., the distance from the gate to the channel). In other words, the equivalent gate capacitance is reduced, resulting in a decreased amount of electrons that the gate can attract; therefore, the drain current should tend to decrease [24]. As a result, the MOS-HEMT exhibits higher OFF-state current, poorer *SS*, and lower ON-state current. On the contrary, PDA treatment effectively improves the interface characteristics, reducing interface defects and stabilizing the device's performance. This leads to a significant reduction in the OFF current and a notable improvement in the SS, which enhances the gate control over the channel. However, PDA also significantly reduces interface states between oxide and *p*-GaN, which, although beneficial for device stability, has the unintended effect of lowering the available carrier concentration in the channel. Donor-like interface states above the AlGaN layer serve as a primary source of additional carriers in GaN materials, and their reduction decreases the channel's carrier concentration [25–27]. Given the inherently low intrinsic carrier concentration in GaN, this directly results in a further reduction in the ON-state current. Table 1 summarizes the comparison of typical performance parameters among the three types of HEMTs.

We explored the effects of these three structures through the I_G–V_G curve shown in Figure 6. First, it can be observed that the OFF-state current of HEMTs is closely related to their respective reverse gate leakage levels. Additionally, the HEMTs with ohmic gate contacts exhibit two

Parameters	Ohmic gate	MOS-HEMT (w/o PDA)	MOS-HEMT (w/PDA)
V_{th} (V)	0.81	1.15	1.05
SS (mV/dec)	75.61	89.79	71.26
$g_{m,max}$ (mS/mm)	76.64	40.33	18.33
Field effect mobility (cm²/V s)	684	153	71.4
I_{ON}/I_{OFF}	2.17×10^{11}	2.48×10^{8}	5.64×10^{9}

Table 1. Comparison of typical performance parameters among the three types of HEMTs.

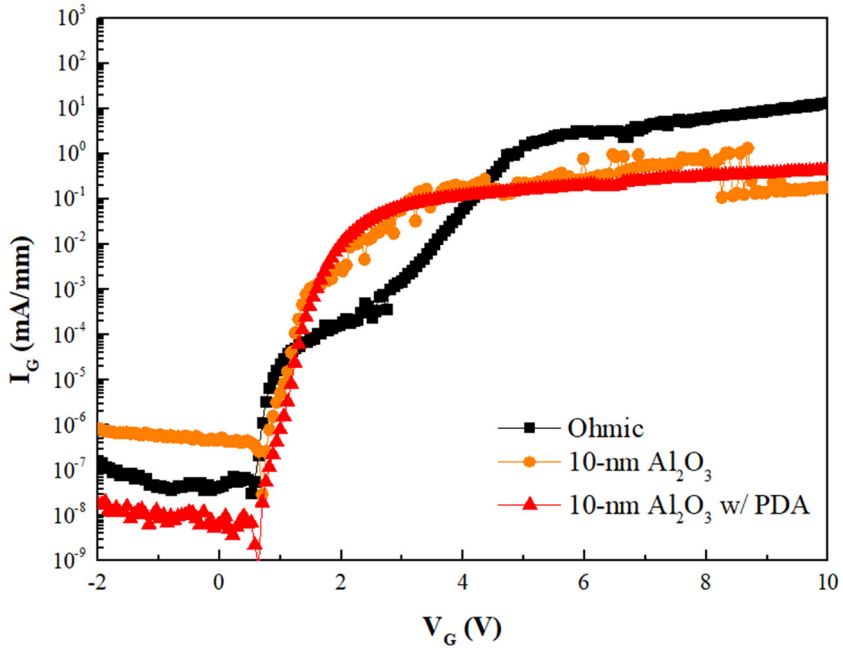

Figure 6. Comparison of I_G–V_G characteristics among the three types of HEMTs.

slope peaks during the turn-on process, which are attributed to the hole injection effect commonly seen in *p*-GaN gate HEMTs [7]. In contrast, this phenomenon is absent in MOS-HEMTs because the gate insulator effectively blocks hole injection. Comparing the ON-state current among the three types, it is evident that the ohmic gate HEMTs experience a significant current increase due to the hole injection effect, which further enhances $I_{D,max}$. On the contrary, MOS-HEMTs

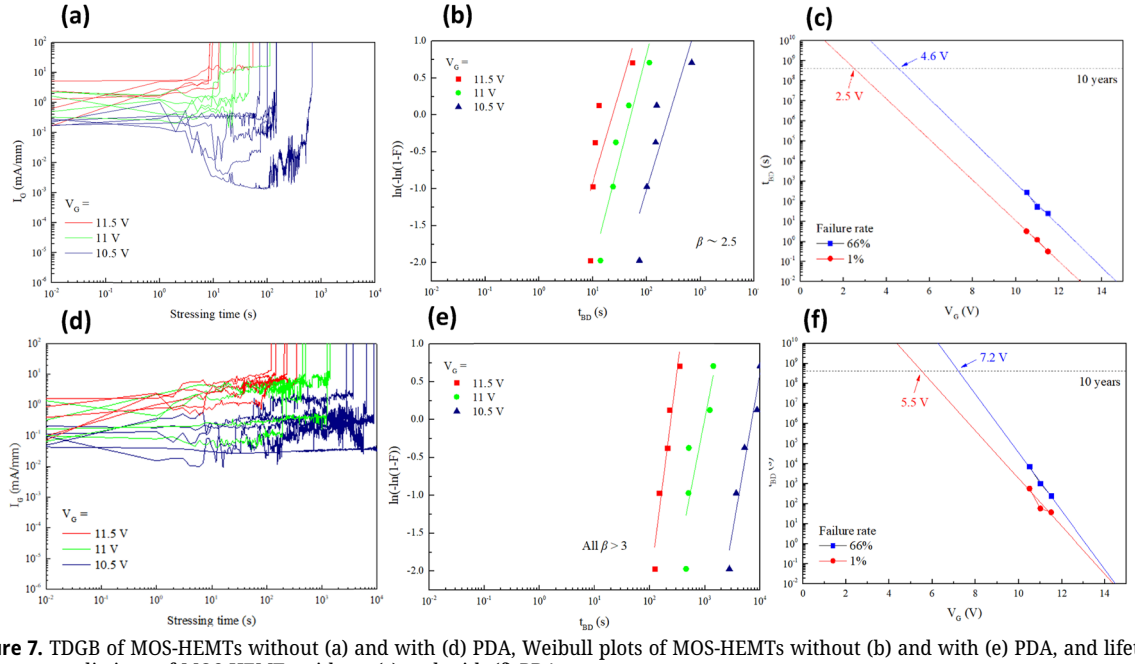

Figure 7. TDGB of MOS-HEMTs without (a) and with (d) PDA, Weibull plots of MOS-HEMTs without (b) and with (e) PDA, and lifetime predictions of MOS-HEMTs without (c) and with (f) PDA.

References	I_{ON}/I_{OFF}	SS (mV/dec)	V_{th} (V)
This work (w/PDA)	10^9	71.26	1.05
[19]	10^5	—	2.40
[28]	10^9	116	0.70
[29]	10^6	—	0.50
[30]	10^9	95	0.30
[31]	10^4	205	0.49
[32]	10^8	—	1.10

Table 2. Comparison of switching performance parameters with other E-mode GaN-based devices.

effectively suppress the sudden rise in forward gate leakage, maintaining a safer current level. Finally, when comparing MOS-HEMTs before and after PDA treatment, MOS-HEMTs with PDA can reduce reverse gate current to an ultra-low leakage level below that of the standard ohmic gate HEMTs. At the same time, they provide a more stable and smoother ON-state current curve.

To further compare the impact of PDA on gate reliability in MOS-HEMTs, we performed TDGB tests. A constant gate voltage was applied while the source and drain electrodes were grounded, as illustrated in Figure 7(a)–(f). The breakdown time (t_{BD}) is defined as the moment when the gate leakage current abruptly increases to 10^2 mA/mm. From Figure 7(a) and (d), it is evident that MOS-HEMTs with PDA improved forward gate leakage characteristics, showing consistently lower leakage current compared to devices without PDA. The Weibull distribution is used to model the TDGB behavior of the devices and is expressed as

$$\ln(-\ln(1 - F(t_{BD}))) = \beta \ln t_{BD} - \beta \ln \eta, \quad (1)$$

where $F(t_{BD})$ represents the probability of failure occurring at a given t_{BD}, β is the shape factor, and η is the scale factor. The Weibull plots in Figure 7(b) and (e), which show $\ln(-\ln(1 - F(t)))$ versus t_{BD}, indicate that the time-to-failure follows a Weibull distribution. Notably, MOS-HEMTs with PDA exhibit a relatively higher shape factor β and a longer lifetime distribution, indicating improved reliability. In the plots of t_{BD} versus V_G (Figure 7(c) and (f)), fitted using an exponential model, the maximum gate voltage that ensures a 10-year lifetime at room temperature with a 1% failure rate is estimated to be 7.2 V for MOS-HEMTs with PDA. This represents a significant improvement in lifetime compared to the poor reliability observed in devices without PDA. These results confirm the enhanced forward gate robustness of *p*-GaN gate MOS-HEMTs after PDA treatment. Table 2 compares the switching performance of our device with other reported E-mode GaN-based devices. Our MOS-HEMT exhibits competitive advantages, particularly in gate leakage suppression and enhancement-mode operation, demonstrating the effectiveness of the Al_2O_3 layer and PDA treatment.

4. Conclusion

In this work, the E-mode *p*-GaN gate HEMT with ohmic gate contact exhibits excellent electrical performance, including a V_{th} of 0.81 V, a field-effect mobility of 684 cm²/V s, a maximum drain current of 363 mA/mm, and a high I_{ON}/I_{OFF}, while maintaining an ON-state resistance comparable to D-mode devices. These superior characteristics result from the effective preservation of the 2DEG channel during ICP selective etching and appropriate ohmic source/drain metal contact. However, without PDA treatment, MOS-HEMTs suffer from poor oxide/*p*-GaN interface bonding and reduced effective oxide capacitance, leading to higher OFF-state current, poorer SS, and lower ON-state current compared to conventional *p*-GaN gate HEMTs with ohmic gate contact. PDA treatment improves interface properties, thereby improving SS and decreasing the OFF-state current. However, it also reduces the interface states of oxide/*p*-GaN, which lowers the available carrier concentration in the channel. Given GaN's inherently low intrinsic carrier concentration, this reduction in surface states further decreases the ON current, resulting in a trade-off between improved stability and reduced ON-state performance. To further validate the effect of PDA, TDGB experiments reveal that MOS-HEMTs with PDA exhibit lower forward gate leakage and longer lifetimes. Weibull analysis confirms improved gate reliability, with a higher shape factor and extended lifetime distribution. Notably, a 10-year lifetime at 7.2 V gate bias is achievable with PDA, highlighting its effectiveness in enhancing gate robustness.

Acknowledgments

This work was supported by the National Science and Technology Council under the contract number NSTC 113-2221-E-992-110.

Funding information

This work was supported by the National Science and Technology Council under contract number NSTC 113-2221-E-992-110.

Author contributions

Tsung-I Liao was responsible for the Writing–original draft, Formal analysis, and Data curation. Sheng-Po Chang contributed to Writing–review & editing, Resources, Methodology, Investigation, Funding acquisition, Data curation, and Conceptualization. Shoou-Jinn Chang contributed to Supervision, Project administration, and Conceptualization. All authors reviewed and approved the final version of the manuscript.

Conflict of interest statement

The authors declare that they have no conflict of interest.

Ethical approval

All authors participated in (a) conception and design or analysis and interpretation of the data; (b) drafting the article or revising it critically for important intellectual content; and (c) approval of the final version.

Consent for publication

All authors have seen and approved the final version of the manuscript being submitted. The manuscript is the original work of the authors. All the authors mutually agree to submit to the journal. It is not being submitted elsewhere.

Data availability statement

All data generated or analyzed during this study are included in this published article.

References

[1] He, J., Cheng, W.C., Wang, Q., Cheng, K., Yu, H., Chai, Y., Recent advances in GaN-based power HEMT devices, Adv. Electron. Mater., 2021, 7: 2001045

[2] Dreyer, C.E., Janotti, A., Van de Walle, C.G., Effects of strain on the electron effective mass in GaN and AlN, Appl. Phys. Lett., 2013, 102: 142105

[3] Roccaforte, F., Fiorenza, P., Greco, G., Nigro, R.L., Giannazzo, F., Iucolano, F., et al., Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices, Microelectron. Eng., 2018, 187: 66

[4] Lin, Y.C., Chang, C.H., Li, F.M., Hsu, L.H., Chang, E.Y., Evaluation of TiN/Cu gate metal scheme for AlGaN/GaN high-electron-mobility transistor application, Appl. Phys. Express, 2013, 6: 091003

[5] Chen, K.J., Häberlen, O., Lidow, A., Lin Tsai, C., Ueda, T., Uemoto, Y., et al., GaN-on-Si power technology: Devices and applications, IEEE Trans. Electron. Devices, 2017, 64: 779

[6] Meneghini, M., Hilt, O., Wuerfl, J., Meneghesso, G., Technology and reliability of normally-off GaN HEMTs with p-type gate, Energies, 2017, 10: 153

[7] Greco, G., Iucolano, F., Roccaforte, F., Review of technology for normally-off HEMTs with p-GaN gate, Mater. Sci. Semicond. Process., 2018, 78: 96

[8] Qi, Y., Zhu, Y., Zhang, J., Lin, X., Cheng, K., Jiang, L., et al., Evaluation of LPCVD SiN x gate dielectric reliability by TDDB measurement in Si-substrate-based AlGaN/GaN MIS-HEMT, IEEE Trans. Electron. Devices, 2018, 65: 1759

[9] Wu, T.L., Marcon, D., De Jaeger, B., Van Hove, M., Bakeroot, B., Stoffels, S., et al., Time dependent dielectric breakdown (TDDB) evaluation of PE-ALD SiN gate dielectrics on AlGaN/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs, In 2015 IEEE International Reliability Physics Symposium, 2015, p. 6C. 4.1

[10] Vandendaele, W., Leurquin, C., Lavieville, R., Jaud, M.A., Viey, A.G., Gwoziecki, R., et al., Reliability of GaN MOSc-HEMTs: From TDDB to threshold voltage instabilities, In 2023 IEEE International Reliability Physics Symposium (IRPS), 2023, p. 1

[11] Chen, J., Hua, M., Wei, J., He, J., Wang, C., Zheng, Z., et al., OFF-state drain-voltage-stress-induced V TH instability in Schottky-type p-GaN gate HEMTs, IEEE J. Emerg. Sel. Top. Power Electron., 2020, 9: 3686

[12] Sarkar, A., Haddara, Y.M., Modeling of forward gate leakage current for normally off pGaN/AlGaN/GaN HEMTs, Solid-State Electron., 2022, 196: 108420

[13] Huang, K.N., Lin, Y.C., Wu, C.Y., Lee, J.H., Hsu, C.C., Yao, J.N., et al., Study of p-GaN gate MOS-HEMT with Al_2O_3 insulator for high-power applications, J. Electron. Mater., 2023, 52: 2865

[14] Liu, Z.H., Ng, G.I., Arulkumaran, S., Maung, Y.K.T., Teo, K.L., Foo, S.C., et al., High microwave-noise performance of AlGaN/GaN MISHEMTs on Silicon With Al_2O_3 Gate insulator grown by ALD, IEEE Electron. Device Lett., 2009, 31: 96

[15] Azam, F., Tanneeru, A., Lee, B., Misra, V., Engineering a unified dielectric solution for AlGaN/GaN MOS-

HFET gate and access regions, IEEE Trans. Electron. Devices, 2020, 67: 881

[16] Rrustemi, B., Piotrowicz, C., Jaud, M.A., Triozon, F., Vandendaele, W., Mohamad, B., et al., Effect of doping on Al_2O_3/GaN MOS capacitance, Solid-State Electron., 2022, 194, 108356

[17] Glaser, C.E., Binder, A.T., Yates, L., Allerman, A.A., Feezell, D.F., Kaplar, R.J., Analysis of ALD dielectric leakage in bulk GaN MOS devices, In 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2021, p. 268

[18] Lükens, G., Hahn, H., Kalisch, H., Vescan, A., Self-aligned process for selectively etched p-GaN-gated AlGaN/GaN-on-Si HFETs, IEEE Trans. Electron. Devices, 2018, 65: 3732

[19] Baby, R., Reshma, K., Chandrasekar, H., Muralidharan, R., Raghavan, S., Nath, D.N., Study of TaN-gated p-GaN E-mode HEMT, IEEE Trans. Electron. Devices, 2023, 70: 1607

[20] Dai, X., Jiang, Q., Huang, S., Feng, C., Ji, Z., Gao, X., et al., Island-ohmic-PGaN gate HEMT: Toward steep subthreshold swing and enhanced threshold stability, IEEE Electron. Device Lett., 2024, 45: 988

[21] Millesimo, M., Fiegna, C., Posthuma, N., Borga, M., Bakeroot, B., Decoutere, S., et al., High-temperature time-dependent gate breakdown of p-GaN HEMTs, IEEE Trans. Electron. Devices, 2021, 68: 5701

[22] Taube, A., Kamiński, M., Ekielski, M., Kruszka, R., Jankowska-Śliwińska, J., Michałowski, P.P., et al., Selective etching of p-GaN over Al0. 25Ga0. 75N in Cl_2/Ar/O_2 ICP plasma for fabrication of normally-off GaN HEMTs, Mater. Sci. Semicond. Process., 2021, 122: 105450

[23] Krishna, A., Investigation of p-Type GaN/AlGaN superlattices: defining a pathway towards low sheet resistance for p-channel III-nitride devices, In University of California, Santa Barbara, 2022

[24] Yue, Y.Z., Hao, Y., Zhang, J.C., AlGaN/GaN MOS-HEMT with stack gate HfO2/Al2O3 structure grown by atomic layer deposition, In 2008 IEEE Compound Semiconductor Integrated Circuits Symposium, 2008, p. 1

[25] Ibbetson, J.P., Fini, P.T., Ness, K.D., DenBaars, S.P., Speck, J.S., Mishra, U.K., Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors, Appl. Phys. Lett., 2000, 77: 250

[26] Stockman, A., Canato, E., Tajalli, A., Meneghini, M., Meneghesso, G., Zanoni, E., et al., On the origin of the leakage current in p-gate AlGaN/GaN HEMTs, In 2018 IEEE international reliability physics symposium (IRPS), 2018, p. 4B. 5

[27] Ahmed, N., Dutta, G., Physics-based models of 2DEG density and gate capacitance for p-GaN/AlGaN/GaN heterostructure, IEEE Trans. Electron. Devices, 2024, 71, 4093

[28] Liu, A.C., Tu, P.T., Chen, H.C., Lai, Y.Y., Yeh, P.C., Kuo, H.C., Improving performance and breakdown voltage in normally-off GaN recessed gate MIS-HEMTs using atomic layer etching and gate field plate for high-power device applications, Micromachines, 2023, 14, 1582

[29] Liu, W., Yu, G., Zhou, J., Yu, Z., Wei, X., Tang, W., et al., Implementation of recessed gate normally off GaN metal–insulator–semiconductor high electron mobility transistors by electrodeless photoelectrochemical etching, ACS Appl. Electron. Mater., 2022, 4: 897

[30] Zhu, M., Ma, J., Nela, L., Erine, C., Matioli, E., High-voltage normally-off recessed tri-gate GaN power MOSFETs with low on-resistance, IEEE Electron. Device Lett., 2019, 40: 1289

[31] Chen, Y.H., Ohori, D., Aslam, M., Lee, Y.J., Li, Y., Samukawa, S., Enhancing the performance of E-mode AlGaN/GaN HEMTs with recessed gates through low-damage neutral beam etching and post-metallization annealing, IEEE Open. J. Nanotechnol., 2023, 4: 150

[32] Greco, G., Iucolano, F., Di Franco, S., Bongiorno, C., Patti, A., Roccaforte, F., Effects of annealing treatments on the properties of Al/Ti/p-GaN interfaces for normally OFF p-GaN HEMTs, IEEE Trans. Electron. Devices, 2016, 63: 2735