

A COMPREHENSIVE STUDY ON THE RELIABILITY OF GaN TRANSISTORS UNDER HIGH HUMIDITY, HIGH TEMPERATURE, AND REVERSE BIAS CONDITIONS

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The paper presents a detailed study of the reliability of GaN high-electron mobility transistors (HEMTs) under high-humidity, high-temperature, and reverse-bias (H³TRB) conditions. Despite growing interest, the number of studies addressing the reliability of GaN HEMTs remains limited. This work differs from previously published studies in its comprehensive approach; for example, the H³TRB test is conducted beyond standard specifications (i.e., at 95 % relative humidity) and at two different reverse-bias voltages (the maximum rated value and 80 % of that value). The drain–source leakage current was monitored during a 1000-h H³TRB test conducted on 11 GaN HEMTs in PowerFLAT 5×6 packages at a temperature of 85 °C. Key electrical characteristics were also measured before the stress test and at multiple time points after its completion (1 h, and for selected parameters also after 168 h) to assess the level of degradation and to investigate possible recovery phenomena. The results indicate that GaN HEMTs in PowerFLAT 5×6 packages exhibit high reliability under H³TRB stress for durations of at least 1000 h, with no catastrophic failures and no significant degradation in electrical characteristics, even under conditions of 95 % relative humidity and maximum drain–source voltage.

Keywords: *Aging, GaN transistors, humidity, leakage currents, reliability, temperature.*

1. INTRODUCTION

Modern electrical equipment (e.g., electric vehicle chargers) relies heavily on power electronic converters based on power semiconductor devices, primarily transistors. Driven by the ongoing demand for higher efficiency and higher power density, gallium nitride (GaN) high electron mobility transistors (HEMTs) have gained significant attention in recent years [1]. Compared to silicon carbide (SiC) field-effect transistors (FETs) and insulated gate bipolar transistors (IGBTs), GaN HEMTs typically operate at lower voltage and power levels [2]. However, due to their extremely fast switching speeds, GaN HEMTs can operate in the MHz range and achieve higher efficiency at high switching frequencies (typically in the hundreds of kHz to MHz range), where switching losses in Si or SiC FETs become significant, while IGBTs are not applicable at such frequencies [3].

In this century, the reliability of power electronic converters has become increasingly important [4]. When electrical equipment is operated outdoors (e.g., electric vehicle charging stations) or in industrial environments, it is often exposed to harsh ambient conditions, which can accelerate the aging of power semiconductor devices, particularly transistors, and other electronic components. Consequently, electrical equipment reliability may be compromised.

To evaluate and ensure reliability under such conditions, transistors are tested in climate chambers that emulate harsh environments. These tests, known as high-humidity, high-temperature reverse bias (H³TRB) tests, subject devices to elevated stress levels. The conditions inside the climate chambers are intentionally more severe than those encountered in real operation in order to accelerate aging processes and sig-

nificantly reduce testing time [5].

According to IEC 60749-5:2023 [6] and JEDEC JESD22-A101 [7], H³TRB tests are typically conducted at 85 °C and 85 % relative humidity (RH) for 1000 h, with controlled tolerances. Obviously, the applied reverse bias voltage (drain–source voltage with gate shorted to source) must not exceed the device’s maximum rated value and is defined by the manufacturer or test specification. In practice, it is often selected to be equal to 80 % of the maximum allowable drain–source voltage [5], [8]–[10].

According to JEDEC, semiconductor device degradation is assessed via changes in electrical parameters, and failure is defined by exceeding specified limits [7]. In practice, leakage current is commonly monitored during H³TRB testing, as it provides a highly sensitive key indicator of degradation of transistors under reverse bias [11]–[13].

Although a substantial body of research [8], [9], [11]–[13] exists on reliability testing and failure analysis of Si and SiC FETs, as well as IGBTs – often implemented as gel-coated modules – under high-humidity, high-temperature conditions, studies focusing on GaN HEMTs in such environments remain limited. Due to differences in semiconductor technology, packaging, and typical application formats (i.e., discrete transistors rather than modules), the impact of humidity and temperature on the reliability of GaN HEMTs, as well as the underlying failure mechanisms, may differ significantly from those observed in Si and SiC transistors. Therefore, further research in this area is necessary.

Despite growing interest, the number of studies [5], [14], [15] on the reliability of GaN HEMTs remains limited. Existing

works on H³TRB testing typically focus on standard conditions (85 °C, 85 % RH, and 80 % of the maximum allowable reverse bias voltage). However, it is important to investigate device reliability under more severe conditions, such as higher RH (e.g., 95 %) and operation at the maximum allowable reverse bias voltage.

Moreover, several important aspects are often not addressed. For example, the static characteristics of GaN HEMTs are usually measured only before and immediately after exposure to H³TRB stress. Evaluating these characteristics both immediately after the test and after a longer recovery period (e.g., one week) would provide insight into possible recovery phenomena.

In addition, many studies conduct tests

at only a single reverse bias voltage, which limits the understanding of how the magnitude of the reverse bias voltage influences the reliability of GaN HEMTs.

This paper aims to address the identified research gap. In contrast to previous studies (e.g., [5], [14], [15]), a more comprehensive investigation of the impact of high temperature and high humidity on the reliability of GaN HEMTs is presented. The study extends beyond standard test conditions and includes a more detailed analysis of the main static characteristics of GaN HEMTs under two different reverse bias voltage levels. The scope and distinguishing features of the proposed study are summarised in Table 1 to facilitate comparison with existing work.

Table 1. Comparison of Studies on Reliability of GaN HEMTs

	RH and reverse bias beyond standards?	H3TRB test conducted at different reverse bias?	Study of recovery effect after test?
[5]	No (85 % RH, 80 % max reverse bias)	No, only at 80 % max reverse bias	No
[14]			
[15]			
This paper	Yes (95 % RH, max reverse bias)	Yes, at 80 % and 100 % max reverse bias	Yes

2. EXPERIMENTAL SETUP

2.1. Description of the Test

The H³TRB test was conducted on 11 GaN transistors (SGT120R65AL) from STMicroelectronics (STM), packaged in PowerFlat 5×6. The total stress duration was 1000 h. The devices under test (DUTs) were divided into two groups: Group A (8 devices) and Group B (3 devices).

For Group A, a reverse bias voltage (V_{DS}) of 650V was applied, corresponding to the

maximum allowable drain-source voltage of SGT120R65AL GaN transistor. For Group B transistors, the applied V_{DS} was set to 80 % of maximum rating, i.e., 520 V. The environmental conditions were identical for all DUTs, with a temperature T of 85 °C and RH of 95 % maintained inside the climate chamber.

The following measurements were performed:

1. **Pre-test measurements:** Before placing the printed circuit board (PCB) inside the climate chamber, the main static characteristics of the GaN HEMTs (drain–source on-resistance $R_{DS(on)}$, drain-source leakage current I_{DSS} , gate-source leakage current I_{GSS} and gate-source threshold voltage $V_{GS(th)}$) were measured at room temperature (25 °C).
2. **Monitoring:** During the 1000 h H³TRB test, I_{DSS} was periodically (every 1 s) measured for all DUTs.
3. **Post-test measurements (short-term):** After removal of the PCB from the climate chamber, the main static characteristics were measured again at room temperature approximately 1 h after the end of the test.
4. **Post-test measurements (long-term):**

$R_{DS(on)}$ and $V_{GS(th)}$ were re-measured at room temperature 168 h after completion of the H³TRB test.

To prevent accelerated degradation of the test PCB and DUTs, as well as to ensure stable leakage current measurements, both JEDEC and IEC recommend avoiding significant condensation on the surfaces of test boards during H³TRB testing. Accordingly, the V_{DS} should be applied only after the temperature inside the climate chamber has reached and stabilized at the target value [6], [7]. Subsequently, the RH should be increased gradually once thermal stability is achieved.

In this study, these JEDEC and IEC recommendations were followed to minimise condensation effects during the H³TRB test.

2.2. Description of the Test Board

A dedicated PCB was designed and fabricated for H³TRB aging tests of 11 SGT120R65AL GaN transistors. A photograph of the test PCB with the soldered DUTs is shown in Fig. 1.

To protect the PCB from moisture-

induced degradation (e.g., electrochemical corrosion of metal traces and electrochemical migration), a protective epoxy resin coating was applied. The DUT packages were intentionally left uncoated to ensure direct exposure to the test environment.

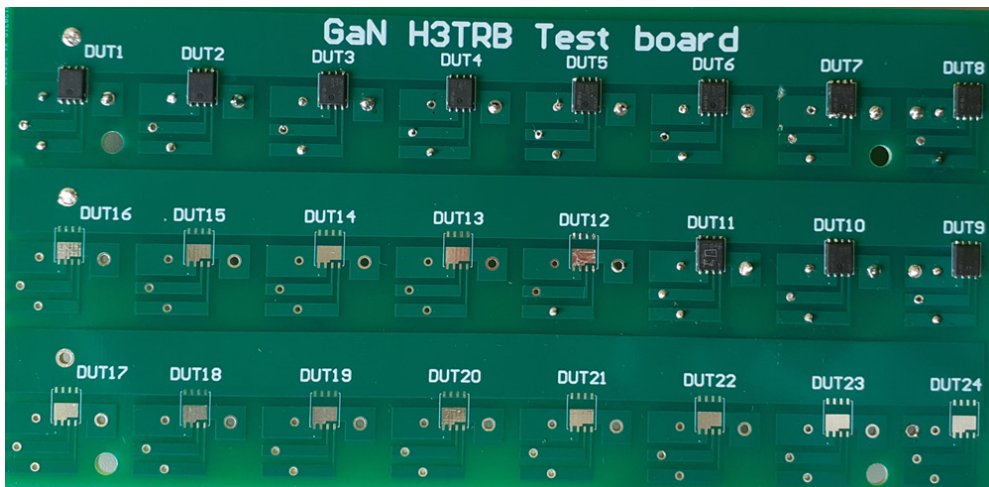


Fig. 1. An image of GaN H³TRB test PCB with soldered 11 DUTs.

Furthermore, to reduce the risk of humidity-related degradation, surface con-

tamination (e.g., flux residues) was removed after soldering using isopropyl alcohol.

2.3. Description of the Experimental Setup

For H³TRB test, a climate chamber Binder KMF 240 was used. The chamber can maintain conditions (temperature and RH level) mentioned previously. Low-

grade distilled water (5 μ S/cm) was used for vaporization in the chamber. A photo of the test board inside the chamber is shown in Fig. 2.



Fig. 2. Image of the test board inside the chamber.

Additionally, Fig. 3 presents a photo of the experimental setup.

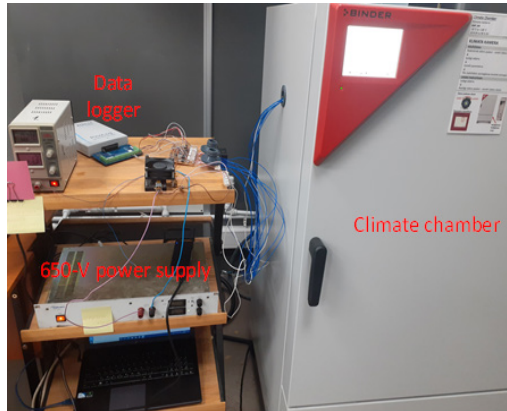


Fig. 3. Image of the experimental setup.

Axillary boards with fuses, leakage-current-sensing resistors and connectors were also used in the test. The schematic diagram of the test setup is shown in Fig. 4.

Voltage drops across resistors $R1-R11$ are proportional to corresponding I_{DSS} of GaN transistors. If the drain-source leakage currents become large, then fuses Fx will dis-

connect failed DUTs from the main circuit. Transient voltage suppression diodes are used to prevent inputs of voltage measuring instruments (such as data loggers) from damaging due to overvoltage at R_x . To get different voltages from 650 Vdc source,

simple resistive voltage divider ($Rd1$, $Rd2$) is used. The divider is used instead of separate regulated DC voltage source because drain-source leakage currents are very low and are much lower than the currents flowing through $Rd2$.

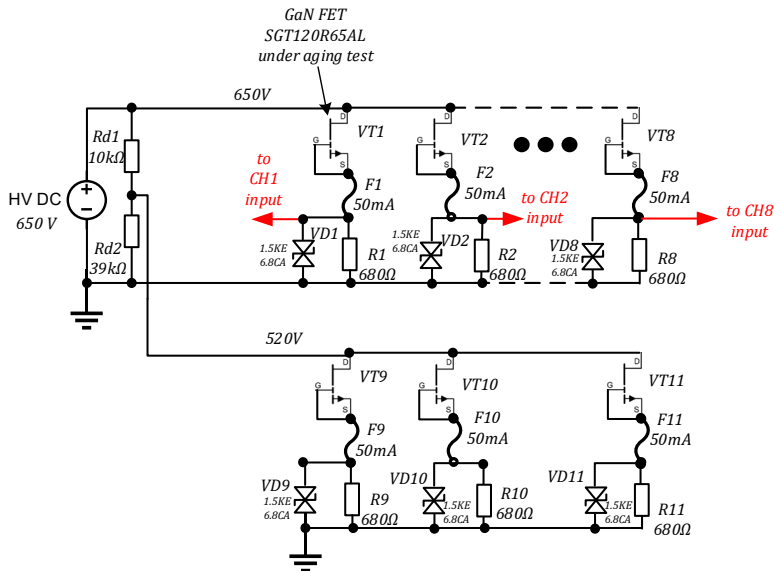


Fig. 4. A schematic diagram of the experimental setup.

To measure I_{DSS} , the voltage drops across the current-sensing resistors were divided by their respective resistance values. To measure the voltages across the current-sensing resistors connected in series with DUT1–DUT8, a high-resolution (20-bits) 8-channel data logger ADC-20 from

Pico Technology was used. To measure the voltages across the current-sensing resistors connected in series with DUT9–DUT11, a standard digital multimeter GDM-451 from GW Instek (with resolution of 0.1 mV) was used.

3. EXPERIMENTAL RESULTS AND DISCUSSION

During the test, the recommendations of IEC and JEDEC for minimising condensation on the surface of the test board were followed. V_{DS} was applied only after both temperature and RH reached their target values and stabilized, which occurred approximately 1.5 h after the climate cham-

ber was switched on. The main experimental results are presented in Figs. 5-10.

As shown in Fig. 5, initially the I_{DSS} of the Group A DUTs is on the order of several μA . It then decreases relatively rapidly within approximately 40 h, followed by a long-term gradual increase observed for all DUTs.

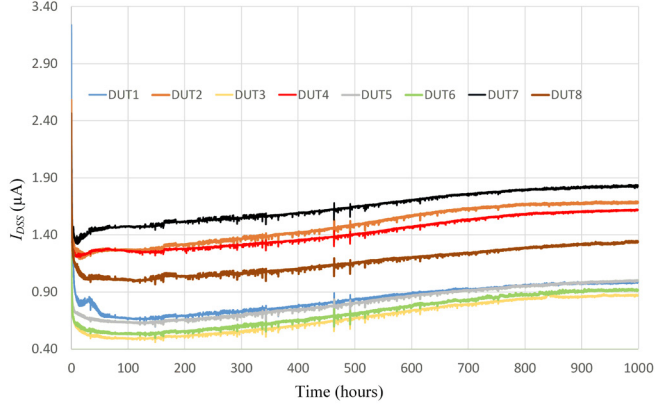


Fig. 5. I_{DSS} as a function of time for DUTs No. 1–8 (from Group A) during the H³TRB test. $V_{DS}=650$ V, $T=85$ °C and RH is 95 %.

No catastrophic failure was observed after 1000h of the H³TRB test. During the test, all Group A DUTs exhibited an increase in I_{DSS} of less than 70% after 1000 h compared to their minimum I_{DSS} values.

Similar trends can be observed for DUTs

No. 10 and 11 in Group B (see Fig. 6). For DUT 9, the apparent constancy of I_{DSS} during the first 500 h is most likely attributable to the insufficient resolution of the measurement instrument used for leakage current measurement of Group B DUTs.

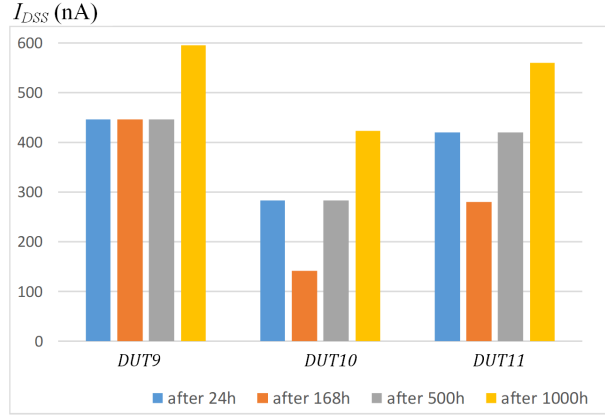


Fig. 6. I_{DSS} readouts of DUTs No. 9–11 (from Group B) during 1000h of H³TRB test. $V_{DS}=520$ V, $T=85$ °C and RH is 95 %. Note: due to the limited resolution (140nA) of the instrument used small changes in I_{DSS} cannot be detected.

From the results presented in Figs. 5 and 6, an important conclusion can be drawn: a higher V_{DS} leads to a higher I_{DSS} for all DUTs. However, the relative increase of I_{DSS} from 24 h to the end of the test is not significantly dependent on V_{DS} within the investigated range of 80 % to 100 % of the maximum allowable drain–source voltage, as similar trends are observed for DUTs in

both groups. In fact, such a time-dependent variation of I_{DSS} was not observed in [5], [14], and [15], most likely due to the use of low-resolution data loggers and/or the application of protective coatings not only on the PCB but also on the DUTs.

The observed time-dependent evolution of I_{DSS} during the H³TRB test is noteworthy. The initially high leakage current can be

explained by moisture-driven surface conduction across the DUTs and partially along the PCB, likely caused by moderate condensation during the early stage of the test. The subsequent rapid decrease in I_{DSS} can be associated with the reduction of surface moisture (condensation) during the initial hours of the test, combined with field-driven charge redistribution, while the subsequent gradual increase may indicate progressive electrochemical and defect-driven degradation of GaN HEMTs under H³TRB stress.

A comparison of the static characteristics measured before and after the H³TRB test at

room temperature is presented in Figs. 7–10. No significant change in the static characteristics is observed after the H³TRB test. Only slight to moderate changes are detected.

I_{GSS} changed slightly (<10 %), both positive and negative shifts are observed (Fig. 7).

I_{DSS} shows small to moderate changes (<30 %), with both positive and negative shifts, while the mean value remains approximately constant (Fig. 8). It is interesting to observe that I_{DSS} increased relative to its minimum value for all DUTs during the H³TRB test.

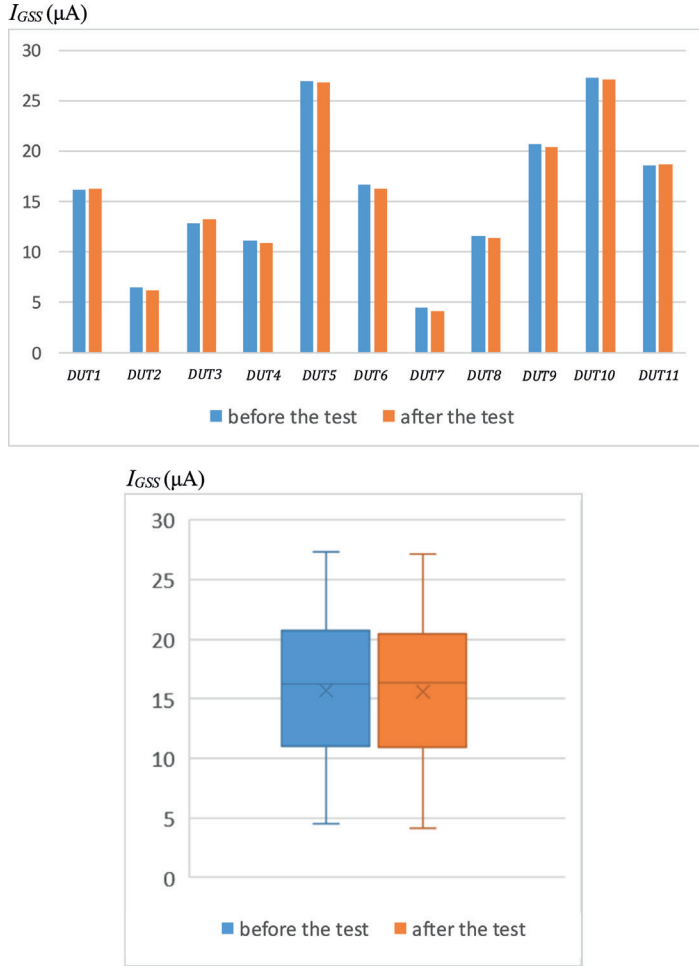


Fig. 7. I_{GSS} (at $V_{GS}=6V$) of all DUTs measured before the test and after the end of the test: bar chart (top) and statistic chart (bottom). In both cases, the test PCB was outside the chamber. Conditions: temperature 25 ± 0.5 °C and RH= 35 ± 5 %.

However, measurements of I_{DSS} performed before and after the test under room temperature and normal RH conditions revealed mixed behaviour across the devices: for three DUTs I_{DSS} remained unchanged, for five DUTs it increased moderately, and for three DUTs it decreased (Fig. 8). This observation suggests that the gradual increase in I_{DSS} for all DUTs may not be solely attributable to progressive electrochemical and defect-driven degrada-

tion of GaN HEMTs under H³TRB stress, as previously assumed. The observed increase in I_{DSS} under H³TRB stress for DUT1, DUT3, DUT5, DUT6, DUT8 and DUT9 is reversible, as I_{DSS} values return to baseline after removal from the climate chamber. This indicates that the dominant mechanism explaining a gradual increase in I_{DSS} is moisture-assisted surface conduction and ionic effects rather than permanent device degradation.

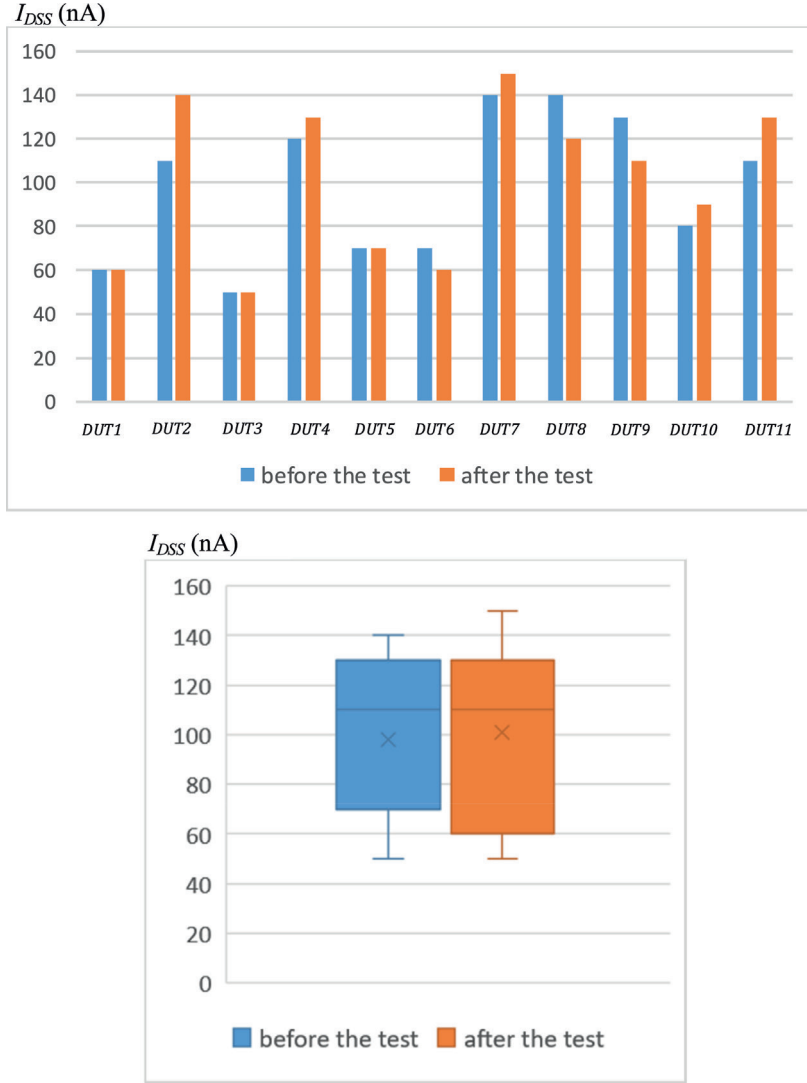


Fig. 8. I_{DSS} (at $V_{DS}=650V$) of all DUTs measured before the test and after the end of the test: bar chart (top) and statistic chart (bottom). In both cases, the test PCB was outside the chamber. Conditions: temperature 25 ± 0.5 °C and RH= 35 ± 5 %.

$R_{DS(on)}$ exhibited only small changes ($\leq 5.6\%$), while $V_{GS(th)}$ showed small to moderate changes ($< 20\%$), with both positive and negative shifts (Fig.9 and Fig.10). Most DUTs exhibited a slight decrease in $R_{DS(on)}$ and a slight-to-moderate decrease in $V_{GS(th)}$. It is interesting to observe a correlation between the change in the characteristics: for DUTs with increased $R_{DS(on)}$, $V_{GS(th)}$ also increased, and vice versa. $R_{DS(on)}$ and $V_{GS(th)}$ measured 1 h after the end of the H³TRB test, increased only for three DUTs (DUT2, DUT4, and DUT7). Notably, these devices also exhibited the highest I_{DSS} during the

H³TRB test, the lowest I_{GSS} both before and after the test, and the highest post-test I_{DSS} .

It is noteworthy that both $R_{DS(on)}$ and $V_{GS(th)}$, measured 168 hours after the H³TRB test, were noticeably closer to their initial (pre-stress) values than those measured just 1 hour after the test completion. This recovery behaviour can likely be attributed to the gradual desorption or redistribution of moisture, which affects charge trapping and related conduction mechanisms.

Values of the static characteristics of the GaN HEMTs remain within the limits stated in the datasheet [16].

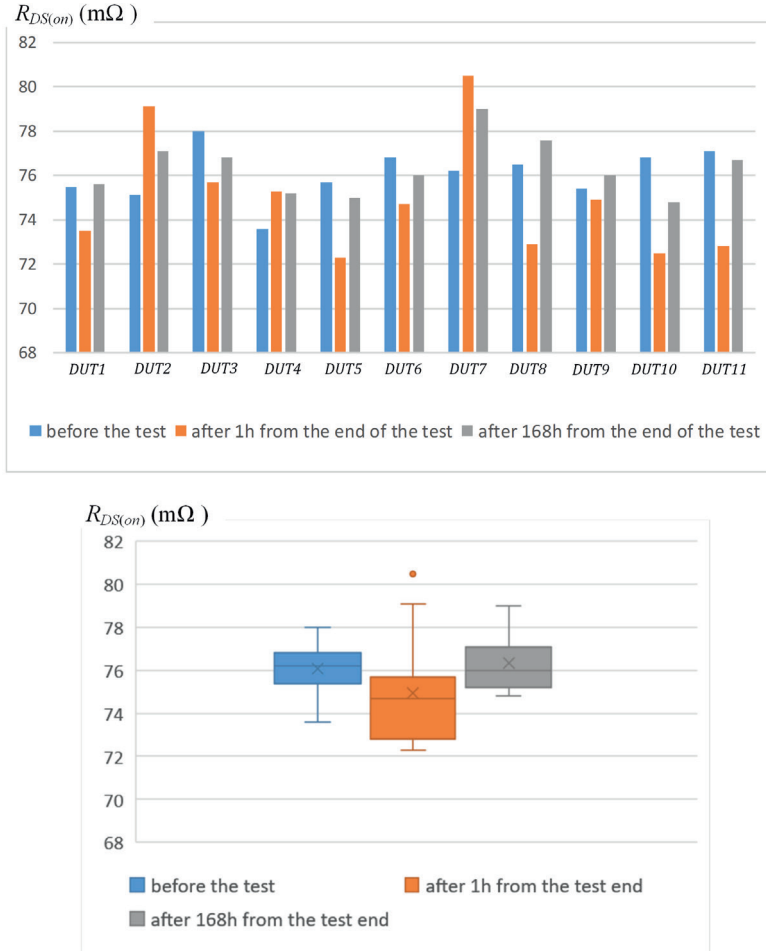


Fig. 9. $R_{DS(on)}$ (at $V_{GS}=6$ V and $I_D=1$ A) of all DUTs measured before the test, after 1h from the end of the test and after 168h from the end of the test: bar chart (top) and statistic chart (bottom). In all cases, the test PCB was outside the chamber. Conditions: $T=25\pm 0.5$ °C and $RH=35\pm 5$ %.

The analysis revealed no clear relationship between the applied V_{DS} during the test (within the investigated range of 80% to 100% of the maximum allowable drain–source voltage) and the post-test

changes in electrical characteristics, since the absolute changes between the pre-test and post-test mean values were similar for all evaluated parameters in both DUT groups.

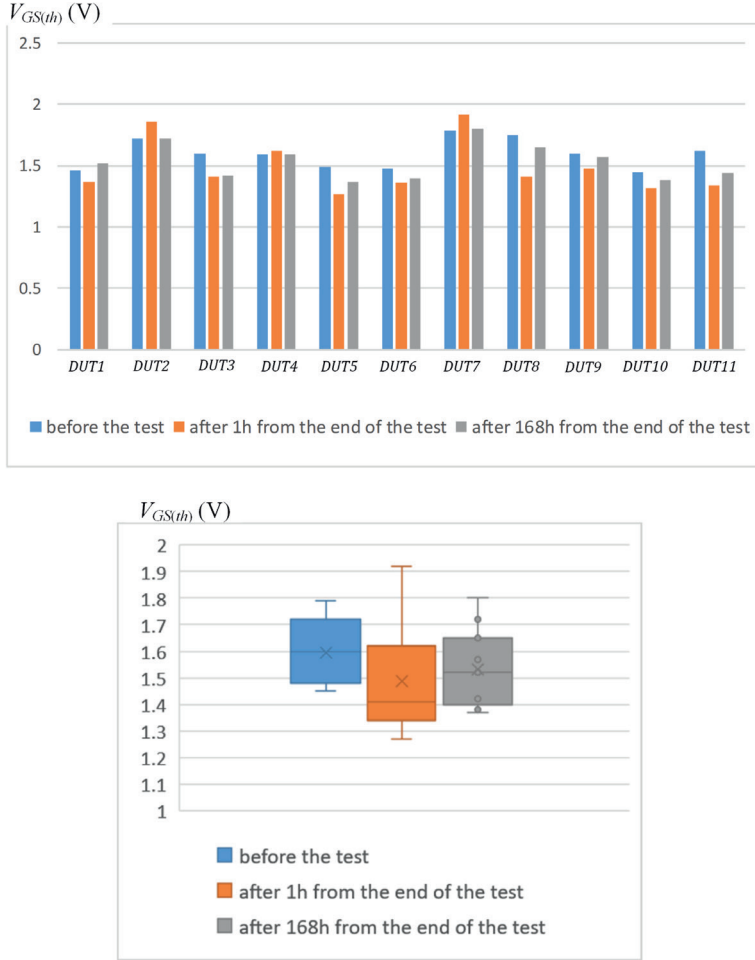


Fig. 10. $V_{GS(th)}$ (at $V_{DS}=0.1$ V and $I_D=12$ mA) of all DUTs measured before the test, after 1h from the end of the test and after 168h from the end of the test: bar chart (top) and statistic chart (bottom). In all cases, the test PCB was outside the chamber. Conditions: $T=25\pm0.5$ °C and $RH=35\pm5$ %.

4. CONCLUSION

GaN HEMTs in PowerFLAT 5×6 packages exhibit high reliability under H³TRB stress for durations of at least 1000 hours, showing no catastrophic failures and

no significant degradation in electrical characteristics, even under conditions of 95 % RH and maximum drain–source voltage, provided that condensation is minimised and

test board cleanliness is maintained.

No significant changes in the static characteristics of the GaN HEMTs were observed after the H³TRB test. Only slight to moderate variations (<30 %) were detected, with both positive and negative shifts. No apparent relationship was observed between the applied drain–source voltage during testing (within the investigated range of 80% to 100% of the maximum allowable drain–source voltage) and the post-test changes in electrical characteristics relative to their pre-test values, as the absolute changes in the group mean values for each parameter were comparable between the two DUT groups.

The most unaffected electrical parameter is gate-source leakage current, as results show only slight changes (<10 %) after the test.

Even though the drain–source leak-

age current increased for all eleven GaN HEMTs during the H³TRB test, the degradation was reversible in a substantial number of devices (six), as the I_{DSS} values returned to their initial values after removal from the climate chamber. This suggests that the dominant mechanism behind the gradual increase in I_{DSS} during the test is moisture-assisted surface conduction and ionic effects, rather than permanent device degradation.

Even though the drain–source on-resistance and gate–source threshold voltage change after the H³TRB test, a recovery phenomenon is observed, as their values measured 168 hours after test completion are noticeably closer to their initial values than those measured 1 hour after the test.

Further research needs to be directed toward the effect of condensation on the reliability of GaN HEMTs.

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