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REDESIGN OF THE AD820 SINGLE-CHANNEL CIRCUIT FOR THE DEVELOPMENT OF THE ARD820 LOW-NOISE RAIL-TO-RAIL OPERATIONAL AMPLIFIER

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The task of this study was to design and later produce a low-power (single supply 5–30 V, dual supply ± 2.5 V and ± 15 V) rail-to-rail operational amplifier aRD820 with low voltage noise (<4 μV, p-p. 0.1 to 10 Hz), ultralow input bias current (< 15 pA), and low offset voltage (< 500 μV) characteristics. Similar characteristics are presented by Analog Devices chip AD820. Thus, the task of the design team was to adapt the prototype circuity of AD820 to our technological capabilities, modify the circuit, if necessary, and eliminate any deficiency of the prototype. The input stage module got source followers at the input of the operational amplifier. The second stage module was modified to be more symmetric. The output stage module obtained additional resistors and capacitors to achieve frequency compensation. One FET transistor in the current reference module was substituted with other elements. Simplified electric schemes of these modules of AR820 and aRD820 are presented. The performance of modules of modified electric schemes was tested in Simulink software. Simulations of the full electric scheme for aRD820 demonstrated characteristics similar to those of AD820 data tables. Later production of the aRD820 chip and measurements demonstrated that the planned characteristics of the operational amplifier were met.

Keywords: *AD820, circuit, electric scheme, operational amplifier, rail-to-rail.*

1. INTRODUCTION

An operational amplifier (op-amp) is an essential component in electronics that amplifies voltage [1]–[3]. Op-amps are widely used in various applications, such as signal processing, filtering, and mathematical operations [4], [5] because they can increase the strength of weak electrical signals and perform complex tasks with simple configurations. While traditional operational amplifiers are designed to amplify voltage, operational transconductance amplifiers (OTAs) provide a current output, making them useful in several medical applications [6], [7]. CMOS operational amplifiers have gained widespread adoption in recent years due to their low power consumption and integration capabilities [8], [9], yet amplifiers based on complementary bipolar technology [10], [11], like the AD820, continue to excel in precision applications. Each technology serves distinct purposes: CMOS is ideal for modern, low-power digital systems, while bipolar amplifiers remain the gold standard for low-noise, high-precision analogue applications.

A rail-to-rail amplifier is a type of operational amplifier designed to utilise the full range of the power supply voltage, from the lowest supply rail (ground) to the highest supply rail (positive voltage). This means it can produce output voltages that go very close to the minimum and maximum supply voltages, enhancing its versatility in low-voltage applications. The development of low-voltage operational amplifiers capable of achieving rail-to-rail input and output operation has been a significant advancement in precision signal processing. One notable design achieves this functionality by incorporating a nested-loop frequency-compensation technique, allowing stable performance even at supply voltages as low as 1.5 V [12]. Operational amplifiers are also used for high supply voltages, e.g., 30 V [13]. For applications requiring rail-to-rail input and output, new bulk-driven amplifier designs offer significant performance improvements. The use of composite transistor arrays has been shown to provide superior voltage gain without sacrificing power efficiency [14]. A recent design using a folded cascode architecture and Class AB output stage achieved rail-to-rail performance with low power consumption and high gain [15]. Another work proposes a rail-to-rail auto-zero operational amplifier using a time-interleaved charge pump circuit to ensure low power consumption and low offset voltage [16].

Operational amplifiers could be single-stage, two-stage, three-stage, and multistage. The comparison of single and two-stage CMOS op-amps showed that single-stage op-amp is more stable and operates for longer duration of time, while two-stage op-amp produces a larger output with lower noise [17].

The design of operational amplifiers for space applications requires consideration of radiation-induced effects, such as total ionizing dose (TID). Techniques such as hardened-by-design (RHBD) have been successfully implemented to mitigate these effects, as demonstrated in the development of a rail-to-rail operational amplifier resilient to radiation doses up to 500 krad(Si) [18].

Analog Devices, Inc. developed a technology for vertical NPN and PNP transistors known as complementary bipolar (CB) technology. This innovation significantly enhanced various chip solutions, including operational amplifiers. Leveraging this technology, Analog Devices, Inc. intro-

duced several operational amplifiers – single-channel AD820 (1993), two-channel AD822 (1994), and four-channel D824 (1995). These amplifiers exhibited exceptional characteristics regarding input current, noise levels, dynamic performance, and low power consumption. While they did not achieve the highest possible specifications in any single parameter, their balanced performance made them highly useful in many applications, particularly those requiring low input currents.

The AD820 is a precision, low-power operational amplifier developed by Analog Devices, Inc., tailored for single-supply applications that demand high accuracy and efficiency. It operates over a wide supply voltage range (single supply 5–30 V, dual supply ± 2.5 V and ± 15 V), making it suitable for both low-voltage portable devices and higher-voltage industrial systems. Key features include an ultralow input bias current of less than 15 pA and a low input offset voltage below 500 μV, which minimise errors when interfacing with high-impedance sources and enhance overall measurement precision. The amplifier also exhibits low voltage noise, specified at less than 4 μV peak-to-peak within the 0.1 Hz to 10 Hz frequency band, crucial for applications involving low-frequency, low-level signal amplification, such as precision instrumentation and sensor signal conditioning. Moreover, the AD820 offers a rail-to-rail output swing, allowing the output voltage to approach the supply rails closely and thereby maximizing the dynamic range, especially in low-supply-voltage scenarios. Despite its low power consumption, with a typical quiescent current of only 800 μA, the amplifier maintains a moderate gain-bandwidth product suitable for various analogue signal processing tasks. Its design effectively minimises both flicker (1/f) noise and thermal noise contributions, ensuring signal integrity across varying temperatures and supply voltages. These attributes make the AD820 an excellent choice for precision analogue applications where low noise, ultralow input bias current, and low offset voltage are essential, including medical instrumentation, active filtering, and high precision data acquisition systems.

The task of this study was to design and later produce a low power (single supply 5–30V, dual supply ± 2.5V and ± 15 V) rail-to-rail operational amplifier with low voltage noise (<4 μV, p-p. 0.1 to10 Hz), ultralow input bias current (< 15pA), and low offset voltage (< 500 μV) characteristics. Similar characteristics are presented by Analog Devices chip AD820. Thus, the task of the design team of RD Alfa Microelectronics was to adapt the prototype circuity of AD820 to our technological capabilities, modify the circuit, if necessary, eliminate any deficiency of the prototype, and utilise previous results obtained from designing the low-voltage four-channel amplifier microchip aRD824 [19], [20].

The list of planned parameters of aRD820 compared to the datasheet values of AD820 is given in Table 1. It shows that aRD820 is expected to achieve similar characteristics to AD820 and even exceed in some parameters.

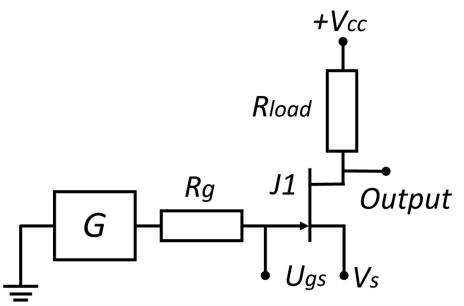

Fig. 1. Electric scheme to test FET transistors. $+V_{cc}$ – supply voltage, R_g – generator resistor, R_{load} – load resistor, $J1$ – FET transistor, G – signal generator, V_s – voltage on source, U_{gs} – voltage gate source.

Table 1. Planned Specification of an Operational Amplifier
aRD820 Chip and Specification of Analog Devices AD820 Chip

No.	Parameter	Tempera-ture*	aRD824 (planned)		AD820 (AD820A) [21]			Units
			Minimal values	Maximal values	Minimal values	Typical	Maximal values	
1	Offset Voltage	T_{NORM} T_{MIN} to T_{MAX}	-0.5 -1.5	0.5 1.5		0.1 0.5	0.8 1.2	mV
2	Input Bias Current	T_{NORM} T_{MIN} to T_{MAX}	-15 -4000	15 4000		2 500	25 5000	pA
3	Input Offset Current	T_{NORM} T_{MIN} to T_{MAX}	-10 -500	10 500		2 500	20	pA
4	Large Signal Voltage Gain R_L = 1 kΩ R_L = 2 kΩ R_L = 10 kΩ R_L = 100 kΩ	 T_{NORM} T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX}	 10 50 250 180		 15 10 80 80 400 400	 30 150 1000		V/mV
5	Output Voltage (High)** I_{SOURCE} = 20 **µA** I_{SOURCE} = 2.5 mA I_{SOURCE} = 15 mA	 T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX}		 14 20 110 160 1500 1500		 10 80 800	 14 20 110 160 1500 1900	mV
6	Output Voltage (Low)*** I_{SOURCE} = 20 **µA** I_{SOURCE} = 2.5 mA I_{SOURCE} = 15 mA	 T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX} T_{NORM} T_{MIN} to T_{MAX}		 7 10 55 80 500 500		 5 40 300	 7 10 55 80 500 1000	mV
7	Voltage noise, 0.1 Hz to 10 Hz			4		2		**µV**, p-p

*T_{NORM} is +22 ± 3 °C for aRD820 and +25 °C for AD820. T_{MIN} to T_{MAX} is a temperature range (-60 ... +125 °C) for aRD820 and range (–40 ... +85 °C) for AD820.

**Output saturation Voltage (High) is the difference between the highest possible output voltage and the positive supply voltage.

***Output Saturation Voltage (Low) is the difference between the lowest possible output voltage and the negative supply rail.

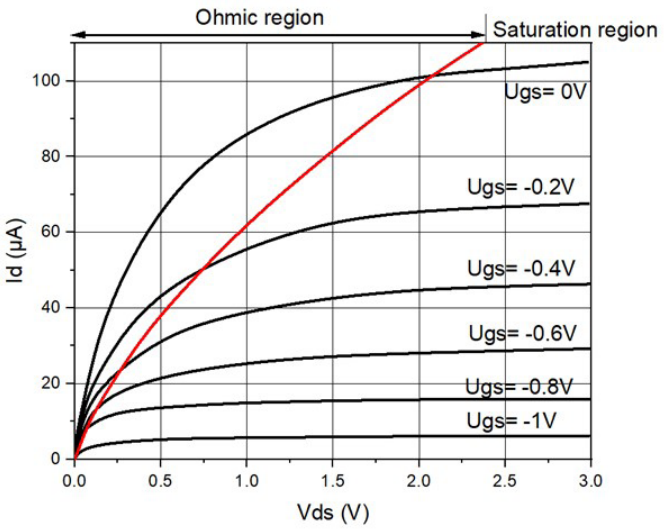

Fig. 2. Exit current-voltage characteristics FET transistor. V_{ds} – voltage drain source, I_d – drain current, U_{gs} – voltage gate source, red line – separation between ohmic and saturation regions for various U_{gs}.

2. INSPECTION OF AD820, REPLICATION, AND DRAWBACK ANALYSIS

We inspected AD820 chip and derived its electric scheme. Then, we replicated this electric scheme on a chip produced in our production facilities. Tests on several such chips showed drawbacks that did not allow them to reach the performance of AD820. We analysed the drawbacks and came to several conclusions.

First, our N-channel FET transistors are inferior to similar transistors used in the input stages and reference source circuits of the AD820. Specifically, amplifier stages using these transistors have poor noise characteristics. The noise voltage swing Vinp-p, referenced to the input, in the range of 0.1 Hz to 10Hz in the circuit shown in Fig. 1 is 5 μV...10 μV, which is more than five times the corresponding value obtained in a similar circuit using an NPN transistor.

Second, the output voltage-current characteristic of our FET transistors has a broader "Ohmic region" compared to the FET transistors of the AD820. The initial section of the voltage-current characteristic of our FET transistor is shown in Fig. 2. The "Ohmic region" is characterised by significantly lower transconductance (gm) values compared to the saturation region: $g_m = dI_d/dV_{gs}$, where dI_d – increment of a drain current I_d, and dV_{gs} – increment of a gate-source voltage V_{gs}. If the FET transistor enters the "Ohmic region" (i.e., the source voltage is close to the drain voltage), the circuit's gain significantly decreases. Since the input stage of the AD820 is similar to the circuit in Fig. 1, its gain undergoes the same changes. When the input voltage (V_{in}) increases to $+V_{cc}$ -2V... + V_{cc} -1V, the op-amp gain can drop to several hundred, especially in amplifiers with a higher gate cutoff voltage (in absolute value) V_{gs0} (the gate source voltage at which I_d becomes 0). Of two operational amplifiers with gate cut-off voltages of -2 V and -1 V, the gain

reduction for input signals close to $+V_{cc}$ will be more significant in the amplifier with the gate cut-off voltage of -2 V, since at equal V_{in} values, the V_{ds} value of these transistors will be lower by approximately 1 V (i.e., it will enter the "Ohmic region" earlier).

Third, our FET transistors have a large spread in gate cutoff voltages V_{gs0}, ranging from -0.5V to -2.5V. This leads to an inability to set the required reference current on crystals with extreme V_{gs0} values, resulting in a low yield of good chips. To demonstrate this assertion, we calculate the value of resistor R_2 (Fig. 3) needed to obtain a 20 μA current flowing through the FET transistor J2: $I_d = I_{d0}(1 - V_{gs}/V_{gs0})^2$, where I_d is the drain current, I_{d0} is the drain current when the gate-source voltage is 0, V_{gs} is the gate-source voltage, and V_{gs0} is the gate cut-off voltage. $V_{gs} = -I_d R_2$; we get: $I_d = I_{d0}(1 + I_d R_2/V_{gs0})^2$. The I_{d0} values obtained from the test FET transistors are as follows: for transistors with V_{gs0} = -0.5 V, I_{d0} is 32 μA. For transistors with V_{gs0} = -2.5 V, I_{d0} is 1600 μA. Substituting the values of V_{gs0} and I_{d0}, we get R_2 values of 5.2 kΩ (V_{gs0} = -0.5 V) and 110 kΩ (V_{gs0} = -2.5 V). This resistance range exceeds the adjustment capabilities of resistors available in our technological line.

Fourth, at drain-gate voltages (V_{dg}) greater than 22 V...25 V, the drain-gate reverse current increases sharply. It can exceed 1 μA, which is unacceptable for input transistors. Therefore, an additional circuit to limit Vdg is needed for the input transistors.

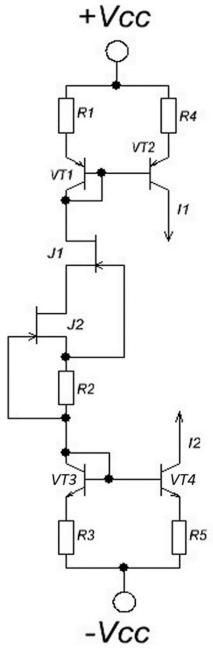

Fig. 3. Electrical scheme used for calculations. Vcc – supply voltage; R1–R5 – resistors; J1, J2 – FET transistors; VT2, VT3, VT4 – NPN transistors; I1, I2 – currents.

Fifth, it was found that produced thin-film resistors had poor characteristics. Therefore, they should be replaced by ion-implanted resistors [22].

Based on the conclusions outlined before, we proposed several modifications for the electric scheme of AD820 that would allow us to reach similar performance, but using strengths and limits of our production facilities. Changes were proposed for the input stage, second (pre-final) stage, output stage, and current reference.

3. PROPOSED DESIGN OF OPERATIONAL AMPLIFIER ARD820

In Microsim software, we developed a model of the AD820 electrical schematic and configured the parameters of the electronic components within limits that can be reached by our production line, e.g., parameters for FET transistors. The simulation results showed that we could not achieve the desired parameters corresponding to the technical data of AD820 [21]. Therefore, several modifications to the elec-

tric scheme of AD820 were proposed and tested. Finally, we got an electric scheme for operational amplifier aRD820 with good simulation performance corresponding to the targeted parameters (see Table 1). Below, we describe several modules of the aRD820 electrical schematic and explain why its performance surpasses that of the AD820 schematic. It should be emphasised that the AD820 electrical schematic is well suited for the production capabilities of Analog Devices, Inc., which manufactures the AD820 that allows it to reach good performance. However, due to the limitations of our production line, this electric scheme does not allow us to reach the expected performance.

3.1. Modification of Input Stage Module

The input stage of an op-amp is designed to receive the input signal and provide initial amplification. This stage is typically implemented as a differential amplifier, which amplifies the voltage difference between the inverting and non-inverting inputs. One of the key functions of this stage is to reject common mode signals, ensuring that only the differential signal is amplified. The input stage is crucial for maintaining a high input impedance, which minimises the loading effect on the preceding circuit. In addition, the bias circuit within the input stage ensures that the transistors operate in the correct region, thus stabilising the overall performance.

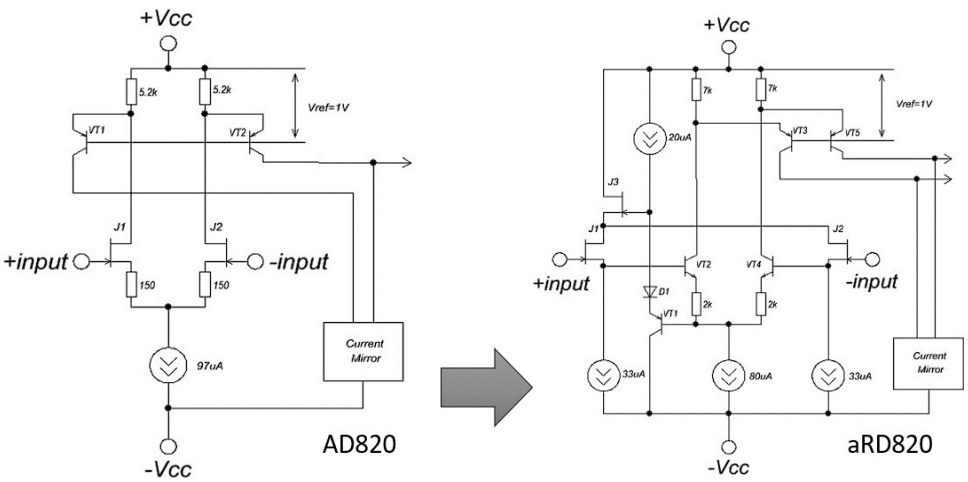

Fig. 4. A simplified electric scheme of the input stage modules of AD820 and aRD820.

Figure 4 shows simplified circuits of the AD820 and aRD820 input stages. By modifying the aRD820 input stage circuit relative to the AD820, we attempted to solve three problems. First, we attempted to reduce the noise of the input stage. Second, we expanded the input signal range toward voltages close to +Vcc. Third, we intended to limit and stabilise the Vds voltage of the input transistors. As indicated above, implementing the input stage as given for AD820 could result in an input noise voltage swing (Vinp-p) of 5 μV to 10 μV in the range of 0.1 H to 10 Hz. Therefore, it was proposed to place source followers J1, J2 at the input of the operational amplifier. This configu-

ration should reduce noise by five times or more. At the same time, using source followers and a differential pair of NPN transistors VT2 and VT4 allows raising the upper limit of the allowable common-mode input signal by at least 0.4 V (since the voltages at the drains of J1 and J2 in these cases are +Vcc - Vref + Vbe for AD820 and +Vcc for aRD820).

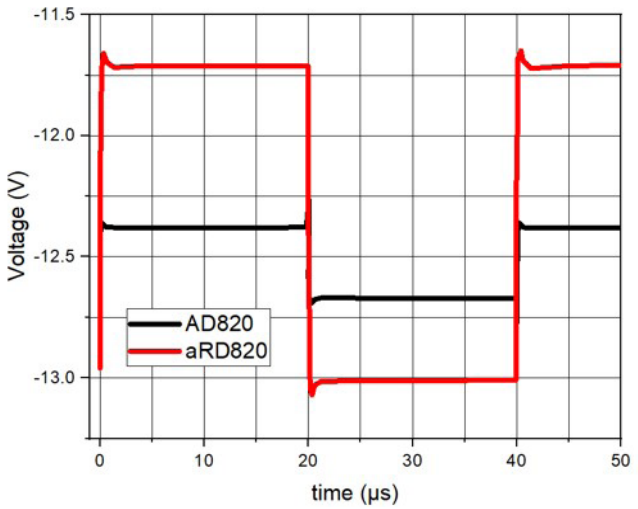

Fig. 5. Signal response of input stage modules of AD820 and aRD820.
Vcc = ±15 V, V(+inp) = 10 V, V(-inp) = 9.9 V ... 10.1 V. Black line: Voltage on the collector of the transistor VT2 of AD820 scheme (Fig. 4), Vout(p-p) = 1.25 V. Red line: Voltage on the collector of transistor VT5 of aRD820 scheme (Fig. 4), Vout(p-p) = 1.5 V.

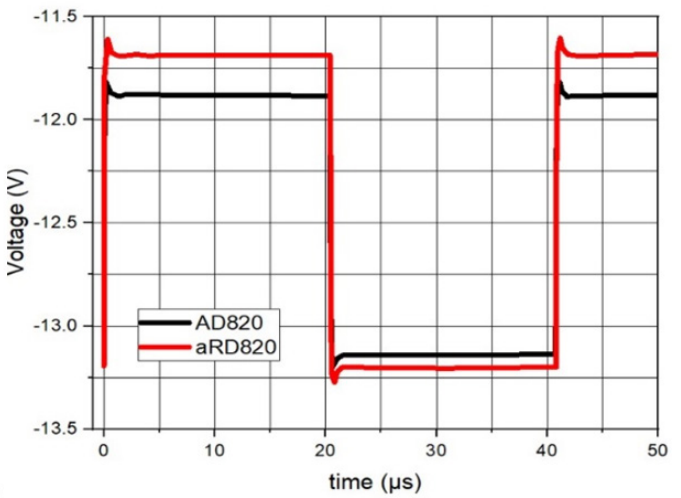

Fig. 6. Signal response of input stage modules of AD820 and aRD820.
Vcc = ±15 V, V(+inp) = 13 V, V(-inp) = 12.9 V ... 13.1 V. Black line: Voltage on the collector of transistor VT2 of AD820 scheme (Fig. 4), Vout p-p = 0.33V. Red line: Voltage on the collector of transistor VT5 of aRD820 scheme (Fig. 4), Vout p-p = 1.3 V.

Figures 5 and 6 illustrate the described advantage of the circuit for aRD820 in Fig. 4, obtained from computer models for input signals close to +Vcc. Instead of a current mirror, a resistive load of 50 kΩ was used, and the FET transistors' gate cut-off voltage was assumed to be Vgs0 = -2 V. In Fig. 5, signal response of input stage modules of AD820 and aRD820 schemes are presented. Parameters used in simulations were Vcc = ±15 V, V(+inp) = 10 V, and V(-inp) is changed from 9.9 V to 10.1 V. The black line corresponds to the voltage Vc(VT2) on the collector of the transistor VT2 of AD820 scheme (Fig. 4) giving peak-to-peak value Vout(p-p) = 1.25 V. The red line corresponds to the voltage Vc(VT5) on the collector of the transistor VT5 of aRD820 (Fig. 4) giving peak-to-peak value Vout(p-p) = 1.5 V.

Figure 6 shows signal response of input stage modules of AD820 and aRD820 schemes. Parameters used in simulations were Vcc = ±15 V, V(+inp) = 13 V, and V(-inp) is changed from 12.9 V to 13.1 V. The black line corresponds to the voltage Vc(VT2) on transistor VT2 of AD820 (Fig. 4) giving peak-to-peak value Vout(p-p) = 0.33 V. The red line corresponds to the voltage Vc(VT5) on transistor VT5 of aRD820 (Fig. 4) giving peak-to-peak value Vout(p-p) = 1.3 V.

Figures 5 and 6 show that for the change of the input signal from +13 V to + 10 V, the gain of the circuit of AD820 drops four times, while the gain drop of the circuit of aRD820 is only 15 %. Similar simulations were made with parameters Vcc = ±15 V, V(+inp) = 14.5 V and V(-inp) change from 14.4 V to 14.6 V. Then, voltage Vc(VT2) on the collector of the transistor VT2 of AD820 showed peak-to-peak value Vout(p-p) = 26 mV. Correspondingly, voltage Vc(VT5) on the collector of the transistor VT5 of aRD820 showed peak-to-peak value Vout(p-p) = 28 mV.

At high supply voltages (+Vcc = +30 V; -Vcc = 0 V) and low input signals (Vin < 7 V), there is a significant reverse current at the drain-gate junctions of the input transistors J1, J2 of (Fig. 4, electrical scheme AD820), causing the input current of the operational amplifier to exceed the norm. To avoid this effect, the aRD820 uses a circuit limiting the voltage in the drains of the input transistors, including the transistors VT1, J3, the diode D1, and a current source of 30 μA. This ensures that the voltages at the drains of J1 and J2 are approximately equal to Vin - 2Vgs +Vbe, where Vgs is the gate-source voltage of J1 (J2). The average Vgs is -1.2 V, and Vbe is 0.65 V. Therefore, the drain voltages of J1 and J2 will be Vin + 3.05 V, and Vdg at the input signals Vin < +Vcc - 3.05 V remain almost constant at 3.05 V.

The input stage circuit of aRD820 has two drawbacks. First, the introduction of an additional stage increases the phase shift and theoretically reduces the stability. Second, the introduction of an additional stage imposes a restriction on the gate cut-off voltage Vgs0 of the input transistors J1 and J2. The gate cutoff voltage must not exceed - 0.8 V ... -0.9 V (i.e., it must be between -0.9 V and -2.5 V). Otherwise, the differential stage transistors VT2, VT3 will close when an input signal close to -Vcc is applied. Considering the advantages and disadvantages of the input stage circuit of aRD820, we deemed it feasible to use this circuit, addressing stability issues by modifying the pre-final stage, using additional frequency compensation in the final stage, and selecting wafers based on the Vgs0 parameter of test FET transistors during manufacturing.

During the design of the input stage, special attention was paid to minimising the offset voltage of the operational amplifier. In AD820, it does not exceed 800 μV and

is achieved by laser trimming of thin-film resistors located in the sources of the input FET transistors. Since we decided not to use thin-film resistors, we proposed to use an array of cutting resistors with fuses, blown by current, in aRD820. The trimming resistors are located in both arms of the lower NPN transistors of the current mirror of aRD820. The resistor values are chosen so that the adjustment range of the operational amplifier offset voltage is from -10 mV to +10 mV, with the total voltage drop across the resistors not exceeding 100 mV.

3.2. Modification of the Second (Pre-final) Stage Module

Typically, the second stage, also known as the gain stage, provides most of the op-amp's voltage gain. This stage may employ a common emitter or common source amplifier configuration, which enables high-voltage amplification. The high gain of this stage allows the op-amp to amplify even very small input signals effectively. Additionally, this stage ften includes frequency compensation, typically in the form of a Miller compensation capacitor, which helps to stabilise the amplifier by controlling the bandwidth and preventing oscillations. This ensures that the op-amp remains stable across a wide range of frequencies. For our scheme of aRD820, the main gain of op-amp was performed at the first stage.

Figure 7 shows simplified circuits of the second (pre-final) stages of AD820 and aRD820. The second stage of aRD820 has a symmetrical structure, resulting in equal signal propagation times in the upper and lower arms. In AD820, the additional signal delay in the upper arm (VT1-VT3-VT2-VT4) is compensated by the parallel connection of capacitor C1. Calculations showed that the signal delay (and, consequently, phase shift) in the circuit in the aRD820 scheme is 3.5 times less than in the circuit in the AD820 scheme, even at lower operating currents in the stage. Thus, the circuit of aRD820 will provide greater stability to the operational amplifier compared to the circuit of AD820. Additionally, the circuit of aRD820 uses additional emitter followers VT3, I3, and VT4, I4 to reduce the operational amplifier's offset voltage. They ensure identical input currents of the stage for any β values of the Npn and Pnp transistors.

3.3. Modification of Output Stage Module

The output stage of an operational amplifier is responsible for driving the load connected to the op-amp's output. To achieve this, the output stage often uses a push-pull configuration, which can both source and sink current, making it highly efficient and capable of driving low-impedance loads. This stage provides current gain and reduces output impedance, ensuring that the op-amp can deliver sufficient current to the load without significant distortion. In some designs, a buffer is also used in the output stage to isolate the high-gain second stage from the load, further improving performance.

Figure 8 shows simplified circuits of the output stages of AD820 and aRD820. To compensate for the increased phase shift introduced by the VT2 and VT3 transistors in the aRD820 input stage (see Fig. 4), frequency compensation was proposed in the output stage. The compensation elements are C1, C2, R1, and R2.

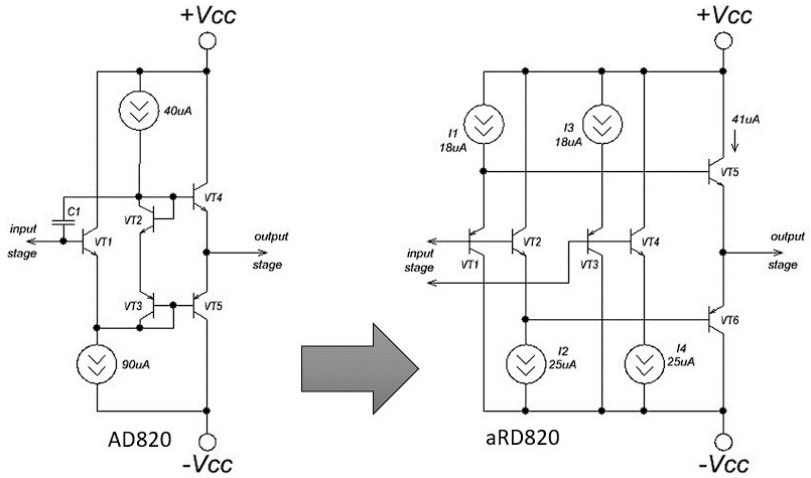

Fig. 7. Simplified electric schemes of the second (pre-final) stage modules of AD820 and aRD820.

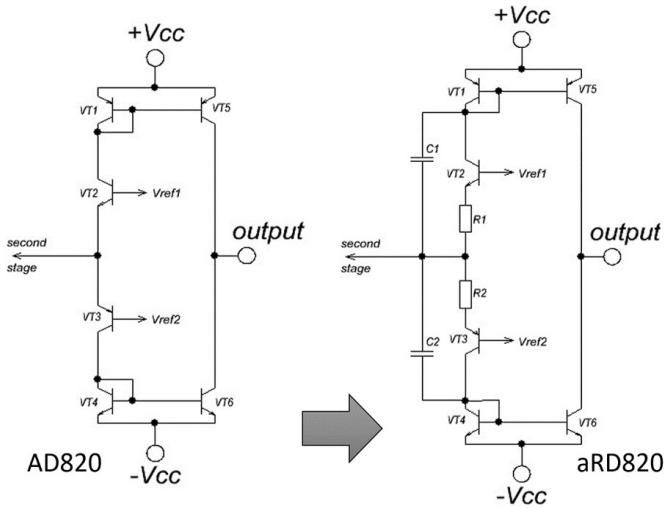

Fig. 8. Simplified electric schemes of the output stage modules of AD820 and aRD820.

Figures 9 and 10 illustrate a comparative analysis of the amplitude-frequency and phase-frequency characteristics of simulated signals of the circuits AD820 and aRD820. The parameters used in simulations were Vcc = ±15V, VACinp = 1mV, Rload = ∞, and Cload = 0. The gain of the output stage of aRD820 is lower than that of the circuit in AD820, but we considered this acceptable due to the ample margin for this parameter. The phase-frequency characteristic of the circuit of aRD820 appears preferable to that of AD820 scheme. The phase margin of the circuit of AD820 at 3MHz is 68.6 degrees, while for aRD820 it is 89.6 degrees. The frequency of 3 MHz was chosen because it is close to the unity gain frequency of the operational amplifier. The operational amplifier is considered stable with a phase margin of at least 45 degrees at the unity gain frequency.

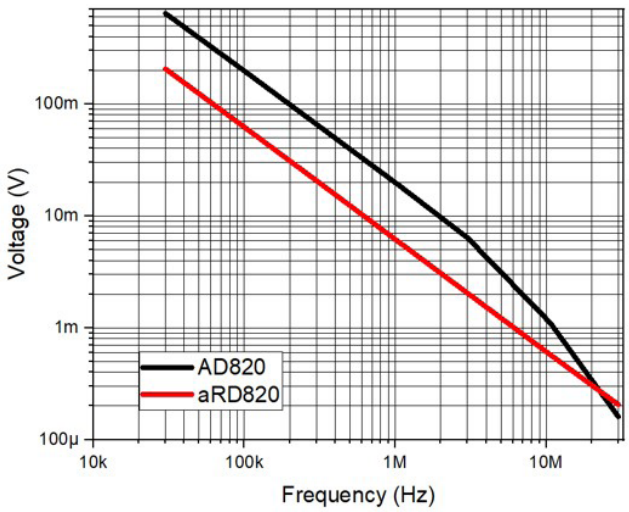

Fig. 9. Simulation of output module of operation amplifiers AD820 and aRD820. Voltage vs. frequency.

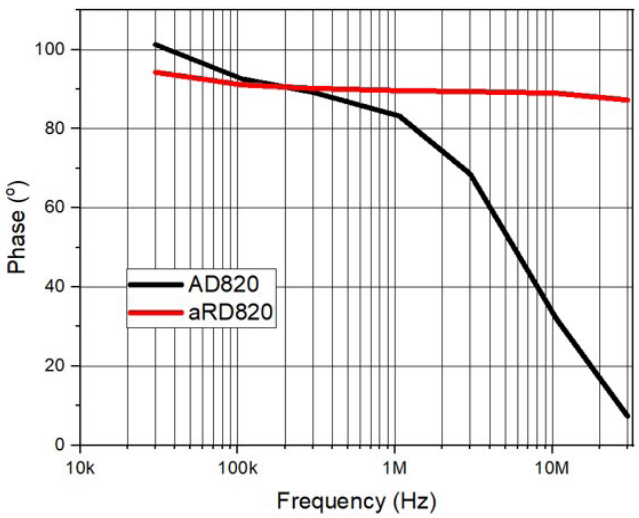

Fig. 10. Simulation of output module of operation amplifiers AD820 and aRD820. Phase vs. frequency.

3.4. Modification of the Current Reference Module

The current reference circuit is a fundamental component that ensures stable operation of the op-amp under varying conditions, such as changes in temperature or power supply voltage. The current reference typically consists of a constant current source and current mirrors, which provide a stable bias current to the transistors in both the input and second stages. This stable biasing ensures consistent operation, allowing the op-amp to maintain its performance across a range of operating conditions.

As described earlier, using a reference source circuit of AD820 would inevitably result in a low yield of good op-amp chips. Therefore, it was proposed to eliminate the FET transistors determining the reference current magnitude. Figure 10 shows the reference source circuits of the AD820 and aRD820. In the current reference circuit of aRD820, there is only one FET transistor that is used as an element to initiate the circuit, so it can also work with average characteristics. The reference current is set using the PNP transistor VT10. This current is approximately equal to the sum of the currents through resistors R3 and R4.

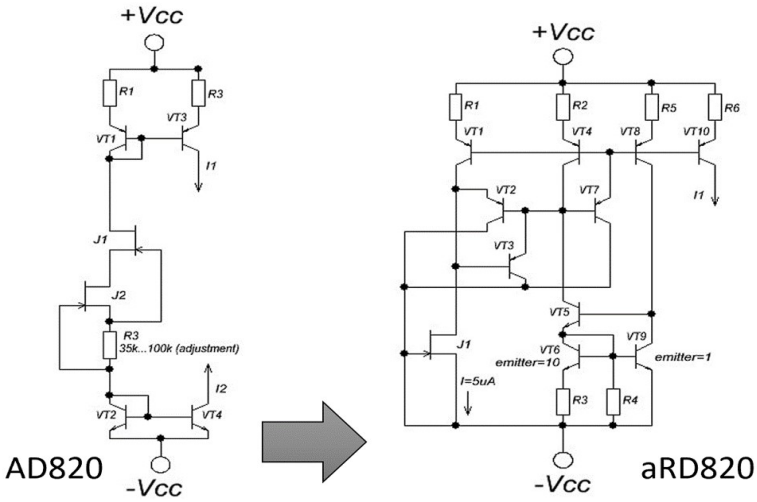

Fig. 11. Simplified electric schemes of the current reference modules of AD820 and aRD820.

The current through resistor R3 has a positive temperature coefficient, while the current through resistor R4 has a negative one. Thus, the resistances of R3 and R4 are chosen so that the current through VT10 remains constant over a temperature range of -40 °C to +85 °C. The exact reference current value will be set using trimming resistors connected in series with R6. The total drift of the reference current over the temperature range of -40 °C to +85 °C and the entire supply voltage range should not exceed 5 % to 10 %.

3.5. Simulations of the Full Electric Schemes of AD820 and aRD820

The modified components described above and the complete operational amplifier circuit were simulated using the Microsim circuit simulation program. Parameters of the components and the entire operational amplifier model were determined over temperature ranges (-40 °C to +85 °C), supply voltages (+30 V 0V; +5 V 0 V; ±2.5 V; ± 5V; ± 15V), input signals (-Vcc ... +Vcc), load capacitances (up to 350 pF), and output currents (up to 20 mA).

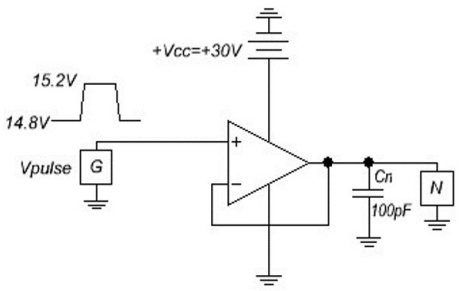

Fig. 12. Schematics to test the performance of operation amplifiers AD820 and aRD820.

Particular attention was paid to the impact of replacing thin-film resistors (as in AD820) with diffusion and ion-implanted resistors, as diffusion and ion-implanted resistors have significantly higher temperature coefficient of resistance. Simulation showed that this replacement did not significantly affect the operational amplifier parameters. Moreover, special attention was given to the model's dynamic properties, specifically its stability. To assess stability, an operational amplifier configuration with a gain of A = +1 and a load capacitance of Cn = 100 pF was used (Fig. 12).

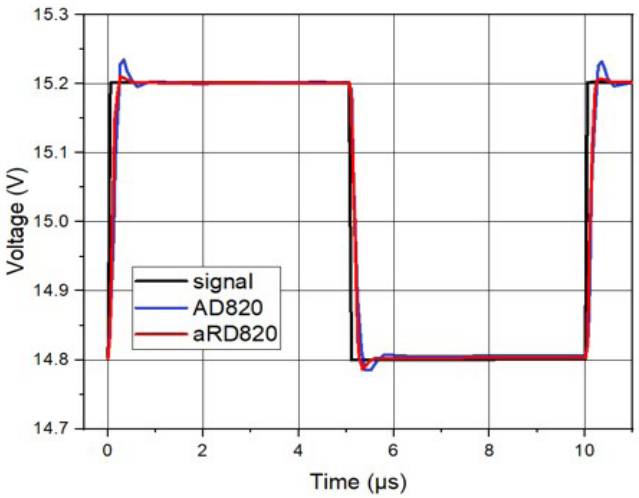

Fig. 13. Input and output signal oscillograms (simulations).

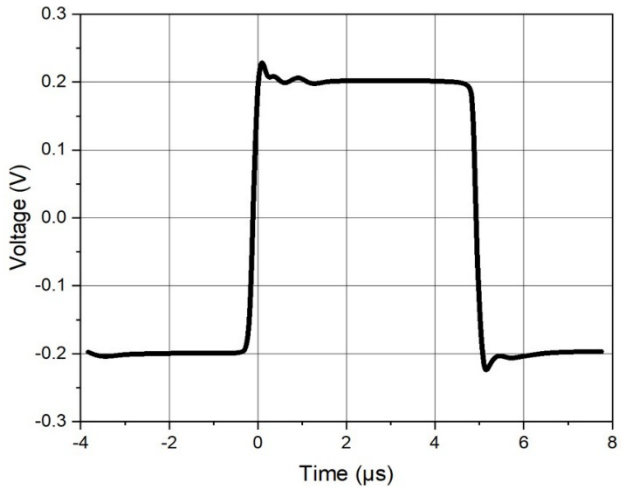

Fig. 14. Output signal oscillograms (tests).

Figure 13 shows the input and simulated output signal oscillograms of the AD820 and aRD820 models for the above configuration. As seen, the AD820 has a longer transition process during voltage jumps. Additionally, the aRD820 has a slightly higher slew rate. Finally, Fig. 14 shows the output signal oscillogram of the

actual aRD820 microchip (Vcc = ±15 V) demonstrating similar performance.

Later production and tests of aRD820 chips showed that the expected parameters of the operational amplifier given in Table 1 were achieved.

4. CONCLUSION

The task of the research was to design, construct, and test a single-channel, low-noise, rail-to-rail operation amplifier aRD820 with the specification given in Table 1, based on an initial prototype of the Analog Device AD820 chip. Due to limitations and specificity of available production lines, the construction of a chip that has implemented an electric scheme of AD820 prototype is not reasonable, as a high rate of damaged chips with poor performance will be obtained. Therefore, a modified electric scheme of AD820 prototype was proposed, allowing it to reach the targeted performance.

The input stage module got source followers at the input of the operational amplifier (Fig. 4). The second stage module was modified to be more symmetric (Fig. 7). The output stage module obtained additional resistors and capacitors to achieve frequency compensation (Fig. 8). One FET transistor in the current reference module was substituted with other elements (Fig. 11). The performance of modules with modified electric schemes was tested in Simulink software. Simulations of the full electric scheme for aRD820 showed that it exhibited characteristics like those of AD820 data tables. The aRD820 chip was produced, and measurements demonstrated that the planned characteristics of the operational amplifier were met.

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