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CMOS rail-to-rail voltage-to-current converter circuit intended for low-voltage IC applications

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In this paper a new CMOS voltage-to-current converter (VTC) circuit with rail-to-rail dynamic range is proposed. The circuit is dedicated for integrated circuits that require low-voltage power supply. The input/output voltage dynamic range of conventional VTC circuits is usually impaired by the reduced of power supply voltage. The proposed VTC aims to alleviate non-desirable the effects of the reduction of the power supply voltage on the VTC dynamic range by using a combination of voltage followers. It is designed using the transistor models of the 65 nm CMOS technology and it is intended to operate with low power supply voltages. SPICE simulation results demonstrate that the input dynamic range of the proposed VTC circuit covers the entire range from 0 V to 1.2 V, the maximum range allowed by the used power supply. This rail-to-rail property makes the proposed VTC circuit highly suitable for CMOS integrated circuits low-voltage applications.

Key words: 65 nm CMOS technology, rail-to-rail voltage-to-current converter, low-voltage IC applications

1 Introduction

The voltage-to-current converter (VTC) is a fundamental electronic circuit essential for various integrated circuits (ICs) applications, such as voltage-controlled oscillators (VCOs), phase-locked loops (PLLs), delay-locked loops (DLLs), DC-DC switching regulators, and variable-gain amplifiers (VGAs) [1-7], among others. As its name states, a VTC converts an input varying voltage to a corresponding current which is used to control the functionality of a dedicated electronic circuit. For example, a VTC is usually used to control or modulate the output frequency of a voltage controlled-oscillator of a PLL.

Nowadays, modern electronic applications are based on integrated circuits that operate with low-voltage power supplies. In these applications, the limited voltage power supply often causes a significant reduction in the input/output dynamic range (DR) of various circuits. Therefore, there is a critical need to redesign most circuits intended to operate with low-voltage power supplies in order to maximize their input/output dynamic range (DR).

In this context, a new VTC circuit with rail-to-rail input dynamic range dedicated to low-voltage power supply IC applications is proposed and described. The circuit improves the input voltage dynamic range by using a combination of voltage followers. It is designed using the transistor models of the 65 nm CMOS technology and it is intended to operate with low power supply voltages. SPICE simulation results demonstrate that the input dynamic range of the proposed VTC circuit covers the entire range from 0 V to 1.2 V, that is the maximum range allowed by the used power supply.

2 Description of the proposed VTC

The most effective way to convert a voltage to current is by applying a voltage to a resistor, as shown in the circuit schematic in Fig. 1.

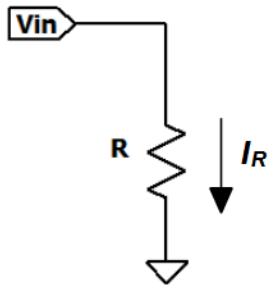


Fig. 1. Concept of converting a voltage to a current using a resistor

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One interesting attribute of such a circuit is its high-linearity, due to the voltage-to-current conversion being governed by the relation $I=V/R$. On the other hand, this circuit faces the issue that the source that generates the input voltage V_{in} should be able to drive a low-impedance charge which is the resistor R_1. Moreover, the converted current cannot be conveyed or reproduced by using a simple resistor as a VTC. These limitations can be easily overcome by using the well known CMOS voltage follower circuit. As shown in Fig. 2. this follower is principally composed of an NMOS transistor, configured as a common drain and a load resistor R_1 and where the input voltage is applied to a high impedance, the gate of the transistor [2, 6, 10-13].

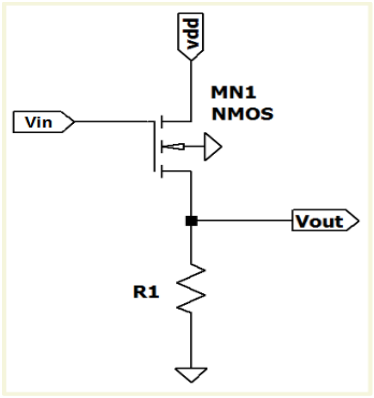


Fig. 2. Basic voltage follower circuit using an NMOS transistor

In this configuration, the NMOS transistor acts as a level shiftier, hence, the voltage (V_{R1}) at the source of the transistor is equal to the input voltage V_{in} scaled-down by the threshold voltage V_{th} of an NMOS transistor

$$(V_{R1} = V_{in} - V_{th})$$

In the case where V_{in} is greater than V_{th} and the MOS transistor body effect is neglected, the circuit works as a voltage follower and the current $I_{R1,}$ flowing through the resistor R_1, can be considered to vary linearly with V_{in}. In such a case, the current can be expressed as:

$$I_{R1} = (V_{in} - V_{th})/R_1$$

In fact, since the threshold voltage V_{th} varies with the voltage V_{R1} across R_1, the linearity of current I_{R1} is influenced by this variation [8, 9, 11, 13].

On the other hand, when the input voltage V_{in} is lower than the threshold voltage V_{th}, the NMOS transistor turns off, and ideally, the current I_{R1} becomes zero (I_{R1}=0). But, in reality, the NMOS is not completely off when $V_{in} < V_{th}$ but operates in the sub-threshold mode. In this case, the current that flows through the transistor is very small and it depends exponentially on the input voltage V_{in}. In a VTC converter circuit, the range from 0 V to V_{th} represents a significant interval during which the converted current remains zero or very small. In some applications, this can lead to the malfunction of circuits that rely on the VTC, such as in the case of PLLs or systems based on feedback control process. Moreover, because the NMOS transistor operates in the sub-threshold region, the VTC cannot function properly as a follower, and as a result, the converted current is strongly affected by the non-linear effects.

In order for the current I_{R1}, of the circuit of Fig. 2, to be exploited in other circuits, a PMOS current mirror has to be added to the circuit so the converted current can be reproduced. A schematic of a voltage follower circuit incorporating such a current mirror is presented in Fig. 3 [1]. The output current I_{out} is a reproduction of I_{R1} that can be used easily in other circuits without affecting the voltage follower behaviour.

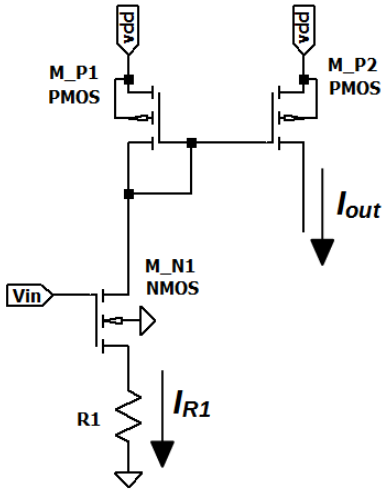


Fig. 3. A basic follower circuit used as VTC

As stated previously, the converted current of the VTC based on a voltage follower is very small when the input voltage V_{in} is smaller than the threshold voltage V_{th}. This is a situation to be avoided in most integrated circuits (ICs) since it leads to the deterioration of the input dynamic range of the VTC.

As shown in Fig. 4, one simple solution to this problem, is to add a DC current source I_1, with a small value, to the output current in such a way that I_{out} is never equal to zero when the voltage V_{in} is equal to zero (V_{in}=0 V).

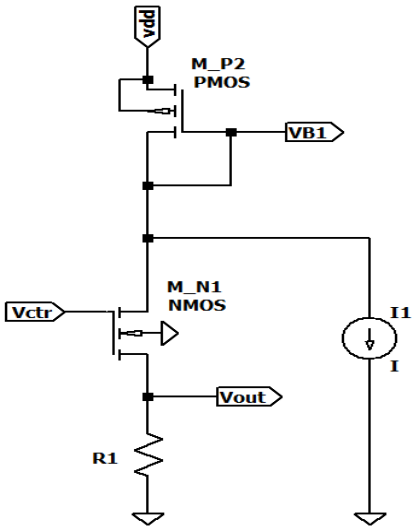


Fig. 4. Conventional *VTC* with an added DC current source

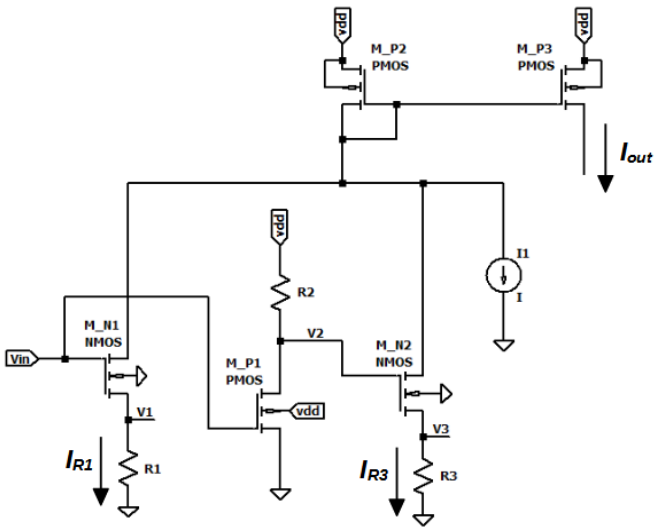


Fig. 5. Schematic of the proposed CMOS voltage-to-current converter

In addition, it is necessary to mitigate the increase in I_{R1} caused by small currents when the input voltage is lower than the threshold voltage V_{th} of the NMOS transistor M_N1. In fact, when $V_{in} < V_{th}$, the transistor M_N1 is either blocked or conducting in the sub-threshold region. In this case, the transistor's drain current is very small and varies exponentially with V_{in}, which consequently introduces significant non-linearity in the converted current.

2.1 The proposed voltage-to-current converter (VTC)

Figure 5 shows a new VTC architecture designed to widen the input dynamic range. To achieve this, two additional stages are added to the basic circuit shown in Fig. 4 to address the non-linearity introduced by the NMOS transistor M_N1 when $V_{in} < V_{th}$. In a such case, the sub-threshold current of the transistor M_N1 will be very negligible compared to the current added by the two additional stages. An addition constant and small current source is added to the circuit to guaranty that the VTC output current I_{out} is always exceeds zero.

The first stage of this VTC is designed to implement an NMOS follower similar to the one in the circuit shown in Fig. 4. The current I_{R1} flowing through the resistor R_1 is equal to the voltage V_1 applied across R_1 divided by the value of R_1

$$I_{R1} = V_1/R_1 = (V_{in} - V_{th})/R_1$$

Here V_1, as stated before, is equal to $(V_{in} - V_{th})$.

The second stage is designed to generate the voltage V_2 which is necessary to properly drive the third stage of the circuit. It is composed of the PMOS transistor M_P1 and a load resistor R_2. This stage also functions as a voltage follower, with the transistor M_P1 controlled directly by the input voltage V_{in}. In this case, instead of using an NMOS transistor, a PMOS transistor is employed, resulting in the output voltage V_2 being equal to the input voltage V_{in} plus the PMOS threshold voltage V_{tp}:

$$V = V_{in} + |V_{tp}|$$

The circuit operates as a voltage follower as long as $V_{in} < V_{DD} - |V_{tp}|$. Consequently, the practical range of V_2 extends from $|V_{tp}|$ to V_{DD} as V_{in} varies from 0 to V_{DD}.

The third stage of the *VTC* also implements an NMOS follower. It is driven by the output voltage V_2 generated by the second stage of the VTC. Since the minimum value of V_2 is equal to $|V_{tp}|$ as V_{in} begins to increase from 0 V, the current I_{R3} flowing through R_3 remains greater than zero at all times, regardless of the value of V_{in}. Moreover, I_{R3} varies linearly with V_2, and consequently, with V_{in} as well. I_{R3} is given by

$$I_{R3} = V_3/R_3 = (V_{in} + |V_{tp}| - V_{th})/R_3$$

Considering that V_{th} and $|V_{tp}|$ are nearly equal, the current I_{R3} can be expressed as:

$$I_{R3} = V_{in}/R_3$$

The current I_{R3} is by far larger than current I_{R1} when V_{in} is less than V_{th} of the MOS transistor. The total output current I_{out} of the proposed *VTC* is formed by adding the current I_1 of the 1st stage to the current I_{R3} of the 3rd stage.

$$I_{out} = V_{in}/R_3 + (V_{in} - V_{th})/R_1 + I_1$$

$$I_{out} = V_{in}/(R_1+R_3) + V_{th}/R_1 + I_1$$

Given that I_1, V_{th}, R_1, and R_3 are constant, it is evident that the output current I_{out} varies linearly with the input voltage V_{in}.

3 Simulation results

The proposed VTC circuit was designed using the parameters of a 65 nm CMOS technology and simulated using LTspice simulation of Linear Technology Inc. The simulated circuit with all the MOS transistor and resistor sizes is presented in Fig. 6.

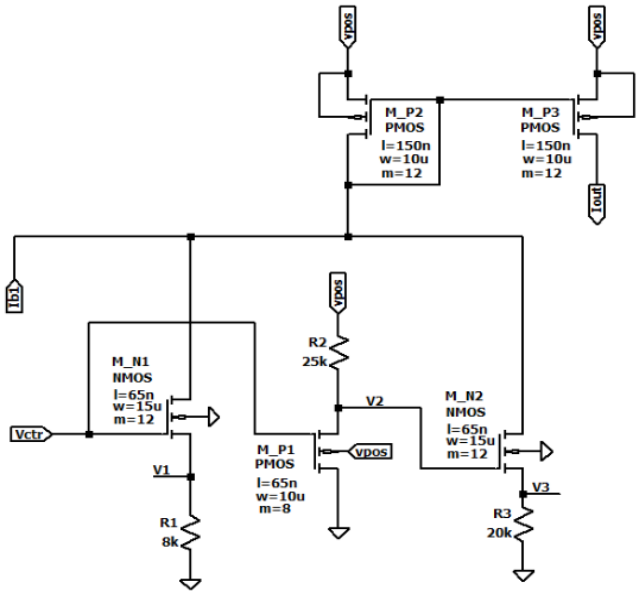


Fig. 6. The actual designed VTC circuit

The current source I_1 is implemented by the circuit of Fig. 7, a beta-multiplier reference [8].

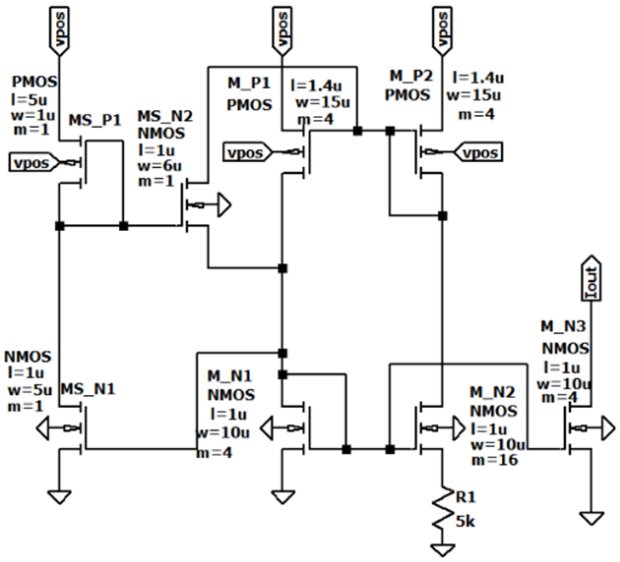


Fig. 7. Schematic of the circuit used to generate reference current I_1 of the VTC circuit

3.1 VTC transfer characteristics

To determine the transfer function of the *VTC* circuit, a DC sweep simulation is carried out with LTspice. The simulation results illustrating the variation of the output current I_{out} with respect to the input voltage V_{in} are shown in Figure 8.

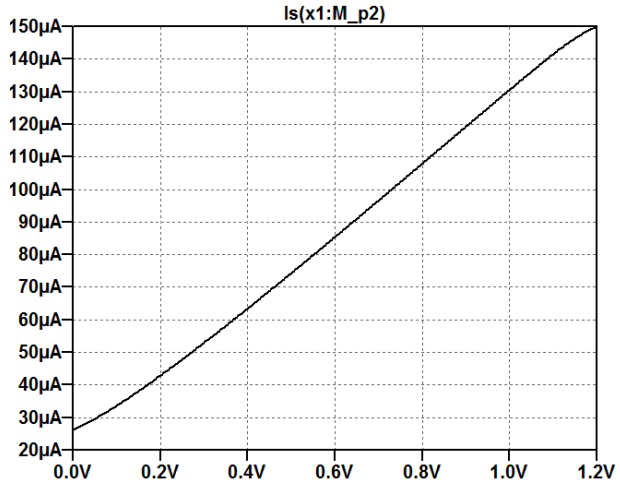


Fig. 8. Simulated input-output characteristic of the proposed *VTC* circuit

The variation of I_{out} with V_{in} shows that the input dynamic range (*DR*) of the *VTC* is very large. In fact, this input dynamic range spans the entire voltage range allowed by the power supply V_{DD}, that is, from 0 V to V_{DD}. This wide dynamic range is highly desirable; however, it is important to note that the linearity of the output current I_{out}, near the upper and lower limits, is not as good as the linearity observed in the mid-range. This non-linearity is primarily due to the fact that when the gate voltage of a MOS transistor falls below its threshold voltage, the device operates in the sub-threshold region [8, 11].

In this mode, the transistor cannot effectively function as a voltage follower, leading to degraded circuit performance.

In certain applications, it is desirable to adjust the slope of the VTC output current variation with respect to the input voltage V_{in}. In the proposed circuit, this can be easily achieved by modifying the value of resistor R_1 in the configuration shown in Fig. 6. This effect is demonstrated by the simulation results for different R_1 values, as illustrated in Fig. 9.

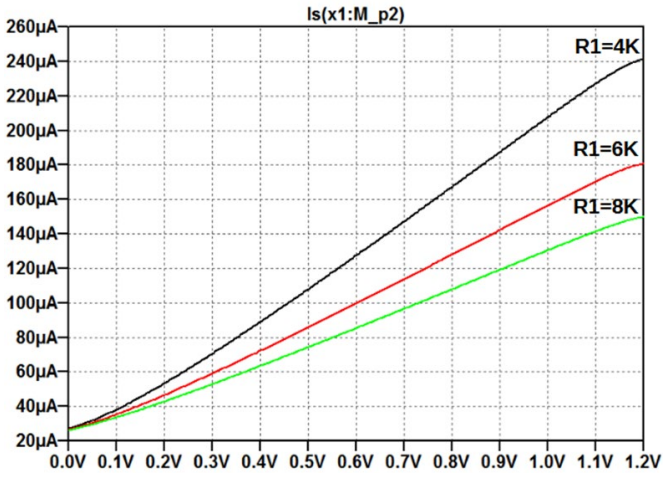


Fig. 9. Variation of the slope of the output current of the proposed VTC of different values of R_1

3.2 Sensitivity of the VTC output current to the power supply fluctuations

Since the VTC is usually used in the area of mixed-mode applications, it is important to evaluate the sensitivity of VTC output current to the power supply SIO fluctuations defined as I_{out}/V_{DD}. In fact, in such situation, the power supply line is subject to large variations induced by the activity of the different digital and analog sub-blocks that share the same substrate. To evaluate the sensitivity SIO, an AC simulation is carried out on the VTC circuit. This simulation is carried out over the range of 1 MHz to 1 GHz and the results are presented in Fig. 10.

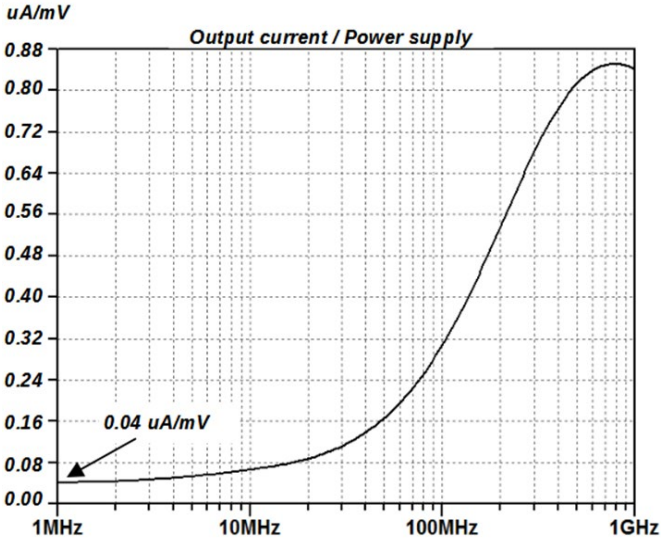


Fig. 10. Frequency variation of the sensitivity, I_{out}/V_{DD} of the proposed VTC

As show, SIO is approximately equal to 0.04 µA/mV to 0.08 µA/mV in the range of low-frequencies (1 MHz to 20 MHz) and increases rapidly as the frequency moves toward higher frequencies.

In the cases where this level of sensitivity at high frequencies is not acceptable, the solution could be the use of a voltage regulator to power supply the VTC and hence reduce the output current sensitivity.

4 Conclusion

The scope of this paper was the description of a new CMOS voltage-to-current converter (VTC) circuit with a wide input dynamic input range (DR). The circuit is dedicated to low-voltage integrated circuits applications that require low-voltage power supply. It based on using a combination of CMOS voltage followers and it is designed using transistor models of a 65 nm CMOS technology and LTspice simulator of Linear Technology Inc.

SPICE simulation results demonstrate that the input dynamic range of the proposed VTC circuit covers the entire range from 0 V to 1.2 V, the maximum range allowed by the used power supply. The sensitivity of the circuit output current to the power supply voltage I/V_{DD} is about 0.04 µA/mV to 0.08 µA/mV at low-frequencies and increases rapidly as the frequency moves toward higher frequencies.

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