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Novel ternary logic gate circuits using CNTFET technology for energy-efficient design

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Ternary logic, which utilizes three distinct logical states instead of the traditional two, is often considered a more effective alternative to binary logic. This increased state capacity can lead to benefits such as reduced chip size, lower power consumption, and faster response time. The special qualities of carbon nanotube field transistors (CNTFETs), namely their ability to alter diameter and achieve the required threshold voltage, are the foundation of STI design. Because of this characteristic, CNTFETs can be used with multiple-Vth design techniques. This paper presents new designs of ternary logic gates using CNTFET technology. The Synopsys HSPICE with 32 nm CNTFET technology is used to model a ternary inverter and universal gates. The proposed standard ternary inverter achieves a 74.45% reduction in power delay product compared to the existing design. Further, the proposed ternary NAND and NOR gates demonstrate a 50.95% and 81.85% reduction in average power consumption, respectively. Finally, the simulation results demonstrate that the proposed gates exhibit a significant improvement in the power-delay product and can be effectively utilized in energy-efficient designs.

Keywords: CNTFET, MVL, universal ternary gate, noise margin

1 Introduction

Demand for portable and embedded electronic devices is growing daily. Battery-powered devices require a strong emphasis on low-power circuit designs. Si-MOSFET technology is primarily used in the design of nanoscale circuits to achieve energy-efficient integration. On a single chip, maximizing transistor density requires decreasing the physical size of each transistor. However, the reduction in size of these nanoscale devices can lead to short-channel effects, which cause an increase in leakage current [1].

Selected for their remarkable qualities – small size, high transconductance, low power consumption, and low noise – carbon nanotube field-effect transistors (CNTFETs) are a promising technology in the field of electronics. Researchers have been exploring for alternatives due to the limits that have been imposed on technological advancements. In addition to this, it offers a high drive current because of the increased mobility of the current carrier [2]. The rate of technological advancement is getting increasingly closer to the termination of Moore's law. The law states that physical constraints are unlikely to further improve data density.

There is a widespread use of ternary logic. This acceptance is attributed to the fact that ternary logic increases the total number of logic states and enhances the capability for bit processing [3]. Ternary circuits provide a discernible improvement in terms of improved chip area, complexities of the interconnect, and the amount of electricity used [4].

Many researchers have studied how ternary logic circuits can provide a higher storage density than traditional binary logic circuits. Ternary logic-based circuits tend to include geometry-dependent threshold characteristics, which are associated with CNTFETs. This results in improved performance. Additionally, the CNTFET offers excellent mobility as a result of ballistic transport, low off-current features, and a threshold voltage that can be tuned. In short, CNTFET-based ternary logic has emerged as a viable alternative to Si-MOSFETs in the semiconductor industry. Existing research on CNTFET-based ternary logic is limited, with current standard ternary inverter (STI) designs showing poor performance trade-offs.

The existing standard ternary inverter design utilizes six transistors and exhibits a higher power-delay product [5, 6]. Similarly, the conventional ternary NAND and NOR gate implementations require ten transistors each and suffer from elevated average power consumption [5] [7, 8]. In this work, we propose novel designs for the standard ternary inverter as well as ternary NAND and NOR gates, which demonstrate reduced circuit complexity and significantly lower average power dissipation. The major contributions of the paper are as follows:

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- Presents a comprehensive review of existing CNTFET-based ternary circuits.
- Implements and evaluates state-of-the-art designs under a uniform simulation environment.
- Proposed novel low-complexity standard ternary inverter and universal gates.
- Provides a comparative analysis of the proposed work over the state-of-the-art circuit using key performance metrics.

The rest of the paper is organized as follows: Section 2 presents a comprehensive literature review, covering (a) the fundamental concepts of CNTFET technology, (b) the background of ternary logic systems, (c) the architecture and limitations of the standard ternary inverter, and (d) existing ternary universal gate designs. Section 3 presents proposed ternary logic circuits, while Section 4 presents the simulation results and analysis. Finally, Section 5 concludes the work.

2 Literature review

This section will provide a brief review of the CNTFET, followed by the ternary logic, and finally, a review of standard ternary inverters and logic gates is presented.

2.1 Basic background of CNTFET

A carbon nanotube (CNT) is a cylindrical nanostructure created by rolling a graphene sheet into a tube, featuring a honeycomb lattice of carbon atoms – making it an allotrope of carbon. Two variants are single-walled (SWCNT) and multi-walled (MWCNT) CNT structures. Single-walled CNT forms and electrical characteristics depend on the orientation of the graphene sheet rolling. The chiral vector, which defines the properties of CNTs, is given by Eqn. (1)

$$\hat{C}h = n\hat{a}_1 + m\hat{a}_2 \tag{1}$$

A pair of positive integers n and m defines the chirality of a carbon nanotube and corresponds to the unit vectors $\hat{a}_1$ and $\hat{a}_2$. The chirality of the tube indeed corresponds to a pair of integers, n and m. The values of n and m will dictate whether CNTs have electrical characteristics equivalent to those of conductors or semiconductors. In the case when $(n - m)$ is not equal to $3i$, where *'i'* is an integer, the material exhibits the behavior of a semiconductor with a moderate band gap, and this band gap narrows as the nanotube's diameter increases [9, 10].

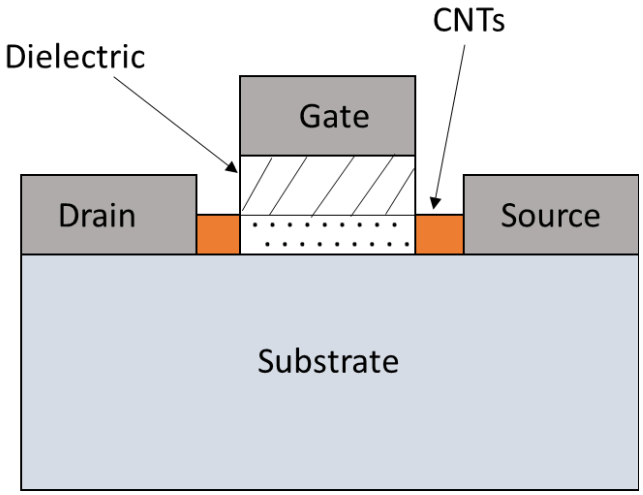

Fig. 1. Schematic of the CNTFET device model

The CNTFET is comparable to the Si-MOSFET, as seen in Fig. 1. Electrons pass from the source (negative) to the drain (positive) via a channel formed of carbon nanotubes. The gate works as a switch, allowing or stopping the flow of current. CNTFETs utilize a single or multiple CNTs as a channel, replacing the silicon layer in Si-MOSFETs [11]. The calculations below help in determining the threshold voltage for various diameters of CNT [12].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{2}$$

$$V_{th} \approx \frac{E_g}{2\epsilon} = \frac{\sqrt{3}a_0}{3\epsilon}\frac{V_\pi}{D_{CNT}} \approx \frac{0.436}{D_{CNT}} \tag{3}$$

D_{CNT} is the diameter of the CNT, while $a_0 = 0.142$ nm is the interatomic distance between each carbon and its neighbour atom. (n, m) pair of integers shows the chirality of the tube, and $V_\pi = 3.033$ eV.

The default channel length of 32 nm, and a high-k top gate dielectric material (planar gate) thickness of 4 nm [13]. The width of the metal gate contact is 6.4 nm, and the pitch (distance between the centers of two adjacent CNTs) is 20 nm. The device has one carbon nanotube with a chirality of (19,0) [14].

2.2 Ternary logic background

Ternary logic circuits have gained significant interest due to their provision of three stable states, which enhances the design of digital circuits. The logic values 0 and 1, respectively, in binary systems correspond to the voltage levels of 0 V and V_{DD}. However, in ternary systems, the voltage levels of 0 V, $V_{DD}/2$, and V_{DD} correspond accordingly to the logic values of 0, 1, and 2, respectively [15]. Ternary circuits make the chip smaller

and simplify connections, which helps save power and reduce delays. Every line has a high storage rate, which could lead to more successful communication paths. Using ternary logic enables fast transfer of data both serially and in parallel [16].

Suppose that X_i and X_j are two literals that are capable of accepting any value from the set {0, 1, 2}, which implies that X_i and X_j are equal to {0, 1, 2}.

$$X_i + X_j = \max\{X_i, X_j\} \quad (4)$$

$$X_i . X_j = \min\{X_i, X_j\} \quad (5)$$

$$\bar{X_i} = 2 - X_i \quad (6)$$

In terms of ternary logic, the sign $'-'$ represents the arithmetic subtraction operation, and '+' denotes the logical OR function. $'\cdot'$ denotes the logical AND operation, and '¯' represents the complement of X_i [17].

2.3 Standard ternary inverters

Three different kinds of inverters are included under ternary logic: the Standard Ternary Inverter (STI), the Negative Ternary Inverter (NTI), and the Positive Ternary Inverter (PTI). Table 1 shows the truth table of these ternary inverters. From the table, it can be seen that the STI provides output at all three levels; however, only two levels are reflected by PTI and NTI [18].

Table 1. Ternary inverter logic table

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

2.3.1 Standard ternary inverters [5]

Figure 2 displays the CNTFET-based STI design, which consists of six CNTFET devices. In this circuit, the CNTFETs *T1*, *T2*, and *T3* exhibit chiralities of (19, 0), (10, 0), and (13, 0), respectively, while the diameters are 1.487 nm, 0.783 nm, and 1.018 nm, respectively. Using Eqn. (2), the calculated threshold voltages of these devices are 0.289 V, 0.559 V, and 0.428 V for *T1*, *T2*, and *T3*, respectively. For transistors *T5*, *T6*, and *T4*, the threshold voltages are –0.559 V, –0.428 V, and –0.289 V, respectively. An output of 0.9 V (logic level 2) results from an input below 300 mV when the supply voltage is set to 0.9 V and the input voltage varies between its low and high states. In this state, *T1* and *T2* are OFF, while *T5* and *T6* are ON. When the input exceeds 300 mV, *T5* remains ON and *T6* turns OFF; *T1* switches ON while *T2* stays OFF. Due to their threshold voltages, *T3* and *T4* cause a 0.45 V drop, setting the output to half the supply voltage (0.45 V), representing logic level 1 as shown in Table 1. When the input surpasses 0.6 V, *T5* and *T6* turn OFF, and *T2*, along with a voltage source, pulls the output to 0 V. A similar transition occurs when the input decreases from high to low.

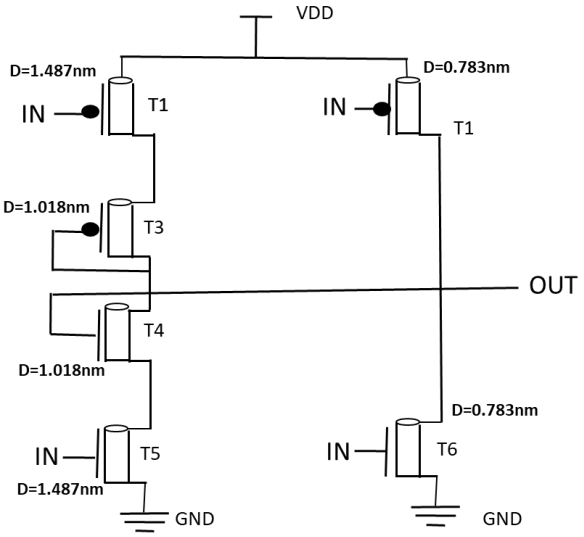

Fig. 2. Standard ternary inverter [5]

The STI circuit shown in Fig. 3 is made up of both PTI and NTI [6]. After the outputs of PTI and NTI, there are two transistors: the N-CNTFET and P-CNTFET, which share the same geometry. Due to their connection to V_{DD} and ground, the transistors connected to PTI and NTI remain active at all times. The sum of NTI and PTI will be the power that comes out of STI. In this way, it gives off the average power. It is shown in Fig. 2 that the STI circuit is faster than the circuit shown in Fig. 3.

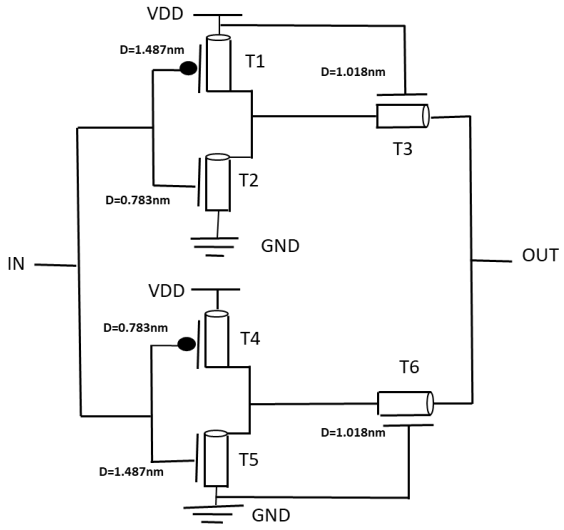

Fig. 3. Standard ternary inverter [6]

2.3.2 Ternary universal gates

Investigating the world of ternary universal gates reveals a fresh landscape of opportunities. This section looks into the complex structure of ternary NAND and ternary NOR gates, examining their capacity to revolutionize digital circuit design. The primary aim of this section is to establish a foundation for emphasizing the significance of universal gates and to analyse them across various parameters that will be examined in detail.

In any design context, consistency and similarity contribute to strength, enhanced performance, and simplified fault identification. Universal gates serve a crucial purpose in digital logic design, enabling the implementation of any logical function [19]. Universal ternary gates possess the capability to realize the functionality of any logic function or equation, making them exceptionally adaptable components in the field of digital circuit design.

The universality of TNAND/TNOR gates allows for the acceptance of all ternary values. For example, a standard ternary inverter can be constructed by linking the inputs of TNANDs, and it can realize a ternary OR gate by interconnecting its inputs via the ternary inverter. In a similar manner, a TNOR gate can be utilized to create a NOT gate (STI) by linking its inputs together. By cascading and mixing these gates, it is possible to create complex logic functions for a variety of applications [20]. Equations (6) and (7) present the logical expression as shown. The logical illustration for ternary universal gates is presented in Table 2.

$$Y_{NAND} = \overline{\min\{In_A, In_B\}} \quad (7)$$

$$Y_{NOR} = \overline{\max\{In_A, In_B\}} \quad (8)$$

In the logical table below, In_A and In_B are the two ternary inputs while Y_{NAND} and Y_{NOR} are the outputs for the ternary NAND and NOR gates, respectively.

Table 2. Ternary universal gates table

In_A	In_B	Y_{AND}	Y_{NOR}
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

Existing ternary NAND and NOR gate designs: The following figure shows the existing ternary NAND gate and NOR designs. The logical formulas for the ternary NAND and NOR gates are shown in Eqns. (7) and (8).

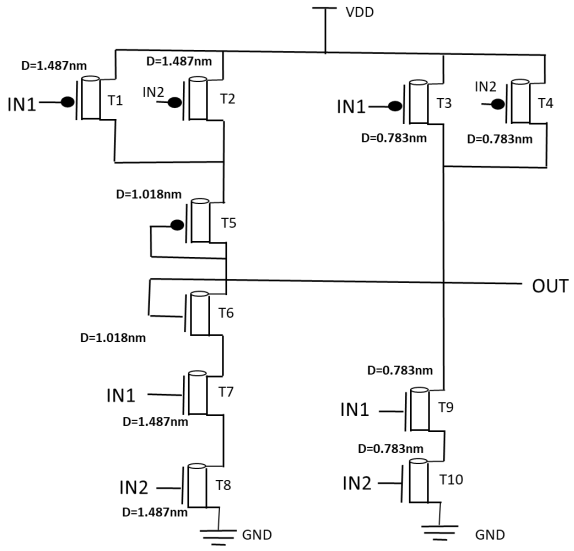

Fig. 4. Ternary NAND gate design [5].

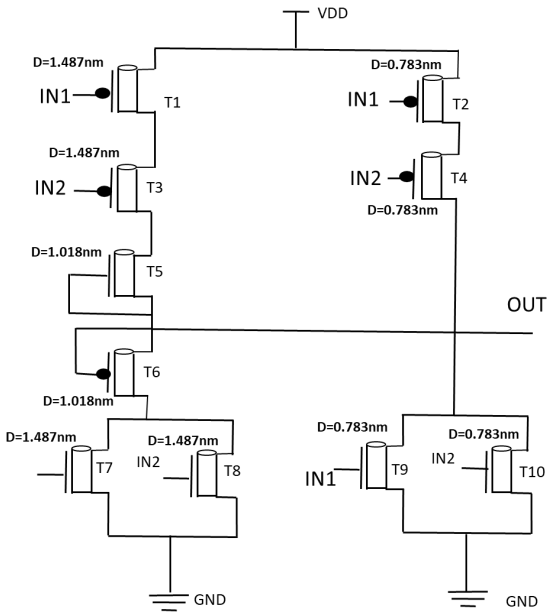

Fig. 5. Ternary NOR gate design [6]

Figures 4 and 5 show the two-input NAND and NOR gate designs from [5]. Comprising ten CNTFETs, each of these two gates combines three different chiralities. Their transistor threshold voltages vary only somewhat; functionally, they are almost exactly like traditional binary CMOS gates. Calculated with Eqn. (2), the matching threshold voltages – using transistor diameters of 1.487 nm, 0.683 nm, and 1.018 nm – are 0.289 V, 0.559 V, and 0.428 V, respectively. These values align

with those seen in the Standard Ternary Inverter (STI) circuit shown in Fig. 2. Using HSPICE simulations – as shown in Tab. 2 – the accuracy of these gate designs was verified.

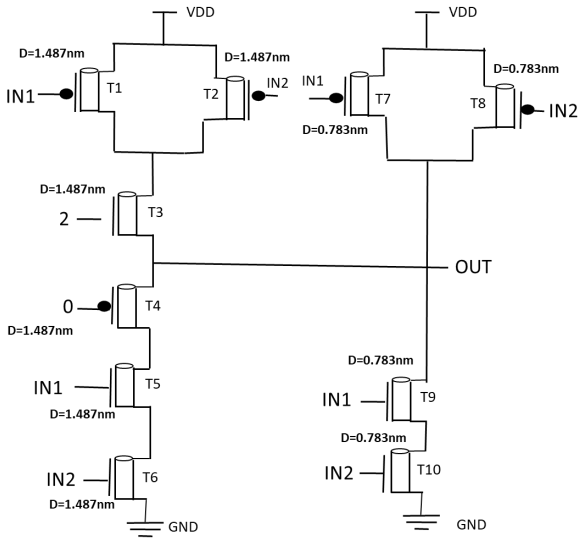

Fig. 6. Ternary NAND gate design [7]

Figure 6 shows the two-input ternary NAND gate design [7]. This design comprises a total of ten transistors, of which five are PCNTFET and five are NCNTFET with the chiralities of (19,0) and (10,0), and their diameters are 1.487 nm and 0.783 nm from Eqn. (1). The correctness of these designs was verified using HSPICE, as shown in Tab. 2.

Figure 7 [8] also comprises ten transistors with chiralities of transistors *T1, T3, T7, T8* considered (19,0) and a diameter of 1.487 nm from Eqn. (1). *T6* chirality is (13,0) with a diameter of 1.018 nm, and transistors *T2, T4, T5, T9*, and *T10* chiralities are (8,0) with a diameter of 0.626 nm, and design correctness has been verified in HSPICE according to Tab. 2.

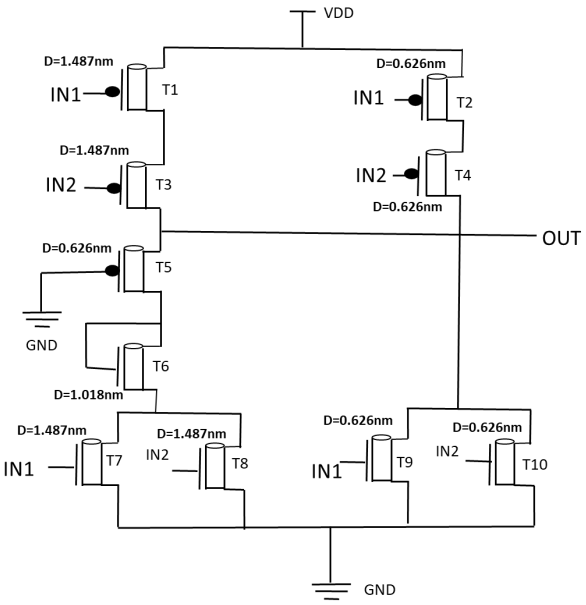

Fig. 7. Ternary NOR gate design [8]

3 Proposed standard ternary circuits

This section presents the proposed circuits, including the Standard Ternary Inverter and the ternary NAND and NOR gates, designed using the Stanford 32 nm CNTFET model. All existing and proposed designs have been simulated in same environment using the Synopsys HSPICE tool to ensure a fair and consistent comparison.

3.1 Proposed standard ternary inverter design

Figure 8 shows the proposed circuit of STI. This STI consists of four transistors, two of which are PCNTFET transistors, and the other two are NCNTFET transistors. *T1* and *T3* transistors are PCNTFET transistors with chiralities (7,0) and a diameter of 0.548 nm, and transistors *T2* and *T4* are NCNTFET transistors with chiralities (10,0) and a diameter of 0.783 nm.

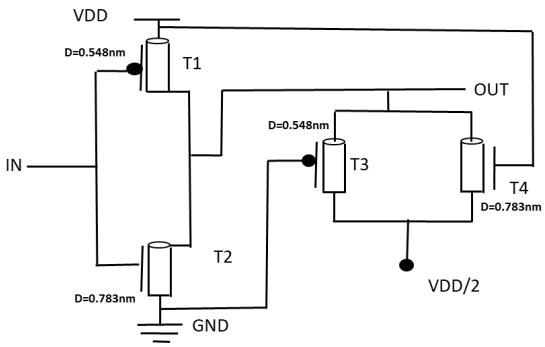

Fig. 8. Proposed standard ternary inverter

In this circuit, the T3 and T4 transistors work as a voltage divider. The circuit operates with three logic levels: logic ”0” (0 V), logic 1 = (V_{DD}/2=0.45 V), and logic ”2” = (V_{DD}=0.9 V), respectively.

3.2 Proposed ternary NAND and NOR gate designs

Figures 9 and 10 show the proposed ternary NAND and NOR gate designs. These circuits contain a total of six transistors: *T1, T2*, and *T5* are the PCNTFET transistors, and *T3, T4*, and *T6* are the NCNTFET transistors. These circuits contain a dual power supply where the *T5* and *T6* circuits function as a voltage divider. The chirality for PCNTFET (7,0) and diameter is 0.548 nm from Eqn. (1). The chirality for NCNTFET is (10,0), and the diameter is 0.783 nm, respectively. Since the circuit consists of a dual V_{DD} supply. The above figures operate with three logic levels: logic ”0” (0 V), logic ”1” = V_{DD}/2=0.45 V and logic ”2” = V_{DD}=0.9 V, respectively. The correctness of these circuits has been verified in HSPICE according to Tab. 2.

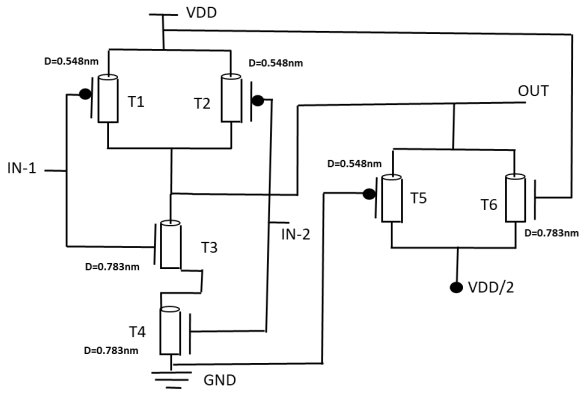

Fig. 9. Proposed ternary NAND gate design

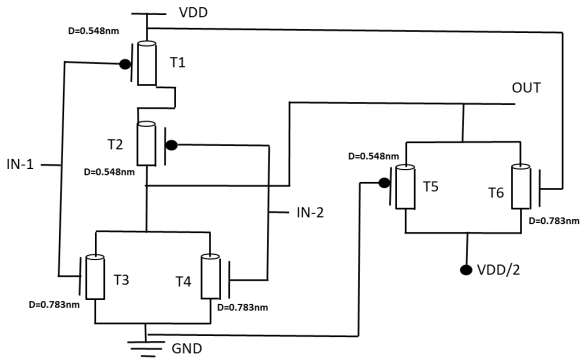

Fig. 10. Proposed ternary NOR gate design

4 Simulation results and analysis

In this section, all the circuits mentioned in sections 2 and 3 are tested using the Synopsis HSPICE simulation tool. With the 32 nm CNTFET Stanford model, the number of CNTs is 3, 1 with different chiralities, and input-output waveforms of ternary inverter and ternary universal gates are also present in this section.

4.1 Standard ternary inverter

Figure 11 shows that the transient analysis of the proposed design has been confirmed and tested. According to Tab. 3, the synopsis HSPICE simulation tool is used. The performance metrics, including delay, power consumption, power delay product, number of tubes, transistor count, and chiralities, are analyzed to evaluate the effectiveness of the ternary logic circuits.

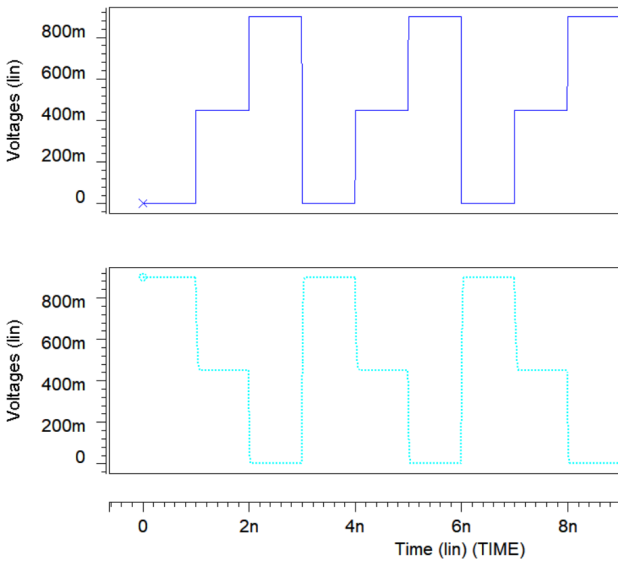

Fig. 11. Input and output waveforms of standard ternary inverter

Table 3. Simulation results of standard ternary inverters

Design	Avg. power (nW)	Delay (ps)	PDP (aJ)	Tran	Chiralities
[5]	166.6	774.92	129.62	6	19,13,10
[6]	93.17	993.73	92.54	6	19,10,13
Prop.	269.65	87.63	23.66	4	7,10

As seen above, among all the STI designs, the proposed design is clearly the best among all designs because it consumes less power, has the lowest delay, and has the lowest PDP. Hence, indicating the highest energy efficiency. Design [5] might be considered if higher power is acceptable for modest speed gain over [6]. Design [6] is the worst in all metrics – highest power, longest delay, and worst PDP. Design [6] is the worst in all metrics – highest power, longest delay, and worst PDP.

4.2 Ternary NAND gate

Figure 12 shows the transient analysis of the proposed ternary NAND gate circuit. The design has been confirmed and tested using the Synopsis HSPICE simulation tool. According to Tab. 4, the performance metrics, including delay, power consumption, and power delay product, number of tubes, transistor count, and chiralities, are analyzed to evaluate the effectiveness of the ternary logic circuits.

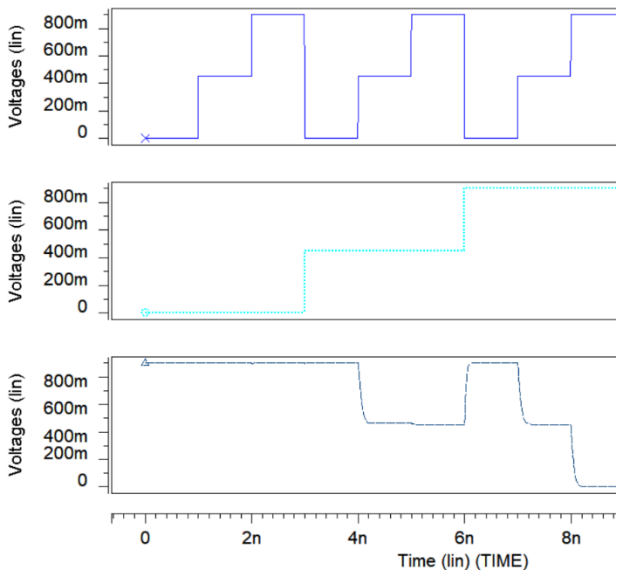

Fig. 12. Input and output waveforms of ternary NAND gate

Table 4. Simulation results of NAND gates designs

Design	Avg. power (nW)	Delay (ps)	PDP (aJ)	Tran	Chiralities
[5]	175.99	6503.6	1144.3	10	19,13,10
[6]	567.77	79322	45014	10	19,10
Prop.	86.31	6032.6	520.6	6	7,10

As seen below, among all designs of NAND gates, the proposed design is clearly the best among all designs because it consumes less power and has the lowest delay among all designs of NAND gates.

4.3 Ternary NOR gate

Figure 13 shows the transient analysis of the proposed ternary NOR gate circuit. The design has been confirmed and tested. According to Tab. 5, using the synopsis HSPICE simulation tool and performance metrics, including delay, power consumption, and power delay product, the number of tubes, transistor count, and also are given in Tab. 5.

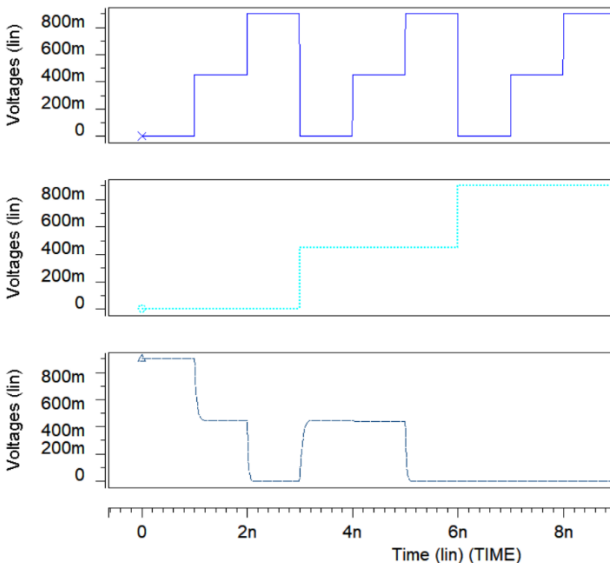

Fig. 13. Input and Output waveform of ternary NOR gate

Table 5. Simulation results of NOR gates designs

Design	Avg. power (nW)	Delay (ps)	PDP (aJ)	Tran	Chiralities
[5]	176.25	518.1	91.31	10	19,13,10
[6]	368.86	578.9	213.58	10	19,8,13
Prop.	32.01	76.37	2.44	6	7,10

As seen above, among all designs of NOR gates, the proposed design is clearly the best because it consumes less power, has the lowest delay, and lowest PDP, hence indicating the highest energy efficiency.

5 Conclusion

This paper examines standard ternary inverters and universal gates, focusing on performance factors such as area, average power, delay, and power-delay product. It proposed new circuits of standard ternary inverters and universal gates, detailing several methods we tested to determine which were most effective. For instance, we reduced the number of transistors and utilized dual source voltages (V_{DD} and $V_{DD}/2$). The proposed Standard Ternary Inverter indicating 33.33% improvement in area efficiency compared to the existing design. Similarly, the proposed ternary NAND and NOR circuits improve the area-efficiency by 40% compared to other designs. The simulation results also clearly indicate that the proposed designs consume less energy, power-delay product (PDP), and area efficiency as compared to the other existing designs.

6 Declaration

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References

[1] P. Saha, A. Jain, and S. Sarkar, "A comparative study of cmos and carbon nanotube field effect transistor based inverter at 32 nm technology node," Asian Journal of Chemistry, vol. 25, no. Supplementary Issue, p. S424, 2013.

[2] S. Ruhil, K. Rohilla, and J. Sehgal, "Cntfet based energy efficient full adder," 2015.

[3] S. Vidhyadharan and S. Vidhyadharan, "An ultra-low-power cnfet based dual vdd ternary dynamic half adder," Microelectronics Journal, vol. 107, p. 104961, 2021.

[4] F. Zahoor, F. A. Hussin, F. A. Khanday, M. R. Ahmad, and I. Mohd Nawi, "Ternary arithmetic logic unit design utilizing carbon nanotube field effect transistor (cntfet) and resistive random access memory (rram)," Micromachines, vol. 12, no. 11, p. 1288, 2021.

[5] S. Lin, Y.-B. Kim, and F. Lombardi, "Cntfet-based design of ternary logic gates and arithmetic circuits," IEEE transactions on nanotechnology, vol. 10, no. 2, pp. 217–225, 2009.

[6] M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nano-technology," IET Circuits, Devices & Systems, vol. 5, no. 4, pp. 285–296, 2011.

[7] S. Etezadi and S. A. Hosseini, "Novel ternary logic gates design in nanoelectronics," Advances in Electrical and Electronic Engineering, vol. 17, no. 3, p. 294, 2019.

[8] T. Khurshid and V. Singh, "Energy efficient design of unbalanced ternary logic gates and arithmetic circuits using cntfet," AEU-International Journal of Electronics and Communications, vol. 163, p. 154601, 2023.

[9] R. Martel, T. Schmidt, H. Shea, T. Hertel, and P. Avouris, "Single-and multi-wall carbon nanotube field-effect transistors," Applied physics letters, vol. 73, no. 17, pp. 2447–2449, 1998.

[10] N. Hamada, S.-i. Sawada, and A. Oshiyama, "New one-dimensional conductors: Graphitic microtubules," Physical review letters, vol. 68, no. 10, p. 1579, 1992.

[11] I. Hussain and S. Chaudhury, "A comparative study on the effects of technology nodes and logic styles for low power high speed vlsi applications," International Journal of Nanoparticles, vol. 12, no. 1-2, pp. 122–135, 2020.

[12] D. Bansal, B. C. Nagar, B. P. Singh, and A. Kumar, "A new keeper domino logic based full adder for high-speed arithmetic circuits," Micro and Nanosystems, vol. 13, no. 2, pp. 223–232, 2021.

[13] J. Deng and H.-S. P. Wong, "A compact spice model for carbon-nanotube field-effect transistors including nonidealities and its application—part i: Model of the intrinsic channel region," IEEE Transactions on Electron Devices, vol. 54, no. 12, pp. 3186–3194, 2007.

[14] A. Lin, G. Wan, J. Deng, and H. P. Wong, "A quick user guide on Stanford university carbon nanotube field effect transistors (cnfet) hspice model v. 2.2. 1," 2008.

[15] M. H. Moaiyeri, R. F. Mirzaee, A. Doostaregan, K. Navi, and O. Hashemipour, "A universal method for designing low-power carbon nanotube fet-based multiple-valued logic circuits," IET Computers & Digital Techniques, vol. 7, no. 4, pp. 167–181, 2013.

[16] A. Paul and B. Pradhan, "Cntfet-based design of ternary logic gates with interchangeable standard positive and negative ternary output," Engineering Research Express, vol. 3, no. 3, p. 035002, 2021.

[17] S. Lin, Y.-B. Kim, and F. Lombardi, "A novel cntfet-based ternary logic gate design," in 2009 52nd IEEE International Midwest Symposium on Circuits and Systems. IEEE, 2009, pp. 435–438.

[18] S. Tabrizchi, F. Sharifi, and A.-H. Badawy, "Energy efficient tri-state cnfet ternary logic gates," International Journal of Nanoscience, vol. 21, no. 04, p. 2250024, 2022.

[19] S. A. Ebrahimi, M. R. Reshadinezhad, A. Bohlooli, and M. Shahsavari, "Efficient cntfet-based design of quaternary logic gates and arithmetic circuits," Microelectronics Journal, vol. 53, pp. 156–166, 2016.

[20] H. Lee, H. Jang, J. Yun, H. Jin, J. Kim, Y. Kim, and T. Song, "Ternary competitive to binary: A novel implementation of ternary logic using depletion-mode and conventional mosfets," in 2022 IEEE 52nd International Symposium on Multiple-Valued Logic (ISMVL). IEEE, 2022, pp. 21–26.

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