

Electronically tunable multiplier-free floating memtranstor emulator employing VDTA and VDCC

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This work presents a compact floating configuration of the memtranstor (MT), a recently introduced memory element defined by the direct relationship between magnetic flux (ϕ) and charge (q). Unlike prior designs, the proposed emulator eliminates the need for multipliers or other complex circuitry, resulting in a simplified and power-efficient architecture. The circuit employs a single voltage differential transconductance amplifier (VDTA) and one voltage differential current conveyor (VDCC) as active devices, together with three grounded capacitors and one grounded electronic resistor as passive components. The emulator successfully reproduces the fundamental ϕ - q relationship and exhibits origin-crossing pinched hysteresis loops under sinusoidal excitation – a defining characteristic of memtransitive systems. It operates reliably at a supply voltage of ± 0.9 V and supports electronic tunability through adjustment of the VDTA and VDCC transconductance parameters), ensuring adaptability across a wide range of operating conditions. Extensive validation was carried out through mathematical modeling and LTSpice simulations based on a 180-nm CMOS process. The evaluation includes demonstration of memory effects, Monte Carlo analysis, temperature sensitivity studies, and characterization of pinched hysteresis loops under variations in DC control voltage, excitation frequency, and transconductance values. A full-custom layout was implemented, occupying a silicon area of 2529.49 μm^2 . Non-ideal effects, including parasitics at active device terminals, were also thoroughly analyzed to ensure functional robustness. Distinguished by its compact structure, low component count, and ease of integration, the proposed design provides a robust and efficient platform for MT-based applications. Its demonstrated performance highlights significant potential for neuromorphic computing, chaos-based systems, nonlinear dynamics, and other emerging analog memory-oriented domains.

Keywords: memtranstor, emulator circuits, VDTA, VDCC, pinched hysteresis loop, non-ideal circuits, simulation, layout

1 Introduction

Neuromorphic computing has emerged as a promising paradigm for next-generation information processing, enabling fast, energy-efficient, and low-power handling of complex data. In contrast to the conventional von Neumann architecture – which suffers from processor-memory bottlenecks due to the physical separation of computation and memory units – neuromorphic systems emulate the neural organization of the human brain, thereby facilitating more efficient execution of artificial intelligence (AI) algorithms [1]. The repetitive execution of simple operations on large datasets in machine learning imposes intensive processor-memory traffic, which significantly limits the efficiency of traditional computing approaches [1].

Neuromorphic architectures address this limitation by implementing artificial neural networks composed of numerous interconnected neurons and synapses that simultaneously compute and store information [2]. Data exchange is realized through these neural connections, enabling efficient execution of iterative machine learning training processes. A critical enabler of such architectures is the availability of circuit elements

capable of retaining information without continuous power supply. These elements provide energy-efficient storage and processing while mirroring biological principles, as the human brain inherently relies on adaptive memory components for learning and spontaneous behavior [3].

At the core of neuromorphic systems are memory elements – commonly referred to as *memelements* – which are nonlinear circuit components exhibiting memory-dependent behavior. Memelements extend the functional capabilities of circuits by establishing nonlinear correlations among fundamental variables [4]. Since their theoretical conception, memelements have been extensively investigated and implemented, resulting in devices that enhance circuit performance beyond the limitations of conventional linear elements. Among these, memristors, memcapacitors, and meminductors have garnered particular attention due to their potential applications in high-density, high-speed non-volatile memory, neuromorphic computing, adaptive filters, chaotic circuits, and hybrid analog-digital systems [5].

The memristor, introduced by Chua in 1971, represents the earliest and most widely studied memelement, derived from mathematical relationships between pairs of fundamental circuit variables [6]. Subsequent research expanded to include memcapacitors and meminductors, which were formally introduced by Chua and colleagues in 2009, opening new avenues for the design of nonlinear and chaotic circuits [4].

In a memelement system, any two complementary constitutive variables, denoted as $u(t)$ and $y(t)$, are typically defined as the input and output of the system, respectively, and expressed as follows [7]:

$$y(t) = g(x, u, t)u(t) \quad (1)$$

$$\frac{dx(t)}{dt} = f(x, u, t) \quad (2)$$

Here, f represents a vector-valued continuous function, g denotes the generalized response, and x corresponds to the state variables. The above mathematical formulations can be employed to describe different types of memelements as functions of their constitutive variables. The four principal nonlinear elements in this category are the memristor (MR), memcapacitor (MC), meminductor (ML), and memtranstor (MT). Furthermore, by defining the corresponding inverse mathematical relations, one can introduce the inverse impedance forms of these memelements, namely $M_R^{-1}, M_C^{-1}, M_L^{-1}, M_T^{-1}$. The memtranstor governs the relationship between electric charge (q) and magnetic flux (φ), and its constitutive relation is defined as follows:

$$\varphi(t) = M_T \left(\int_{t_0}^t q(\tau) d\tau \right) q(t) \quad (3)$$

In the flux-driven mode, the inverse memtranstance is expressed as follows:

$$M_T^{-1}(\rho(t)) = \frac{q(t)}{\varphi(t)} \quad (4)$$

Here, ρ represents the time integral of magnetic flux φ , defined as $\rho(t) = \int_{-\infty}^t \varphi(\tau) d\tau$. The σ - ρ constitutive relationship of the memtranstor emulator can be derived, as shown in [7], by constructing the emulator based on a second-order dependence between charge and flux.

$$\sigma(\rho) = \frac{1}{2}A\rho^2 + B\rho \quad (5)$$

$$M_T^{-1} = \frac{d\sigma(\rho)}{d\rho} = A\rho + B \quad (6)$$

where $\sigma(t) = \int_{-\infty}^t q(\tau) d\tau$. The initial value of M_T^{-1} is denoted by B , and the rate of change by A .

The memtranstor operates based on the magneto-electric (ME) effect, which enables coupling between magnetic and electric properties. Unlike conventional memelements, typically defined via voltage-current or voltage-charge relationships, the memtranstor is

uniquely characterized by a direct constitutive relationship between electric charge (q) and magnetic flux (φ). Consequently, it is described in terms of φ and q rather than voltage and current. This distinct formulation gives rise to characteristic behaviors, such as pinched hysteresis loops (PHLs) in the φ - q plane. Depending on the input conditions, these loops may occupy different quadrants and exhibit shapes resembling a slanted figure “8” or a butterfly.

Although the memtranstor and memristor share the same dimensional units of ohms, they belong to fundamentally different classes of devices, with distinct physical mechanisms and constitutive relationships. The memtranstor can be considered the memory counterpart of the transtor, a “fourth” fundamental circuit element introduced by S. D. Shan et al. [8], alongside the resistor, capacitor, and inductor. While the transtor performs linear bidirectional conversion between q and φ , the memtranstor incorporates memory functionality via intrinsic ME coupling, resulting in a nonlinear charge–flux relationship that cannot be realized through conventional voltage-current interactions.

This unique property enables a range of novel applications. For example, a four-terminal current converter can be implemented using two transtors in a longitudinal configuration, leveraging ME-mediated interactions between electric and magnetic domains [8]. Similarly, the axial nature of the memtranstor facilitates gyrator design, where the voltage at one port is proportional to the current at the opposite port. Furthermore, its ME effect allows the development of next-generation non-volatile devices, including nonvolatile random-access memory and logic gates [9].

Recent studies have highlighted the potential of memtranstors for neuromorphic and nonlinear applications. They have been employed to emulate synaptic behaviors, including long-term potentiation, long-term depression, and spike-timing-dependent plasticity in artificial neural networks [7, 10], as well as for the implementation of chaotic oscillators [11, 12]. Despite their promise, large-scale commercial fabrication of memelements remains challenging and costly due to technological and material constraints [5]. To address these limitations, significant research has focused on the development of emulator circuits capable of replicating memelement behavior in a more practical and integrable form. Accordingly, a variety of emulator circuits have been reported in the literature, including memristor emulators [13–18], memcapacitor emulators [16, 18, 19], and meminductor emulators [20, 21], realized using diverse active device configurations.

Memtranstors, the latest addition to the memelements family, integrate functional attributes of memristors, memcapacitors, and meminductors into a single multi-functional device. Their unique advantages – such as

intrinsic nonvolatile switching, parallel readout capability, and improved isolation compared to memristors – enable reduced power consumption and enhanced data storage and signal-processing performance reminiscent of conventional transistors [10, 22, 23]. Moreover, memtransistors can be configured to operate in discrete two-state modes suitable for nonvolatile memory and logic applications, or in continuously variable modes that emulate artificial synapses [10, 24–26]. These characteristics, particularly high-density integration and low-power operation, position memtransistors as strong candidates for next-generation electronic circuits. While sharing the nonvolatility and programmability inherent to other memelements [13–21], memtransistors offer more convenient operation and lower energy consumption.

Despite extensive investigations into the nonlinear dynamics of memristors, memcapacitors, and meminductors, the dynamic behavior of memtransistors remains comparatively underexplored. This lack of systematic study could limit their application in low-power circuit design and nonlinear system analysis, underscoring the need for further research.

The memtransistor operates based on the magnetoelectric (ME) effect, in which a material's electrical properties are modulated by an applied magnetic field [10, 24]. This effect establishes a direct correlation between charge (q) and magnetic flux (ϕ), defining memtransistor behavior [25, 26]. Several studies have demonstrated physical realizations of memtransistors. For example, Shen et al. reported memtransistive behavior at ambient temperature in a magnetoelectric hexaferrite device ($\text{Ba}_{0.5}\text{Sr}_{1.5}\text{Co}_2\text{Fe}_{11}\text{AlO}_{22}$), where electric polarization could be modulated by an external magnetic field, resulting in a nonlinear q - ϕ relationship with a butterfly-shaped hysteresis loop [25]. Furthermore, Shen and colleagues demonstrated that memtransistors can simultaneously perform memory and logic operations. Using a Ni/PMN-PT/Ni heterostructure, they implemented NOR and NAND logic gates as well as multi-level nonvolatile memory, highlighting the potential of memtransistors to unify memory and logic within a single device and transcend the limitations of the von Neumann architecture [9].

Realizing physical memtransistors remains highly challenging, as they require a specialized nonlinear magnetoelectric effect with intrinsic memory characteristics. To address these limitations, emulator circuits have been developed to replicate the pinched hysteresis loops that define memtransistive behavior. To date, only a few memtransistor emulators suitable for integrated circuit implementation have been reported.

The first emulator, proposed by Zheng et al. [7], employed four current feedback operational amplifiers (CFOAs), two operational amplifiers (Op-Amps), an analog multiplier (AM), three capacitors, and five resistors. While functional, this design suffered from high component count, elevated power consumption due to op-amp reliance, and bandwidth limitations inherent to op-amp-based circuits. Subsequently, Sagbas et al. [12] introduced an emulator using four differential voltage current conveyors (DVCCs), an AM, three grounded capacitors, and four grounded resistors. Although more efficient in some respects, this design lacked electronic tunability, relied on an external voltage source, and depended heavily on resistors, reducing integration feasibility.

A more recent design [11] utilized three operational transconductance amplifiers (OTAs), one dual-output current conveyor (DOCCII), an AM, three capacitors, and one resistor. Compared with [7], this approach required fewer components, eliminated op-amps, and provided tunability, yet the overall component count remained relatively high. Another alternative [27] employed OTAs with a simpler internal structure than the DVCCs in [12], reducing power consumption, silicon area, and resistor usage, while enabling a CMOS implementation with fewer transistors and smaller process parameters, thereby improving efficiency relative to both [7] and [12]. The most recent work [28] presents a compact, multiplier-free memtransistor emulator using only one OTA, a CDTA, and a VDCC, successfully reproducing the essential ϕ - q memtransistive characteristics in a practical and integration-friendly form. Reference [29] presents an early CCII-based memtransistor emulator validated through PSPICE simulations and experimental measurements using commercial integrated circuits, thereby demonstrating the practical feasibility of memtransistive behavior for neuromorphic computing applications.

The proposed design adopts a voltage differencing transconductance amplifier (VDTA) and a voltage differencing current conveyor (VDCC) as the active building blocks (ABBs), together with three grounded capacitors and one grounded electronic resistor. Both ABBs are based on differential amplifier or translinear loop principles, feature symmetric biasing, and maintain a simple architecture. In contrast, multipliers exhibit more complex structures with asymmetric biasing and are prone to non-idealities such as offset voltages, which – if uncompensated – can shift the pinch-off point and introduce asymmetry in the pinched hysteresis loop (PHL) curves. By eliminating multipliers, the proposed circuit achieves a more symmetric, compact, and simplified implementation, enhancing its suitability for practical integrated designs.

The advantages of the proposed floating memtranstor emulator over previously reported designs can be summarized as follows:

- It utilizes fewer active devices and significantly fewer transistors compared to [11, 12, 27, 28], enabling a more compact implementation.
- By eliminating operational amplifiers, it avoids the bandwidth limitations at higher gains associated with the fixed gain-bandwidth product of op-amps.
- It achieves lower power consumption and reduced silicon area relative to [7, 11, 12, 27, 28], due to the use of active components with smaller CMOS process parameters, operation at lower supply voltages, and support for a wider frequency range than [28].
- It provides enhanced electronic tunability compared with [28] while removing the dependence on resistors, thereby improving compatibility with integrated circuit (IC) technology.

The remainder of this paper is organized as follows. Section 2 presents the theoretical foundations of the memtranstor and details the proposed floating emulator circuit, including its operational principles. Section 3 examines the influence of parasitic impedances on circuit performance. Section 4 provides comprehensive LTSpice simulation results, encompassing analyses of pinched hysteresis loops, electronic tunability, and Monte Carlo evaluation. Finally, Section 5 concludes the paper by summarizing the main contributions and outlining potential directions for future research.

2 Proposed configuration

Figure 1 depicts the proposed configurations of the emulator circuits for floating decremental and incremental memtranstors.

The memtranstor shown in Fig. 1 utilizes a single VDTA and VDCC, along with three capacitors and one electronically controlled resistor. Equation (7) describes the current-voltage relationships among the various terminals of the Voltage Differencing Transconductance Amplifier (VDTA).

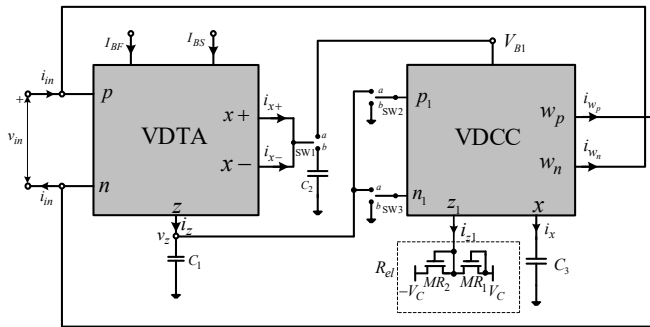
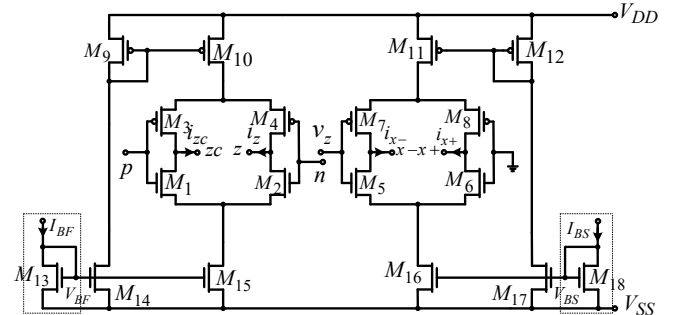


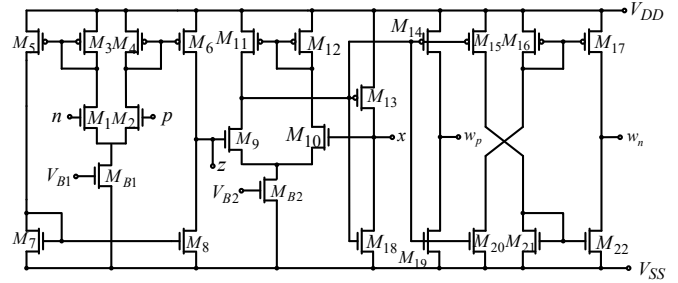
Fig. 1. Floating memtranstor emulator circuits based on VDTA and VDCC

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \beta_S g_{mS} \\ 0 & 0 & -\beta_S g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad (7)$$

The transconductance gains of the Voltage Differencing Transconductance Amplifier (VDTA), denoted as g_{mF} and g_{mS} , are electronically controlled via biasing voltages or currents. These gains are determined by the tracking errors of the first and second VDTA stages, represented by β_F and β_S , respectively. In practice, these parameters can be considered non-ideal transconductance gains, typically ranging from 0.9 to 1, with an ideal value of 1. The VDTA can be modeled as a cascade of two stages: a differential-input, single-output (DISO) operational transconductance amplifier (OTA) followed by a single-input, dual-output (SIDO) OTA. This two-stage characterization, together with the CMOS implementation illustrated in Fig. 2(a), provides a clear representation of the VDTA's equivalent structure.



(a)



(b)

Fig. 2. (a) CMOS implementation of VDTA, (b) CMOS implementation of VDCC

The CMOS implementation of the Voltage Differencing Transconductance Amplifier (VDTA) is illustrated in Fig. 2(a). This design integrates two Arbel-Goldminz (AG) transconductance cells. In this configuration, the transconductance gains, g_{mF} and g_{mS} , are mainly governed by the transconductance of the output transistors. These gains can be reasonably approximated as follows:

$$\begin{aligned} g_{mF} &\cong \left(\frac{g_1 g_2}{g_1 + g_2} \right) + \left(\frac{g_3 g_4}{g_3 + g_4} \right) \\ g_{mS} &\cong \left(\frac{g_5 g_6}{g_5 + g_6} \right) + \left(\frac{g_7 g_8}{g_7 + g_8} \right) \end{aligned} \quad (8)$$

$$g_i = \sqrt{\mu_i C_{ox} W_i I_{BF} (I_{BS}) / L_i}, i = 1, \dots, 8 \quad (9)$$

In the preceding equation, μ denotes the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are the effective channel width and length of the i -th MOS transistor, and K_i represents the gain factor of the Arbel-Goldminz (AG) transconductance cells. Notably, the AG cells used in this configuration do not introduce additional imperfections in voltage or current gain, in contrast to other active blocks such as current conveyors, which are often limited by slew rate, bandwidth, and dynamic range.

The VDTA based on AG cells can drive a grounded load with a bipolar signal while maintaining a feedback current that closely matches the output current across a wide frequency range. The temperature dependence of the VDTA is primarily governed by the temperature dependence of its transconductance g_m . Specifically, the threshold voltage (V_T) exhibits an approximate change of -2.4 mV/°C, decreasing by roughly 0.24% with increasing temperature. The carrier mobility follows the relation $\mu(T) = \mu(T_0)(T/T_0)^{-1/5}$, which decreases by approximately 1.5% with temperature. Consequently, the decrease in mobility dominates the variation in g_{mF} and g_{mS} , leading to a reduction in transconductance as temperature increases.

The terminal behavior of the Voltage Differencing Current Conveyor (VDCC) can be described using a hybrid matrix, as defined in (10).

$$\begin{bmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_{w_p} \\ i_{w_n} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 & 0 \\ 0 & 0 & \gamma & 0 \\ 0 & 0 & 0 & \alpha_p \\ 0 & 0 & 0 & -\alpha_n \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \end{bmatrix} \quad (10)$$

The VDCC (Fig. 2(b)) exhibits high impedance at all terminals except the x -terminal. In this framework, β represents the tracking error of the OTA stage, with an ideal value of 1. The non-ideal voltage gain between the z and x terminals is denoted by γ , which also ideally equals 1. Similarly, α_p and α_n correspond to the non-ideal current gains between the x , w_p , and w_n terminals, respectively, with their ideal values being 1. The transconductance gain of the VDCC is expressed as follows:

$$g_m = k(V_{B1} - V_{Tn} - V_{SS}) \quad (11)$$

where

$$k = B\mu_{nB}C_{oxB}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_{MB1}\left(\frac{W}{L}\right)_{MN}} \quad (12)$$

The transistor aspect ratio $(W/L)_{MN}$ is defined such that $(W/L)_{M1} = (W/L)_{M2}$, while the current mirroring ratio among transistors M_3 , M_4 , M_5 , and M_6 is denoted by B . Furthermore, μ_{nB} and C_{oxB} represent the electron mobility

and the oxide gate capacitance per unit area of the M_{B1} transistor, respectively. From (11), it can be inferred that the p , n , and z terminals operate as a transconductance amplifier, whereas the other ports (x , w_p , and w_n) – including the output z from the first stage – are interconnected with the internal current conveyor stage. Both stages can be implemented using CMOS technology, as illustrated in Fig. 2(b), requiring a total of 24 MOS transistors.

The equivalent resistance R_{el} , realized through two p-MOS transistors (Fig. 1), is connected between the selected node of the VDCC and ground. This resistance can be electronically tuned by means of a control voltage (V_c), and its relationship is expressed as follows:

$$R_{el} = \frac{1}{2\mu_p C_{ox}(V_c - V_{Tp})} \left(\frac{1}{(W/L)_{MR}} \right) \quad (13)$$

The $(W/L)_{MR}$ ratio is defined such that $(W/L)_{MR1} = (W/L)_{MR2}$. In the high-frequency region, MOS capacitances can be employed in the emulator circuits in place of the grounded capacitors shown in Fig. 1. This substitution provides additional advantages for integrated circuit implementation.

The configuration illustrated in Fig. 1 shows that voltages V_{y1} (V_{y2}) are determined by the voltage across the capacitance C_1 (the following equations are obtained from a straightforward analysis of the circuit in Fig. 1). Based on the relationship defined in Eqn. (7), the expression for the voltage across the external capacitor C_1 can be derived as follows:

$$v_{C_1}(t) = v_z(t) = \frac{\beta_F g_{mF}}{C_1} \int v_{in}(t) dt = \frac{\beta_F g_{mF}}{C_1} \phi_{in}(t) \quad (14)$$

In the given equation, $\phi_{in}(t)$ denotes the flux associated with the input voltage signal. The voltage v_{C1} is determined by the output currents of the VDTA.

$$i_{x+}(t)(i_{x-}(t)) = g_{mS} v_{C_1}(t) = \pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1} \phi_{in}(t) \quad (15)$$

Consequently, the voltage across capacitor C_2 can be expressed as:

$$\begin{aligned} v_{C_2}(t) &= \pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1 C_2} \int \phi_{in}(t) dt = \\ &= \pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1 C_2} \rho_{in}(t) = V_{B1} \end{aligned} \quad (16)$$

The integral of the flux, denoted as $\rho_{in}(t)$, appears in the equation. Equation (11) indicates that the voltage V_{B1} governs the transconductance g_m of the VDCC.

$$g_m(t) = k \left[\pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1 C_2} \rho_{in}(t) - V_{SS} - V_{Tn} \right] \quad (17)$$

From the analysis of the circuits shown in Fig. 1, and considering the functional relationships among the VDCC ports, the following conclusions can be drawn:

$$\begin{aligned} i_{W_p} &= -i_{W_n} = \alpha_p i_x = \pm i_{in} \Rightarrow v_x(t) = \\ &= \pm \frac{1}{\alpha_p(\alpha_n)C_3} \int i_{in}(t)dt = \pm \frac{1}{\alpha_p(\alpha_n)C_3} q_{in}(t) \end{aligned} \quad (18)$$

where $q_{in}(t)$ is charge of the input current signal. Consequently, the voltage on the resistance R_{eq} is defined as

$$\begin{aligned} v_{z1} &= R_{el} i_{z1} = \frac{v_x}{\gamma} = \pm \frac{1}{\alpha_p(\alpha_n)\gamma C_3} q(t) = \\ &= \beta k R_{el} (V_{B1}(t) - V_{Tn} - V_{SS}) (v_{y1} - v_{y2}) = \\ &= \pm \beta k R_{el} (V_{B1}(t) - V_{Tn} - V_{SS}) v_{c1}(t) \end{aligned} \quad (19)$$

Finally, it follows that the following relationship can be established:

$$\begin{aligned} v_{z1} &= \pm \frac{1}{\alpha_p(\alpha_n)\gamma C_3} q_{in}(t) = \\ &= \pm \beta k R_{el} \frac{\beta_F g_{mF}}{C_1} \times \\ &\times \left(\pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1 C_2} \rho_{in}(t) - V_{Tn} - V_{SS} \right) \varphi_{in}(t) \end{aligned} \quad (20)$$

Hence, the formula for calculating the inverse memtranstance in flux-driven mode is given by:

$$\begin{aligned} M_T^{-1} &= \frac{q_{in}(t)}{\varphi_{in}(t)} = \pm \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p(\alpha_n) \gamma C_3}{C_1} \times \\ &\times \left(\pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{C_1 C_2} \rho_{in}(t) - V_{Tn} - V_{SS} \right) = \\ &= A \rho_{in}(t) + B \end{aligned} \quad (21)$$

A represents the variable gain component of the inverse memtranstance, while B denotes its fixed gain component. These can be calculated as:

$$A = \pm \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p(\alpha_n) \gamma C_3 \beta_F \beta_S g_{mF} g_{mS}}{C_1^2 C_2} \quad (22)$$

$$B = \pm \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p(\alpha_n) \gamma C_3}{C_1} (V_{Tn} + V_{SS}) \quad (23)$$

The fixed and variable components of the memtranstor may take either positive or negative values, depending on the position of the switches. To evaluate the performance of the memtranstor emulator in the frequency domain, a sinusoidal voltage is applied to its input ports. By selecting the input voltage as $v_{in} = V_m \sin \omega t$, $\rho_{in}(t)$ can be determined as given in (21), where V_m and ω represent the amplitude (in volts) and angular frequency (in radians per second) of the input voltage signal, respectively.

$$\varphi_{in} = \int v_{in} d\tau = -\frac{V_m}{\omega} (\cos \omega t) \quad (24)$$

$$\rho_{in} = \int \varphi_{in} d\tau = -\frac{V_m}{\omega^2} (\sin \omega t) \quad (25)$$

Substituting Eqn. (25) into Eqn. (21), we obtain:

$$\begin{aligned} M_T^{-1} &= \mp \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p(\alpha_n) \gamma C_3 \beta_F \beta_S g_{mF} g_{mS}}{C_1^2 C_2} \frac{V_m}{\omega^2} (\sin \omega t) \\ &\mp \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p(\alpha_n) \gamma C_3}{C_1} (V_{Tn} + V_{SS}) \end{aligned} \quad (26)$$

The inverse memtranstance in Eqn. (26) consist of both fixed and time-varying components. Analysis of the equations reveals that the variable component is inversely proportional to the capacitance values C_1 and C_2 , as well as the input frequency ($\omega = 2\pi f$), while it is directly proportional to the capacitance C_3 , the resistance R_{el} , and the amplitude of the input signal v_{in} . With increasing frequency, the contribution of the variable component diminishes, and the emulator circuit progressively approximates the behavior of a linear resistor. The ratio of the peak magnitudes of the two terms is calculated as follows:

$$\begin{aligned} \lambda &= \frac{\text{Variable part}}{\text{Fixed part}} = \pm \frac{\beta_F \beta_S g_{mF} g_{mS} V_m}{C_1 C_2 (V_{Tn} + V_{SS}) \omega^2} = \\ &= \pm \frac{1}{\tau f} = \pm \frac{T}{\tau} \end{aligned} \quad (27)$$

where T and τ denote the period and time constant of the proposed circuit, respectively. Accordingly, the time constant of the proposed emulator can be expressed as:

$$\tau = \frac{C_1 C_2 (V_{Tn} + V_{SS}) 4\pi^2}{\beta_F \beta_S g_{mF} g_{mS} V_m} \quad (28)$$

The time constant must be adjusted in accordance with Eqn. (28) to ensure the proper operation of the proposed memtranstor. This adjustment can be accomplished by varying the values of C_1 , C_2 , the threshold and supply voltages (V_{Tn} and V_{SS}), and/or the input amplitude (V_m). For correct operation of the proposed emulator circuit, the input voltage amplitude must be maintained at a constant level.

3 Non-ideal and parasitic analysis

In practical implementations, the VDTA and VDCC exhibit non-ideal gains, commonly referred to as tracking errors, as discussed in the previous section. These tracking factors remain approximately constant and independent of frequency within the low- to medium-frequency ranges. Analysis of the relationship in Eqn. (21) indicates that the proposed designs demonstrate low sensitivity, with normalized passive and active sensitivities equal to or less than unity. Therefore, the

proposed circuits are characterized by low passive and active sensitivities.

Considering the influence of parasitic components, i.e., the parasitic impedances at the input and outputs of the VDTA and VDCC, it becomes possible to investigate the performance of the proposed simulators in high-frequency environments. Parasitic resistances and capacitances are present in parallel with the corresponding terminals (p , n , z , $x+$ and $x-$) of the VDTA and (p , n , z_1 , w_p and w_n) of the VDCC, whereas at port x , a parasitic resistance R_x and parasitic inductance L_x appear in series (in an ideal VDCC, R_x and L_x are approximately zero). In ideal VDTA and VDCC devices, the parasitic parallel resistances approach infinity, and the parasitic capacitances approach zero. In practical implementations, however, they manifest as shunt R - C and series R - L networks in conjunction with external circuit elements. Specifically, all terminals exhibit shunt R - C parasitics in combination with the external circuitry.

By accounting for the influence of these parasitic components, the operation of the proposed memtransistor emulator can be analyzed in high-frequency environments. At sufficiently high frequencies, the effects of R_z , R_{x+} , R_{x-} , R_{wn} , R_{wp} , R_p , R_{z1} , L_x and R_n can be neglected. Therefore, considering the influence of these parasitic elements, we can conclude that:

$$M_T^{-1} = \pm \frac{\beta k R_{el} \beta_F g_{mF} \alpha_p (\alpha_n) \gamma (C_3 + C_x)}{(C_1 + C_z)} \left[\left(\pm \frac{\beta_F \beta_S g_{mF} g_{mS}}{(C_1 + C_z)(C_2 + C_{x+}(C_{x-}))} \rho_{in}(t) - V_{Tn} - V_{SS} \right) + \frac{R_x}{\tau_{in}} \right] \quad (29)$$

where τ_{in} is the time constant of the input port of the proposed emulator circuit $\tau_{in} = R_{in} C_{in}$.

By examining the proposed emulator in Fig. 1, including the incorporated parasitic elements, the following steps can be taken to determine the constraints on the component values. First, to account for the effect of parasitic elements on the resistor R_{el} at the z_1 terminal of the VDCC, the condition $R_{z1} \ll R_{el}$ must be satisfied. To minimize the influence of the parasitic resistance R_{z1} , R_{el} should be at least ten times larger than R_{z1} , that is, the resistance of the equivalent electronically controlled resistor must exceed the series resistance of the z_1 port. Second, the configuration of capacitors C_1 , C_2 , and C_3 is considered. Capacitors C_1 and C_2 are connected to the z and $x+/x-$ terminals of the VDTA. According to the VDTA parasitic impedance model, parasitic capacitances at these terminals are grounded and appear in parallel. To reduce the impact of these parasitic effects, the values of C_1 and C_2 should be at least ten times greater than the corresponding parasitic capacitances. Based on the derived relations (17-19), selecting C_1 and C_2 with values several times larger than the parasitic

capacitances ensures effective absorption of parasitic effects at the operating frequencies. Finally, the selection of capacitor C_3 is critical to minimizing parasitic effects. C_3 is connected to the x terminal of the VDCC, which, according to the parasitic impedance model, includes a series parasitic resistance R_x and inductance L_x . If C_3 is too small, it may act as an open circuit at certain input frequencies, causing the output current at the x terminal to approach zero. Conversely, if C_3 is too large, the current may increase excessively, potentially exceeding the linear limits of the x terminal. Therefore, to mitigate the impact of parasitic resistances, the values of C_1 , C_2 , and C_3 should be chosen such that their equivalent impedances are several times smaller than the parasitic resistances of the respective terminals.

Furthermore, it is important to note that the transconductance of the OTA cells in both the VDTA and VDCC is frequency-dependent and can be adequately modeled by a single-pole approximation. Accordingly, the transconductance gain and the parameter K of the first stage of the VDCC and both stages of the VDTA can be defined as follows:

$$g_m = g_{m0} \frac{\omega_g}{(s + \omega_g)}; k = k_0 \frac{\omega_k}{(s + \omega_k)} \quad (30)$$

In the presented equations, the transconductance gain is denoted by g_{m0} , and the gain factor of the OTA cell at zero frequency is represented as k_0 . The pole frequencies, $\omega_g = 1/\tau_g$ and $\omega_k = 1/\tau_k$, correspond to the respective time constants τ_g and τ_k , and characterize the bandwidth limitations of the system. By substituting the values of g_m and k into Eqns. (17-19), a more comprehensive understanding of the frequency-dependent behavior of the emulators can be obtained, including their sensitivity to non-idealities.

It is evident that the emulators shown in Fig. 1 exhibit a useful operating frequency range defined by $\omega \ll \min(\omega_g, \omega_k)$. The exact values of these pole frequencies, as given in Eqn. (20), depend on the practical implementation of the VDTA and VDCC. To enhance the bandwidth of the VDTA and VDCC, a compensating resistor R can be introduced at port p . This adjustment modifies the transconductance gain, yielding a new value given by $g_m = g_{m0}/(1 + g_{m0}R)$. Consequently, the bandwidth of the OTA cells – including both stages of the VDTA and the first stage of the VDCC – can be tuned accordingly.

4 Simulation results

The VDTA- and VDCC-based memtransistor emulator was simulated using HSPICE, with its operating performance evaluated using Level 49 TSMC CMOS 0.18 μm process model parameters. The DC supply

voltages and V_{B2} of the circuit were set to ± 0.9 V and 0 V, respectively.

The MOS transistor aspect ratios were chosen as follows: 16.1/0.7 for M_1, M_2, M_5, M_6 , 3.6/0.36 for M_3, M_4, M_7, M_8 , 16.64/0.36 for M_9-M_{12} , 3.6/0.36 for M_{13}, M_{18} , 4.5/0.36 for $M_{14}-M_{17}$. For a bias current of $I_{BF}=I_{BS}=160$ μ A, the small-signal transconductance was $g_{mF}=g_{mS}=810$ μ A/V. Key DC and AC parameters of the proposed VDTA circuits (Fig. 2(a)), including the obtained port parasitic impedances, are summarized in Tab. 1. The DC and AC transfer characteristics are illustrated in Fig. 3. The DC characteristics depict the variation of i_{x+} and i_{x-} with respect to v_z , while the AC characteristics show the variation of the transconductance gain g_{mF} as a function of frequency. Simulation results indicate that the transconductance gain decreases by 3 dB at 2.163 GHz. Based on the derived relation (29) and the analysis of parasitic impedances and other nonidealities presented earlier, the implemented VDTA circuit is expected to operate reliably at frequencies up to 500 MHz. This performance is also maintained with the passive element values used in the subsequent simulation tests, as they do not significantly degrade the impedance levels at the VDTA ports. It is evident that the adjustment of $g_m(I_B)$ has a significant effect on the resulting circuit parameters.

Table 1. DC and AC parameters of VDTA for two particular values of bias-control current

Parameter	Value for $I_{BF}=I_{BS}=10$ μ A	Value for $I_{BF}=I_{BS}=100$ μ A
p and n DC resistance $R_p=R_n$	>1 G Ω	>1 G Ω
z output dc resistance R_z	2.46 M Ω	368 k Ω
$x+$ and $x-$ output dc resistance, $R_{x+}=R_{x-}$	1.33 M Ω	462 k Ω
p and n input capacitance $C_p=C_n$	11 fF	11 fF
$x+$ and $x-$ output capacitance $C_{x+}=C_{x-}$	16 fF	16 fF
z output capacitance C_z	26 fF	26 fF
3dB attenuation for transfer from p input to z output $K_{-3dB}(p \rightarrow z)$	>1 GHz	>1 GHz
transconductance of first and second OTA, $g_{mF}=g_{mS}$	270 μ S	512 μ S
corner frequency ω_F, ω_S	5.6 rad/s	7.3 rad/s

The bulk terminals of the PMOS and NMOS transistors are connected to their respective source terminals and the most negative voltage node (V_{SS}). The aspect ratios of the VDCC transistors (Fig. 2(b)) were selected as follows: 3.6/1.8 for M_1-M_4 , 7.2/1.8 for M_5-M_6 , 2.4/1.8 for M_7-M_8 , 3.06/0.72 for M_9, M_{10} , 9/0.72 for M_{11}, M_{12} , 14.4/0.72 for $M_{13}-M_{17}$, 0.72/0.72 for $M_{18}-M_{22}$, while M_{B1}, M_{B2}, MR_1 , and MR_2 were chosen as 3.6 μ m/1.8 μ m, 3.06 μ m/0.72 μ m, 60 μ m/2 μ m, and 60 μ m/2 μ m, respectively. An electronically controlled resistor, implemented using only two PMOS transistors, can be tuned via a control voltage. For a control voltage of 0.65 V, the equivalent resistance is $R_{el}=1.47$ k Ω .

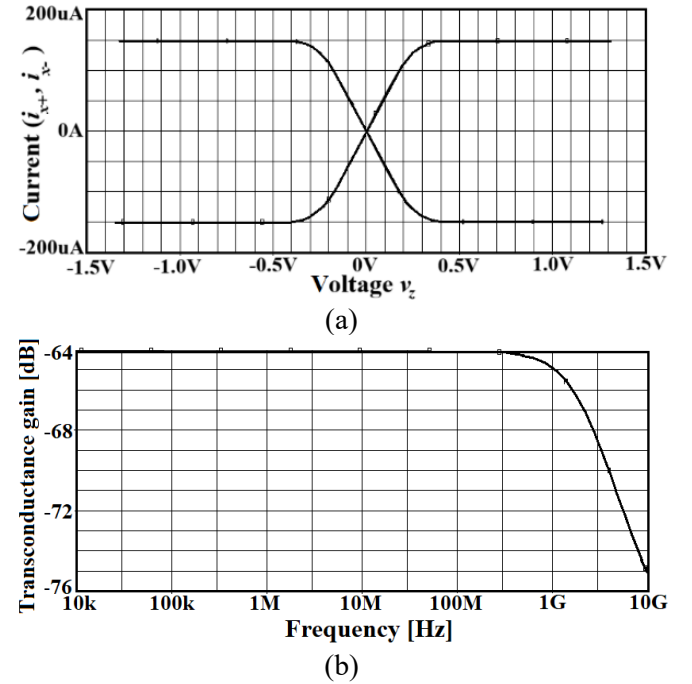


Fig. 3. (a) DC characteristics of VDTA, (b) AC characteristics of VDTA

The frequency response of the VDCC, including the current transfer gain, the transconductance gain tracking error, and the voltage transfer gain, is shown in Figs. 4(a) and 4(b). Simulation results indicate that the transfer gains remain approximately constant up to 100 MHz.

Key DC and AC parameters of the implemented VDCC, including the obtained port parasitic impedances, are summarized in Tab. 2. The bias voltage ranges from -0.4 V to -0.1 V, within this range, the VDCC maintains the defined operating characteristics. The power consumption of the proposed emulator circuits is 0.83 mW.

To investigate the dynamic behavior of the proposed memtransistor emulator, transient simulations were conducted using a sinusoidal input signal with an amplitude of 100 mV and a frequency of 1 kHz. The passive components were selected as $C_1=C_3=2$ nF and $C_2=2.5$ μ F. For this analysis, the switch SW1 in Fig. 1 was set to position *a*. The voltage waveforms across C_1 (representative of magnetic flux, ϕ) and C_3 (representative of charge, q) were examined to evaluate the flux-charge relationship.

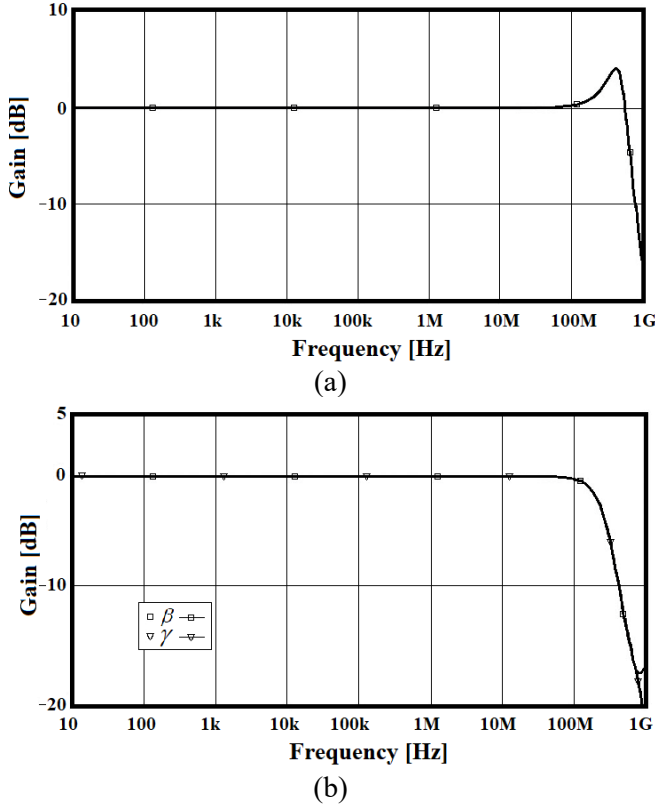
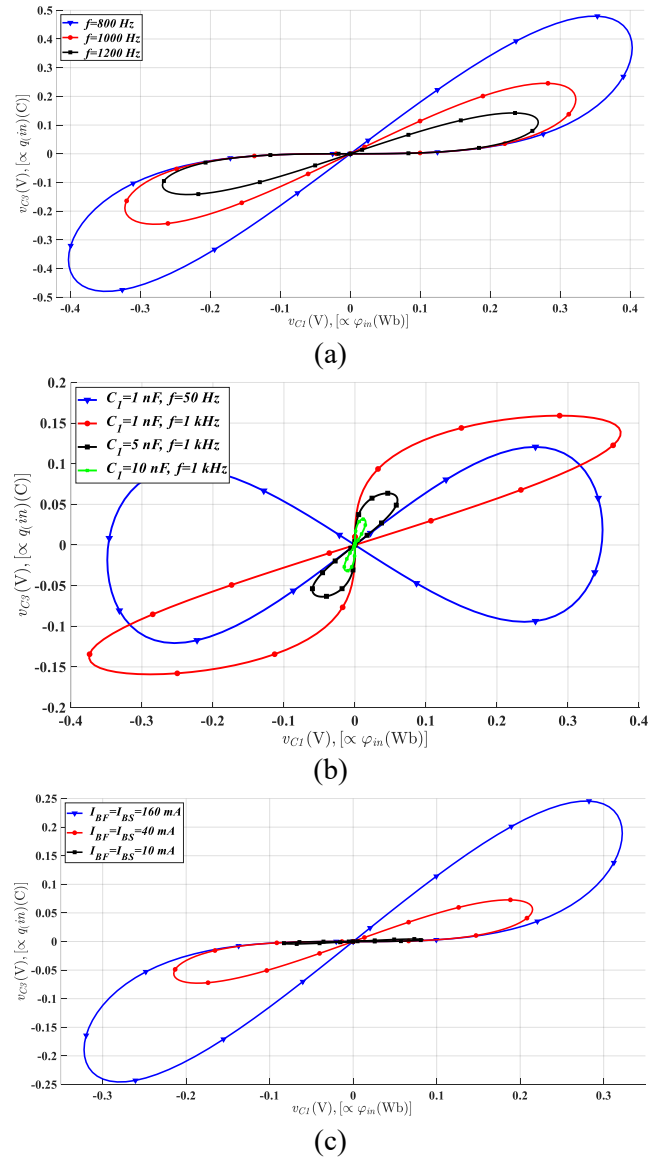


Fig. 4. (a) Frequency response for the current transfer gain (α), (b) Frequency response for the tracking error of the transconductance gain of the VDCC (β) and the voltage transfer gain (γ)

Figure 5(a) illustrates the evolution of pinched hysteresis loops (PHLs) at various excitation frequencies, clearly demonstrating the nonlinear memory behavior of the memtransistor. Here, v_{CI} (*x*-axis) serves as a proxy for magnetic flux (ϕ_{in}), while v_{C3} (*y*-axis) corresponds to charge (q_{in}). As the input frequency increases beyond 1 kHz, notable effects emerge. At higher frequencies, parasitic capacitances of the active devices (VDTA and VDCC) and interconnection nodes begin to dominate the circuit response.

Table 2. DC and AC parameters of VDCC

Parameter	Value for $V_{B1} = -0.28$ V
p and n dc resistance, $R_p=R_n$	4.38 T Ω
z output dc resistance R_z	229.43 k Ω
w_p and w_n output dc resistance	$R_{wp}=186.66$ k Ω $R_{wn}=175.28$ k Ω
p and n input capacitance $C_p=C_n$	0.034 pF
w_p and w_n output capacitance	$C_{wp}=0.0105$ pF $C_{wn}=0.022$ pF
z output capacitance C_z	0.025 pF
x output dc resistance R_x	43 Ω
z output inductance L_x	1.28 μ H
transconductance of OTA stage g_m	282 μ S
corner frequency ω_g, ω_k	5.6 rad/s



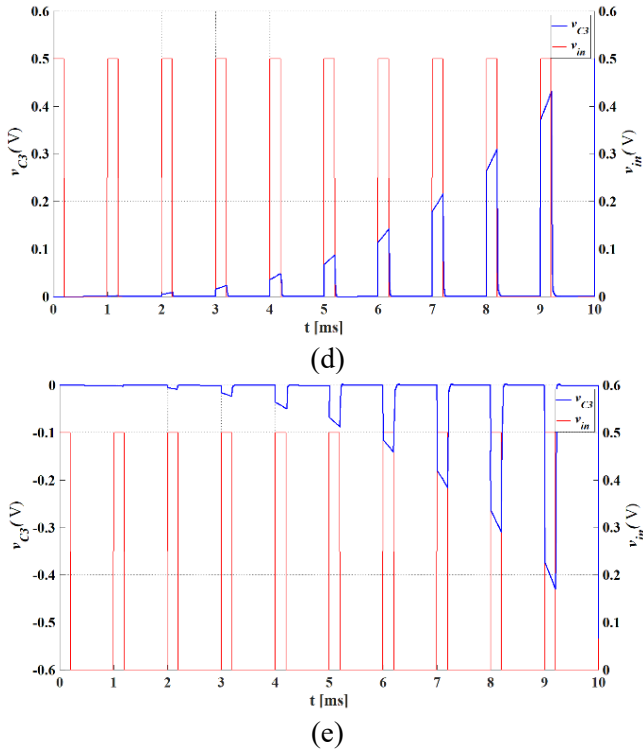


Fig. 5. PHLs of the proposed memtranstor emulator: (a) at various frequencies, (b) for different values of capacitor C_1 , (c) for varying bias currents I_{BF} and I_{BS} of the VDTA-PHLs at different biasing currents, (d) memory effects of the memtranstor for incremental configuration, (e) memory effects of the memtranstor for decremental configuration.

Additionally, the finite bandwidth and slew-rate limitations of the active elements introduce phase shifts and signal attenuation. Consequently, the hysteresis loop becomes frequency-dependent, with the enclosed area decreasing as the frequency rises, highlighting the memtranstor's frequency-sensitive dynamics, consistent with the behavior of memtransitive systems.

Extending the operating frequency of the emulator requires optimization of the active devices (VDTA and VDCC) for higher bandwidth. This can be achieved either by adopting faster CMOS processes or by refining internal circuit topologies to minimize parasitic Capacitances and enhance slew rates. Moreover, reducing the external capacitor values (C_1 , C_2 , C_3) can further increase the achievable frequency range, provided that the transconductance parameters (g_{mF} , g_{mS}) are proportionally adjusted to preserve the desired memtranstance characteristics, as expressed in Eqn. (26).

Figure 5(b) presents the transient response of the proposed memtranstor emulator for varying C_1 values ranging from 1 nF to 10 nF, and $f=1$ kHz ($V_m=100$ mV). The results indicate that changes in capacitance substantially affect both the shape and size of the pinched hysteresis loop (PHL).

As C_1 increases, pronounced modifications in the hysteresis lobes are observed, demonstrating the emulator's sensitivity to passive-element tuning. This capacitive dependence induces systematic shifts in the PHL geometry ("figure-eight" – butterfly), confirming that the hysteresis characteristics can be effectively controlled via capacitive adjustments under both positive and negative memtranstance operation.

The tunable nature of the emulator is further highlighted in Fig. 5(c), which illustrates the influence of varying the VDTA bias currents, I_{BF} and I_{BS} . These currents directly determine the VDTA transconductance, and their adjustment produces corresponding shifts in the PHL response. The results confirm that the emulator's behavior can be precisely modulated by altering the VDTA operating point. For this analysis, the input signal was a sinusoid with 100 mV amplitude at 1 kHz ($C_1=C_2=C_3=2$ nF). The combination of bias-current-dependent and capacitive tunability provides significant reconfigurability, enhancing the circuit's adaptability for diverse application-specific requirements.

Figures 5(d) and 5(e) illustrate the temporal variation of the memtranstance in the proposed floating memtranstor emulator circuit when subjected to a continuous positive pulse train with an amplitude of 0.5 V, a pulse width of 0.2 ms, and a period of 1 ms. Specifically, Fig. 5(d) corresponds to the incremental configuration, whereas Fig. 5(e) represents the decremental configuration. As shown, the memtranstance exhibits an increasing trend in the incremental case and a decreasing trend in the decremental case under the same excitation conditions. In both configurations, the memtranstance evolves through discrete, step-like transitions, indicative of the memory-dependent response of the emulator. These transitions confirm that the memtranstor retains information about both the polarity and magnitude of prior pulses, thereby producing cumulative effects on its dynamic state. This behavior provides further validation of the intrinsic non-volatility characteristic of the memtranstor.

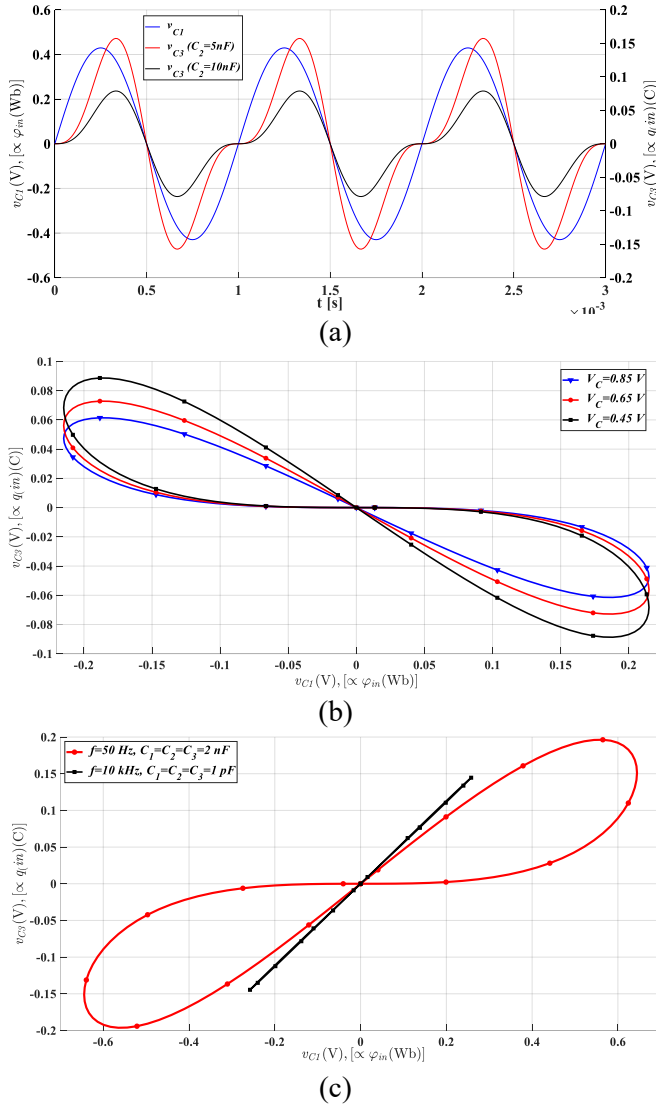


Fig. 6. Transient analysis depicting φ - q relationship of proposed simulator: (a) time-domain waveforms at 1 kHz, (b) PHLs at different control voltage V_C in negative mode, (c) PHLs at frequencies 50 Hz and 10 kHz

The transient response of the emulator under sinusoidal excitation (100 mV, 1 kHz) is shown in Fig. 6(a), where the time-domain waveforms of φ and q are plotted. The flux φ exhibits an approximately sinusoidal waveform, while the charge q deviates from a pure sinusoid. This non-ideal tracking of q underpins the pinched hysteresis loops observed in the φ - q Lissajous plots. Moreover, the in-phase behavior of φ and q confirms the positive memtransance property of the emulator.

The emulator was also tested under bipolar sinusoidal excitation with switch S1 set to position b . As shown in Fig. 6(b), the resulting PHLs appear in the second and fourth quadrants with negative slopes, confirming the emulator's negative memtransance characteristics. In this configuration, φ and q are out of phase, further validating the device's negative polarity operation.

Figure 6(b) also demonstrates the emulator's response for different values of the control voltage V_C , with $C_1=C_2=C_3=2$ nF, excitation frequency $f=1.5$ kHz, and input amplitude $V_m=0.2$ V. The results reveal an additional level of tunability through the electronic resistance R_{el} , further enhancing the flexibility and design space of the proposed emulator.

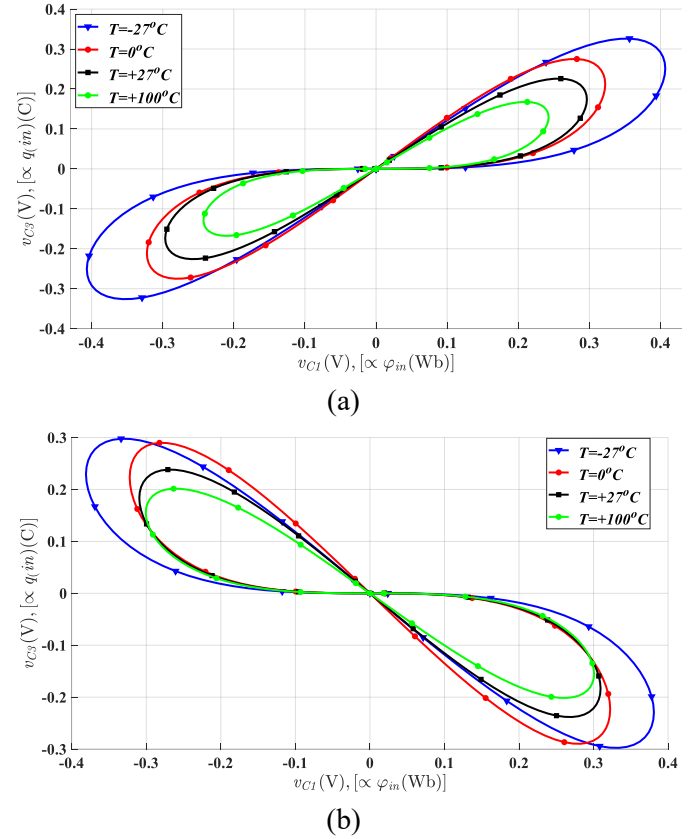


Fig. 7. PHL characteristics of the proposed memtransistor under temperature variations from -27°C to 100°C : (a) for SW2 connected to a and SW3 connected to b , (b) for SW2 connected to b and SW3 connected to a

Quantitative performance metrics are first evaluated at lower operating frequencies, specifically around 50 Hz. As shown in Fig. 6(c), achieving the desired memtransator characteristic – namely, the distinctive hysteresis signature – at such low frequencies requires the use of a larger capacitance value. This requirement arises from practical limitations in integrated circuit technology, where the physical size of the capacitor becomes comparable to the order of parasitic capacitances associated with the VDTA and VDCC ports. As the operating frequency increases, the influence of these parasitic elements becomes more pronounced. In particular, the effective value of the designed capacitance approaches that of the parasitic capacitances, thereby amplifying their impact. Finally, Fig. 6(c) demonstrates that the proposed emulator circuit achieves a maximum operating frequency of approximately 10 kHz.

The temperature sensitivity of the proposed memtranstor emulator was evaluated over a broad range, from -27°C to $+100^{\circ}\text{C}$ ($C_1=C_2=C_3=2\text{ nF}$, $f=1\text{ kHz}$ and $V_m=0.1\text{ V}$). The corresponding pinched hysteresis loop (PHL) characteristics for positive and negative memtranstance configurations are shown in Fig. 7(a) and Fig. 7(b), respectively. Although minor variations in the PHL shapes are observed with temperature changes, the core memtranstor behavior is consistently maintained. These results demonstrate the emulator's thermal stability and confirm its reliable operation across the investigated temperature range.

4.1 Monte Carlo simulation and process variation

In semiconductor fabrication, process parameter variations are inevitable due to intrinsic fluctuations in manufacturing technology and design conditions. Such variations can significantly impact the electrical characteristics of MOSFETs, thereby influencing overall circuit performance. To account for these uncertainties, semiconductor foundries define specific process corners that represent the upper and lower bounds of fabrication-induced variations. Circuits are expected to operate reliably within the design space defined by these limits.

For CMOS-based designs, four standard process corners are commonly specified: Fast-Fast (FF), Fast-Slow (FS), Slow-Fast (SF), and Slow-Slow (SS). In this notation, the first term indicates the performance of the NMOS transistor, while the second corresponds to the PMOS transistor. Evaluating a circuit under these corners is essential to ensure robustness against fabrication variability. The proposed memtranstor emulator was analyzed under all four process corners to assess its stability and functional reliability. The corresponding pinched hysteresis loop (PHL) characteristics, obtained using a 100 mV , 1 kHz sinusoidal input, are presented in Fig. 8(a). The results confirm that consistent PHL behavior is preserved across all process corners, validating the integrity of the proposed design throughout the fabrication design space. This analysis demonstrates that the circuit maintains reliable operation even under worst-case process variations, ensuring its practical feasibility for real-world applications.

To further evaluate robustness against passive component variations, a standard Monte Carlo (MC) analysis was performed. Analytical sensitivity studies for highly nonlinear circuits, such as the proposed emulator, are often challenging. MC simulations provide an effective and widely accepted statistical approach to quantify the impact of component tolerances on circuit behavior. This method involves random perturbation of device and component parameters – such as MOSFET threshold voltages, capacitances, and resistor values – according to their statistical distributions, revealing both the spread and worst-case performance scenarios. The use of

grounded capacitors (C_1 , C_2 , and C_3) in the emulator topology is expected to enhance robustness by mitigating certain parasitic effects and improving overall stability. Consequently, this statistical approach not only highlights sensitive design hotspots but also provides a realistic distribution of performance metrics, bridging the gap between idealized worst-case analysis and the probabilistic nature of practical integrated circuits.

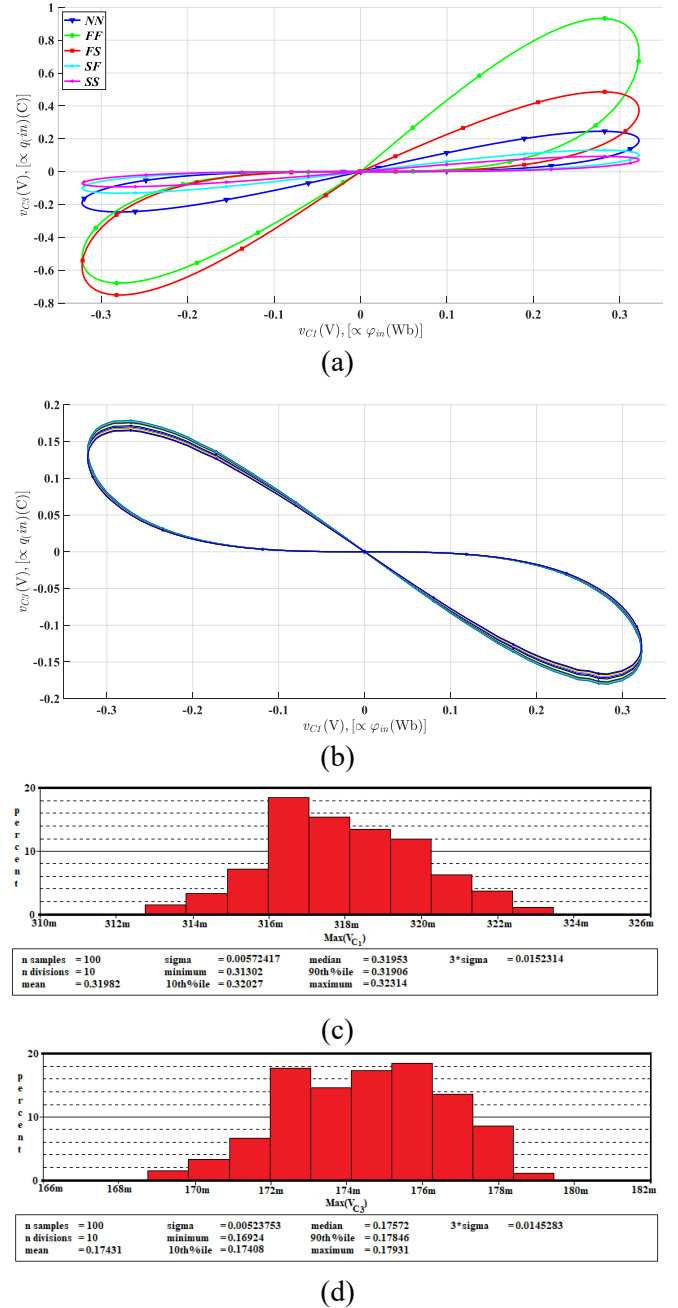


Fig. 8. (a) PHL characteristics of the proposed memtranstor with corner analysis, SW1 connected to *a*, (b) PHL characteristics of the proposed memtranstor for 100 Monte Carlo samples – variation in capacitors ($\pm 10\%$ tolerance in passive components) with switch SW1 connected to *b*, (c) histogram of maximum voltage across C_1 (v_{C1}), (d) histogram of maximum voltage across C_3 (v_{C3})

In the proposed emulator, MC simulations were conducted over 100 iterations, with MOSFET aspect ratios (W/L) and threshold voltages (V_{th}) varied within $\pm 10\%$. The resulting statistical variations in PHL characteristics are shown in Fig. 8(b). Although fabrication-induced parameter variations introduce minor distortions in the PHL curves, the fundamental memtransistor behavior remains preserved. This confirms that the emulator retains its functional integrity under broad process variations, highlighting its robustness and suitability for practical deployment. Furthermore, Figs. 8(c) and 8(d) present the maximum voltages v_{C3} and v_{C1} , respectively, derived from histograms generated through MC simulations. These results demonstrate that the PHL characteristics exhibit low sensitivity to passive-element tolerances, further validating the proposed circuit's robustness against component variability.

4.2 Custom layout and post-layout validation

To validate the practical feasibility of the proposed design, a full-custom layout of the memtransistor (MT) emulator was developed, as illustrated in Fig. 9(a). The corresponding post-layout simulation results are shown in Fig. 9(b), along with a comparative analysis of the pre-layout simulations ($C_1=C_2=C_3=2$ nF, excitation frequency $f=1$ kHz, and input amplitude $V_m=0.1$ V). The fabricated layout occupies an area of approximately $2529.49 \mu\text{m}^2$.

It should be noted that the capacitor is intentionally omitted from the layout to facilitate detailed examination of the influence of varying capacitance values on the simulation results. In practical implementations, the capacitor can be readily realized using a metal-insulator-metal (MIM) structure.

Although the post-layout simulation in Figure 9(b) exhibits noticeable deviations – particularly in the loop region within the third quadrant – relative to the pre-layout results, the two memtransistance states remain clearly distinguishable. This observation confirms that the intrinsic memory behavior of the emulator is preserved, and that the design remains functionally viable for practical applications. The observed discrepancies in current response between pre- and post-layout simulations are primarily attributed to RC parasitic effects introduced during layout synthesis and routing.

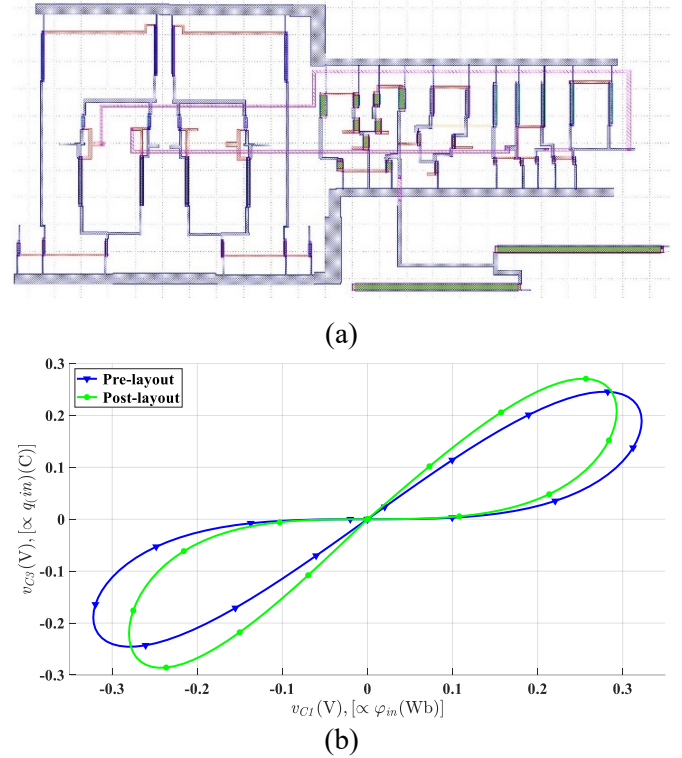


Fig. 9. Layout results: (a) Layout of proposed MT emulator, (b) Simulation results (overlapped) obtained for post layout vs pre layout at 1 kHz frequency

It should be noted that further optimization of the implemented layout is feasible. However, the primary objective of this work was to perform a direct comparison with the results obtained through simulation (the transistor drawings and placements require professional redesign). The simulations were carried out using 180-nm CMOS technology, for which well-established and extensively characterized MOSFET device libraries are available. This approach enables a reliable and consistent validation of the proposed emulator circuit and provides strong evidence supporting its practical feasibility for full custom IC implementation.

In addition to confirming functional correctness, the layout realization in a mature 180-nm process offers several advantages. The technology provides robust design rules, predictable parasitic behavior, and a comprehensive Process Design Kit (PDK), which collectively ensure high confidence in post-layout performance estimation. Furthermore, the chosen technology is still widely used in mixed-signal and analog IC design due to its favorable trade-offs between device matching, noise performance, and fabrication cost. Consequently, the successful layout-to-simulation correlation strongly indicates that the proposed emulator architecture can be fabricated as an integrated solution with minimal risk, making it suitable for future silicon prototyping and potential system-level integration.

To evaluate the effectiveness of the proposed memtranstor (MT) emulator, a comparative analysis with previously reported designs is provided in Tab. 3.

The following key observations can be drawn:

- Multiplier-less design: Unlike [7, 11, 12, 27, 29], the proposed emulator is fully multiplier-free (similar to [28]), eliminating non-idealities of analog multipliers and enabling a compact, symmetric, and low-power architecture.
- Reduced active blocks: Utilizes only two active elements (1 VDTA, 1 VDCC), resulting in simplified and power-efficient implementation.
- Supply voltage & frequency: Operates at the lowest supply voltage (± 0.9 V) while achieving the highest operating frequency (up to 10 kHz) among reported MT designs [7, 11, 12, 27, 28, 29].
- Low power consumption: Consumes only 0.83 mW, confirming high energy efficiency (much less than in [27, 28]).
- Electronic tunability: Provides tunability similar to existing designs, but with additional options, enabling adaptability for reconfigurable systems.

Table 3. Comparison of the proposed emulator with existing emulators based on key performance metrics

Ref.	Number of ABB	Multiplier	Number of C/R	Supply voltage (V)	Operational frequency (Hz)	Tuneability	Power consumption (mW)	F/G
[7]	4CFOA2OA	Yes	3/5	± 15	60-120	Yes	NA	F
[11]	3OTA 1DO-CCII	Yes	3/1	± 1.5	30-1k	Yes	NA	F
[12]	4DVCC	Yes	3/4	± 1.5	100-1k	Yes	NA	F
[27]	1VDTA 1DO-DVCC	Yes	3/0	± 1.5	50-1k	Yes	11.3	F
[28]	1OTA 1CDTA 1VDCC	No	3/1	± 1.5	0.74k-1.5k	Yes	3.8	F
[29]	3CCIIs	Yes	3/2	± 1.2	50-1k	No	NA	G
This work	1VDTA 1VDCC	No	3/0	± 0.9	10k	Yes	0.83	F

It should be emphasized that the emulator proposed in [28] also achieves its functionality without the use of a dedicated multiplication circuit, similar to the approach adopted in the present work. However, several significant distinctions exist between the two implementations. The proposed configuration requires substantially fewer MOS transistors, resulting in a reduced silicon area when implemented as an integrated circuit. Furthermore, the designed circuit operates at a lower supply voltage and exhibits considerably lower power consumption, thereby improving operational autonomy, especially in battery-powered or energy-constrained systems.

The described MT emulator circuit demonstrates notably reduced parasitic effects, enabling improved matching of the active and passive device characteristics. This contributes to enhanced stability and accuracy of the emulated behavior. In addition, the proposed architecture supports operation over a significantly wider frequency range, achieving reliable

functionality up to approximately 10 kHz. Such an extended bandwidth is beneficial for practical applications requiring dynamic signal processing, adaptive control, or real-time emulation of nonlinear memristive phenomena.

From a broader perspective, minimizing circuit complexity while maintaining functional accuracy is a key design challenge in analog emulator circuits, particularly when targeting CMOS integration. Reducing the number of transistors not only decreases chip area and fabrication cost but also improves yield and reduces thermal noise contributions. Moreover, low-voltage and low-power operation is increasingly important in modern IC design trends, where energy efficiency and compatibility with portable or IoT platforms are essential. The improved parasitic profile and extended frequency response further indicate that the proposed MTE structure offers enhanced scalability and robustness compared to previously published designs.

Overall, the proposed design offers an optimized balance of simplicity, low power, wide frequency operation (up to 10 kHz), and tunability, establishing clear advantages over previously reported memtranstor emulators.

5 Conclusion

This paper presents a compact and efficient emulator for the memtranstor, an emerging φ - q memory element, realized without the need for multipliers or complex circuitry. The proposed design employs only one VDTA, one VDCC, and a minimal set of passive components, yet successfully reproduces the core memtranstive characteristics, including frequency-dependent, origin-crossing pinched hysteresis loops with both positive and negative slopes. The circuit operates reliably at a low supply voltage of ± 0.9 V and supports electronic tunability through VDTA bias currents, external capacitors, and a programmable resistor, thereby enhancing adaptability for diverse applications. Simulation results using a 180-nm CMOS process confirm the accuracy and dynamic stability of the emulator. The circuit can be seamlessly configured for both incremental and decremental memory operation, demonstrating high flexibility. Comprehensive evaluations – including pinched hysteresis analysis, Monte Carlo simulations, and tunability tests – verify its functional integrity and robustness against parameter variations. The practical viability of the design is further established through non-ideal analysis and post-layout verification. A full-custom layout, occupying $2529.49 \mu\text{m}^2$, was implemented, and post-layout simulations confirmed preservation of the key memtranstive properties. By avoiding operational amplifiers, the proposed design eliminates limitations associated with fixed gain-bandwidth products, thus enabling improved high-frequency performance. Overall, the proposed fully monolithic memtranstor emulator offers simplicity, functional accuracy, and design flexibility, making it a strong candidate for integration in advanced memory systems, neuromorphic computing architectures, adaptive signal processing [7, 28], and chaotic oscillator applications [12, 27].

Acknowledgment

This research was supported by the Ministry of Education, Science and Technological Development of the Republic of Serbia, and these results are parts of the Grant No. 451-03-33/2026-03/ 200132 with University of Kragujevac – Faculty of Technical Sciences Čačak.

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Received 15 April 2026