

Meminductor emulator using VDBA and CDBA and its application in chaotic oscillator

Shireesh Kumar Rai¹, Bhawna Aggarwal^{2*}, Rupam Das³, Amaan Siddiqui⁴, Akanksha Arora⁵

A voltage differencing buffered amplifier (VDBA) and a current differencing buffered amplifier (CDBA) are used in the proposed compact meminductor emulator design. The proposed emulator reduces the passive components number by utilizing parasitic components of CDBA to obtain a compact layout. This feature also aids in the realized circuit's ability to operate at a high frequency. The element in the suggested design has memory of its previous state, since the effective meminductance is dependent on the total charge stored on the capacitors. By altering the capacitance values, pinched hysteresis loops between magnetic flux (Φ) and current (i) are shown throughout a broad frequency range (1 kHz to 3 MHz). Both incremental and decremental hysteresis assessments, non-volatility measures, and transient response tests verify that the suggested emulator is operating correctly. The theoretical predictions are closely matched with LTspice simulations utilizing 0.18 μm process characteristics. The non-ideal analysis of the suggested configuration verifies the accuracy of the derived expressions and simulation results. Lastly, the meminductor practical application in actual circuits is confirmed by incorporating it into a chaotic oscillator.

Keywords: active building block, meminductor, hysteresis curve, chaotic oscillator

1 Introduction

Mem-elements are gaining significant importance because of their wide-ranging applications in electrical, electronics, and computer engineering. Among these, the memristor – first proposed as the missing link between charge q and flux Φ – is considered the foundational member of the memelements family [1]. In circuit theory, electrical and electronic engineers work with four fundamental variables: flux Φ , current i , voltage v , and charge q . The relationships between these variables define the three classical passive components: the resistor R relates voltage v and current i , the inductor L relates flux Φ and current i , and the capacitor C relates charge q and voltage v . The memristor complements these by linking charge and flux, thereby completing the theoretical framework of circuit elements. Memristor is viewed upon as a resistor with memory whose resistance is varied according to the previous history of the device. The idea of the memristor has been further developed to introduce memcapacitor and meminductor, considering the dependency of capacitances and inductances on the past history of the devices [2]. Recently, memristor has gained a lot of popularity in various domains. However, physical implementation of the memristor is a challenging task and amounts to high cost in prevailing

CMOS technology. Memristor is the only known memristive device available in market and is not compatible with various applications [3]. Following these facts, there are numerous researchers who are involved in realizing various devices that can mimic their behaviour. Along with memristors, other memelements – memcapacitors and meminductors – are also examined due to their inherent storage characteristics. Each of these elements possess a unique relationship not seen in any other element, broadening the application domain. Many new circuits have been designed using these memelements that are being used in several applications [4-9]. A meminductor provides a flux-current relationship with inherent energy storage capability, which not only contributes nonlinearity but also adds a dynamic state associated with magnetic energy. This dual role enhances the system's effective dimensionality more naturally than a memristor, which is fundamentally resistive and dissipative in nature [10]. As a result, meminductor-based circuits are more capable of generating sustained oscillations and richer chaotic or hyperchaotic dynamics without relying heavily on external reactive components. From a design perspective, meminductors can reduce dependency on bulky inductors by emulating

¹ECE Department, Thapar Institute of Engineering and Technology, Patiala, Punjab, India

²ECE Department, Faculty of Technology, Delhi University, New Delhi, India

³ECE Department, Asansol Engineering College, West Bengal, India

^{4,5}ECE Department, Netaji Subhas University of Technology, New Delhi, India

¹skumar.raai@thapar.edu, ²bhawna.aggarwal031@gmail.com, ³rupam.ece@aecwb.edu.in,

⁴amaans.ec18@nsut.ac.in, ⁵akanksha.ec18@nsut.ac.in

inductive behavior in a compact and tunable form, while avoiding some limitations of memristors such as pinched hysteresis sensitivity to frequency and higher dissipative losses. Consequently, meminductor-based designs often achieve better energy efficiency, enhanced controllability, and greater dynamical richness compared to their memristor-based counterparts [11]. Meminductors play a unique role in neuromorphic and brain-inspired computing beyond memristors [12]. The meminductor finds applications beyond chaotic and non-linear circuits such as image encryption [13], adaptive learning circuit [14], neural spike generator [15, 16], and Fitz-Hugh-Nagumo (FHN) neuron-based circuit [17], etc.

The significant impact of the memelements on the new era of electronics and electrical engineering demands the easy availability of these components in the market. Driven by this need many researchers and engineers are continuously trying to design memelement emulators with available resources. Although many memristor emulators are available in literature [18-23], the availability of meminductors and memcapacitors is rather limited. Researchers are making efforts to find alternative realizations to obtain emulator designs with simple structure and possessing improved performance characteristics. The behavior of a designed memelement emulator is verified by observing the pinched hysteresis loops (PHLs) among voltage, current, charge and flux [24]. The memristor emulator exhibits a PHL in the relationship between charge and flux or equivalently, between current and voltage. Similarly, the memcapacitor displays a PHL in charge versus voltage plane, while the meminductor shows a PHL between flux and current.

The meminductor and memcapacitor emulators available in literature can be majorly classified in two broad categories: (i) with memristor and (ii) memristor-less. The first such emulator reported in [25] was designed using an operational amplifier (OP-AMP), memristor, and a few passive components. Mutator-based memelement emulators have been suggested in literature, where second-generation current conveyors (CCII) and operational transconductance amplifiers (OTAs) are used [26]. In the mutator design reported in [26], a memristor is required and thus it falls under the first category of realization. Subsequently, other circuits of memcapacitor and meminductor emulators were reported utilizing CCII, memristor and passive components [27] and are based on mutator realizations. Other mutator circuits using current feedback operational amplifier (CFOA), memristor and passive components have been reported that can transform memristor into memcapacitor and meminductor emulators [28]. In [29], an attempt was made to implement a memristor-less floating meminductor emulator but the circuit was very complex. Another attempt for the memristor-less realization of meminductor emulator

has been done in [30] but due to usage of the analog multiplier, passive inductor along with three OP-AMPs, several resistors and capacitors make the circuit less attractive. Next, meminductor emulator based on CCII has been introduced using capacitor, with an additional requirement of adder and multiplier [31]. Mutator-based meminductor emulator was introduced in [32], where memristor emulator was connected at output terminal and thereby the requirement of memristor emulator is must for this design. The idea of mutator circuit designed in [32] has been extended for the series, parallel and hybrid connections of mem-inductors in [33]. A mem-inductor emulator based on memristor was introduced using a CCII, an OP-AMP, and a few passive components [34]. A universal mutator was reported for the emulation of memristor, mem-capacitor, and mem-inductor with some modifications in the circuit, while a memristor is needed for the implementation of mem-capacitor and meminductor emulators [35]. A mem-inductor emulator was designed and implemented with the help of current conveyors, an analog multiplier, an adder, and a few passive components in [36]. An OP-AMP based meminductor emulator was realized employing memristor, resistors, and capacitors [37]. However, in this design the use of memristor and matching between passive components is required to emulate the meminductor behavior. The exact components matching often do not meet practically. A simple mutator circuit for the emulation of memelements using AD844s, OP-AMP, resistors, capacitors, and varactor diode has been demonstrated in [38]. Another universal emulator was reported using CCII and OP-AMPs but the use of an analog multiplier results in complex circuitry [39]. A meminductor emulator was suggested employing seven OP-AMPs, fourteen resistors, and two capacitors [40]. Another meminductor emulator has been reported using two voltage differencing transconductance amplifiers (VDTAs), a multiplier, and two grounded capacitors [41]. A current backward transconductance amplifier (CBTA) based memcapacitor and meminductor emulator was realized with the help of a memristor and capacitor [42]. An operational amplifier and multiplier-based meminductor emulator using nine OP-AMPs, several resistors, and two capacitors have been reported in [43]. A miscellaneous block-based emulator for meminductor has been designed with the help of an OTA, CFOA, OP-AMP, resistors, and capacitors [44]. A floating configuration utilizing Riordan's gyrator was demonstrated in [45] that employs three OP-AMPs, six resistors, and a memristor. VDTA based meminductor emulator utilizing two additional grounded capacitors was reported in [46]. A grounded configuration employing two VDTAs, an OTA, and two grounded capacitors was reported in [47]. Another meminductor implementation employing three OTAs and two capacitors was introduced in [48]. Memelement emulators using one OTA, two CCII, and two

capacitors were reported in [49]. Several circuits of meminductor emulators were reported using OP-AMPs, resistors, capacitors, and memristors [50]. Other mem-capacitors and meminductor emulators were realized by employing voltage differencing current conveyor (VDCC), memristor, and capacitor [51]. A floating meminductor emulator using VDTA and current differencing buffered amplifier (CDBA) with two grounded capacitors was realized in [52].

Numerous reported meminductor emulators utilize memristors [25, 27, 28, 33, 35, 43, 50, 51]. Some emulators do not employ a memristor, however, the requirement of analog multiplier and several other components result in significant design complexity [30, 31, 32, 34, 36, 39, 44, 45, 49, 50]. Some compact realizations have also been reported but their frequency of operation is limited up to a few Hz or kHz range [25, 33, 36, 37, 42, 44, 45]. The objective of this manuscript is to propose a circuit of meminductor emulator without employing memristor and multiplier, while operating for a wide frequency range.

This paper has eight sections: Section 1 includes the introduction. A detailed explanation of the analog building blocks used in the meminductor-based emulator is given in Section 2. The operating principle, analysis of the emulator is given in Section 3. Section 4 describes the simulation results, while Section 5 presents the non-ideal analysis of the proposed emulator configuration. Section 6 compares the proposed meminductor emulator with existing designs, highlighting its performance advantages. Section 7 showcases its integration into a chaotic oscillator. Finally, Section 8 presents the conclusion.

2 Voltage and current differencing buffered amplifiers: Characteristics and circuit diagrams

The schematic of a VDBA is given in Fig. 1. As described by Eqn.(1), the VDBA has two input terminals, labeled P and N, implying that no current flows through them.

$$I_P = I_N = 0 \quad (1)$$

$$I_Z = G_m(V_P - V_N) \quad (2)$$

$$V_W = V_Z \quad (3)$$

According to Eqn. (2), the current at the Z terminal is determined by transconductance G_m multiplied by the voltage difference between the inputs $V_P - V_N$. As shown in Eqn. (3), the voltage at the W terminal mirrors the voltage at the Z terminal.

The G_m , as indicated in Eqn. (4), is controlled by the bias voltage V_B .

$$G_m = K(V_B - V_{SS} - V_{th}) \quad (4)$$

Here, K is a transconductance parameter of the VDBA, expressed as

$$K = \frac{\sqrt{\beta_1\beta_9}}{2}(V_B - V_{SS} - V_{th}) \quad (5)$$

where

$$\beta = \mu_n C_{ox} \frac{W}{L}$$

of the corresponding MOSFET, with μ_n , C_{ox} and W/L representing carrier mobility, oxide capacitance per unit area and aspect ratio of the MOSFET respectively. V_{SS} is the magnitude of negative supply rail and V_{th} represents the threshold voltage of the MOSFET.

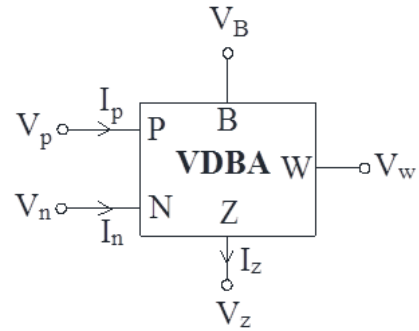


Fig. 1. VDBA block diagram

CMOS diagram of VDBA is given in Fig. 2. In this circuit, two biasing terminals have been represented: V_B and V_{VC} . As depicted in Fig. 1, V_B is made available to the designer for external biasing to control the transconductance G_m of VDBA, while V_{VC} is an internal voltage of the block for biasing the transistors M10 to M16.

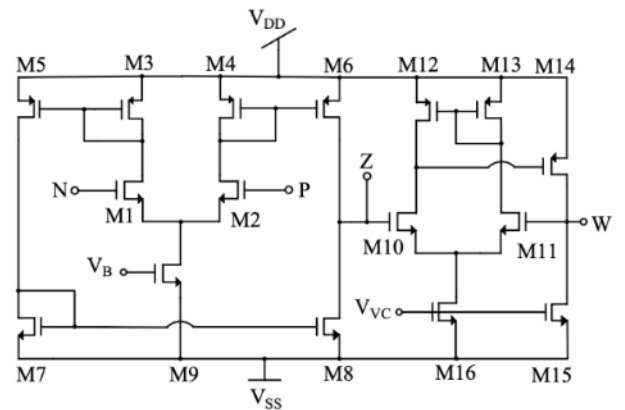


Fig. 2. Circuit diagram of VDBA [53]

As illustrated in Fig. 3, CDBA is a multi-terminal active building block (ABB) featuring P and N input ports, and Z and W output ports. In Fig. 3, two Z terminals are shown to provide identical currents, as required by the suggested circuit.

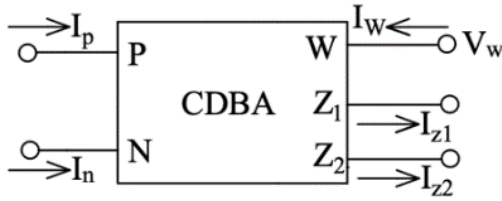


Fig. 3. CDBA block diagram

As described by Eqn. (5), the voltages at the P and N ports are effectively zero due to their very low input impedances. The current flowing through Z is the difference between the input node currents, as indicated in Eqn. (6). Furthermore, according to Eqn. (7), voltage V_z at terminal Z gets transferred to W terminal as V_W .

$$V_P = V_N = 0, V_W = V_{Z1} \quad (6)$$

$$I_{Z1,Z2} = I_P - I_N \quad (7)$$

The CMOS realization of CDBA is illustrated in Fig. 4. Here, I_{B1} and I_{B2} are the biasing currents and V_{CC} is a voltage source, which are crucial for proper operation of the block and are responsible for deciding its DC and AC characteristics.

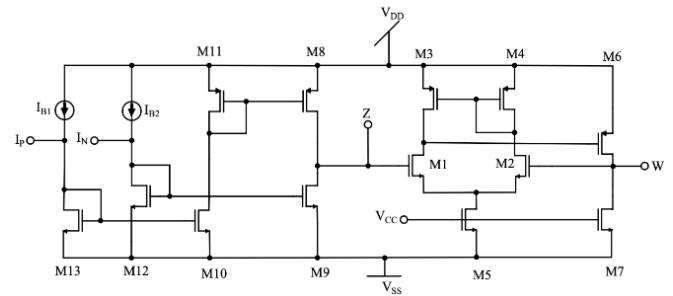


Fig. 4. Circuit diagram of CDBA [54]

To design the proposed circuit, VDBA and CDBA have been chosen because of their distinct advantages compared to other blocks. A comparative assessment of these blocks to other analog building blocks is given in Tab. 1. The table compares six widely used analog blocks – OTA, CFOA, second-generation current controlled current conveyor (CCCII), VDTA, VDBA, and CDBA, based on their behavior, performance, and implementation aspects.

Table 1. Comparative assessment of analog building blocks

Aspect	OTA [57]	CFOA [58]	CCCII [59]	VDTA [60]	VDBA [53]	CDBA [61]
Functional behavior	Voltage-to-current	Voltage-mode	Current-mode	Voltage-to-current	Voltage differencing with dual outputs	Current differencing with buffered output
Input impedance	High	High	Medium	High	High	Low
Output nature	High impedance current	Low impedance voltage	High impedance current	High impedance current	Simultaneous current and voltage outputs	Current output with voltage buffering
Power requirement	Low-moderate	Moderate	Moderate	Low-moderate	Low	Low
Supply voltage demand	Low	High	Moderate	High	Low	Low-moderate
Frequency performance	Wideband	Wideband	Wideband	Moderate-wide	Wideband	Wideband
Electronic control	Transconductance (g_m)	Feedback resistor	X-terminal resistance	Transconductance (g_m)	Transconductance (g_m)	Limited (externally controlled)
Implementation complexity	Low	High	High	Medium	Low	Low
CMOS compatibility	Yes	Bipolar preferred	Yes	Yes	Yes	Yes

A routine analysis conducted on Fig. 5 based on the connections shown, gives input current I_{in} as:

$$I_{in} = -I_{ZC2} = -I_{ZC1} = -\frac{G_m}{R_P C_1} \varphi_{in}(t) \quad (16)$$

Substituting G_m from Eqn. (4) in Eqn. (16) and using Eqn. (15), I_{in} can be expressed as:

$$I_{in} = \frac{K}{R_P C_1} \times \left(-\frac{G_m}{C_1 C_2 R_P} \rho_{in}(t) + V_{SS} + V_{th} \right) \varphi_{in}(t) \quad (17)$$

The constitutive relationship linking current $I(t)$ and flux $\varphi(t)$ in a meminductor is described as [62]

$$I(t) = L_M^{-1} \cdot \varphi(t) \quad (18)$$

where, L_M^{-1} denotes an inverse meminductance. Comparison of Eqns. (17) and (18) yields L_M^{-1} for the circuit as:

$$L_M^{-1} = \frac{K}{R_P C_1} \left(-\frac{G_m}{C_1 C_2 R_P} \rho_{in}(t) + V_{SS} + V_{th} \right) \quad (19)$$

The constant term and the variable term make up the meminductance of the suggested meminductor emulator, as demonstrated by Eqn. (19). The fixed-term depends upon V_{SS} and V_{th} , and on the contrary, the variable term depends upon input flux and transconductance. The overall meminductance can be controlled by C_1 and C_2 at the design time and is greatly dependent on process parameters K and R_P . Overall, these parameters play a crucial role in shaping the dynamic response and tuning the emulator characteristics. This meminductance response depicted by Eqn. (19) represents incremental behavior of the proposed emulator. For a sinusoidal input signal V_{in} applied to the suggested meminductor emulator, $\rho_{in}(t)$ is given by:

$$\begin{aligned} \rho_{in}(t) &= \int \varphi_{in} dt = \int \frac{V_m}{\omega} \cos(\omega t - \pi) \\ &= \frac{V_m}{\omega^2} \sin(\omega t - \pi) \end{aligned} \quad (20)$$

Here, V_m denotes the highest amplitude of the excitation signal and ω represents its angular frequency. Upon substituting this value of ρ from Eqn. (20) into Eqn. (19), yields:

$$\begin{aligned} L_M^{-1} &= \frac{K}{R_P C_1} (V_{SS} + V_{th}) \\ &\quad - \frac{K G_m}{C_1^2 C_2 R_P^2 \omega^2} \sin(\omega t - \pi) \end{aligned} \quad (21)$$

Equation (21) shows that the meminductance of the circuit depends upon the frequency and amplitude of the signal applied. Moreover, it shows that the value of meminductance can be controlled by varying the capacitances C_1 and C_2 .

The circuit shown in Fig. 5 can be configured in decremental mode by adjusting the switch position and connecting it to position ②. Routine analysis of the suggested emulator, when operated in decremental configuration gives meminductance L_M similar to Eqn. (21) with the difference in polarity of fixed-term expressed as:

$$\begin{aligned} L_M^{-1} &= -\frac{K}{R_P C_1} (V_{SS} + V_{th}) \\ &\quad - \frac{K G_m}{C_1^2 C_2 R_P^2 \omega^2} \sin(\omega t - \pi) \end{aligned} \quad (22)$$

Equation (22) represents the meminductance of the circuit in decremental configuration. Equations (21) and (22) show that the proposed meminductor's meminductance consists of two parts, one component being fixed and other being variable. These components can be controlled by the values of capacitors and operating frequency.

4 Simulation results

The simulations have been done by LTspice program to examine the behavior of the meminductor emulator. With the aid of a power supply voltage of ± 0.9 V, VDBA and CDBA have been implemented utilizing TSMC 180nm CMOS technology. $I_{B1}=I_{B2}=20$ μ A are the DC currents of CDBA, and -0.1 V is the bias voltage set for V_{VC} and V_{CC} . The MOSFET aspect ratios utilized in the design of buffered amplifiers with voltage and current differencing are listed in Tab. 2. In the simulations, 100 pF, 10 pF, and 100 Ω are selected as the values for capacitances C_1 , C_2 , and resistance R_1 , respectively.

Table 2. Device size of MOSFETs employed in VDBA and CDBA

VDBA			CDBA		
MOSFET	W (μ m)	L (μ m)	MOSFET	W (μ m)	L (μ m)
M1-M4	7	0.35	M1- M4, M16, M17	32	2
M5, M6	21	0.7	M5, M6, M14, M15	42.5	0.36
M7, M8	7	0.7	M7, M8	0.8	0.5
M9	3.5	0.7	M9, M12, M13	10	0.5
M12-M14	14	0.35	M10, M11	4	0.5

4.1 Transient analysis

The suggested circuit's meminductive behavior has been investigated using a ± 50 mV bipolar sinusoidal voltage signal with a 90° phase shift. The inductive nature of the suggested meminductor is demonstrated by the transient waveforms for voltage, current and flux produced in incremental arrangement (S_1 connected to ①) in Fig. 6. When compared to the applied voltage signal, it is evident that the flux and current waveforms are lagging in phase. This confirms the inductive nature of the proposed circuit.

The ability to store prior knowledge is a crucial feature of the memelements. The meminductance (the ratio of flux to current) of the suggested circuit has been examined and plotted in Fig. 7 to demonstrate its non-volatility behavior. This waveform has been observed by exciting the emulator with a 50 mV pulse signal having 20 μ s period and an ON time of 1 μ s.

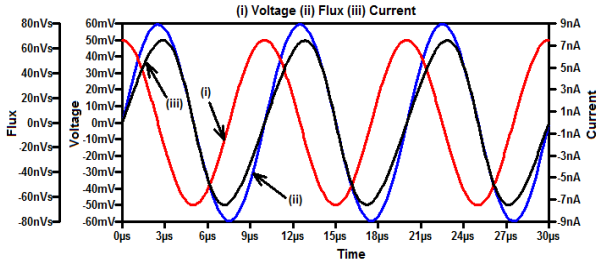


Fig. 6. Transient response of proposed incremental meminductor with a 100 mV (± 50 mV), 10 kHz sinusoidal signal

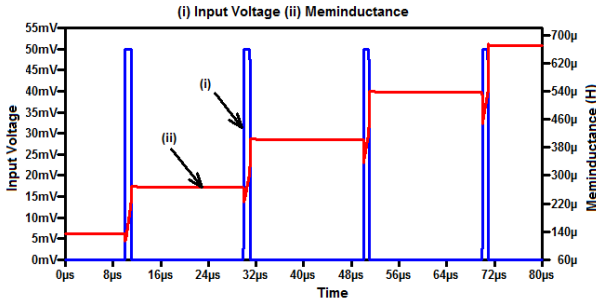


Fig. 7. Non-volatile response of the proposed circuit with 50 mV, 20 μ s pulse signal and 1 μ s ON time

4.2 Pinched hysteresis plots

The ϕ - i characteristic of a meminductor generally displays a PHL. To evaluate this response, a sinusoidal bipolar signal of ± 50 mV, 100 kHz and 90° phase shift was applied in the suggested meminductor connected in decremental configuration (connecting S_1 to ②). The resulting ϕ - i curve, shown in Fig. 8, clearly demonstrates a zero-crossing PHL thereby confirming the meminductive nature of the circuit.

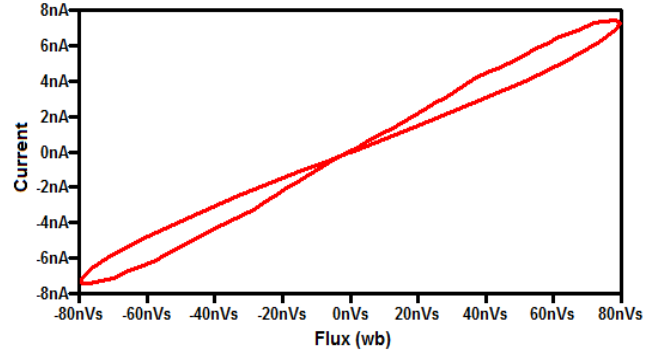
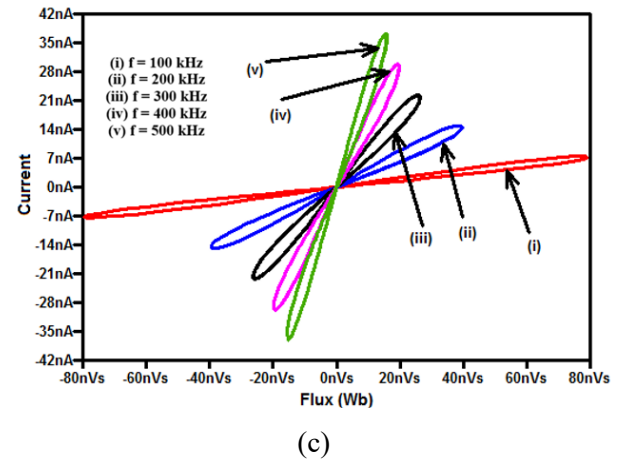
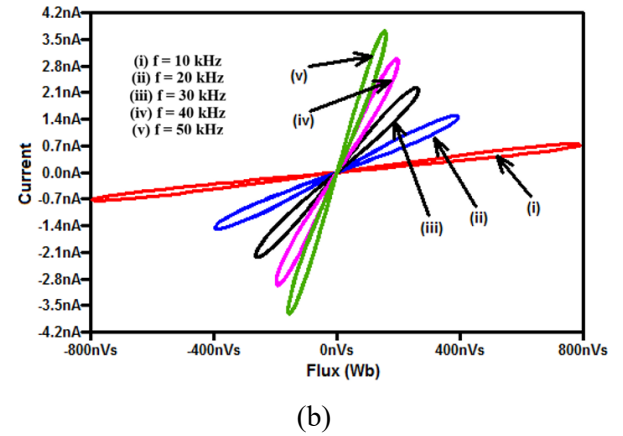
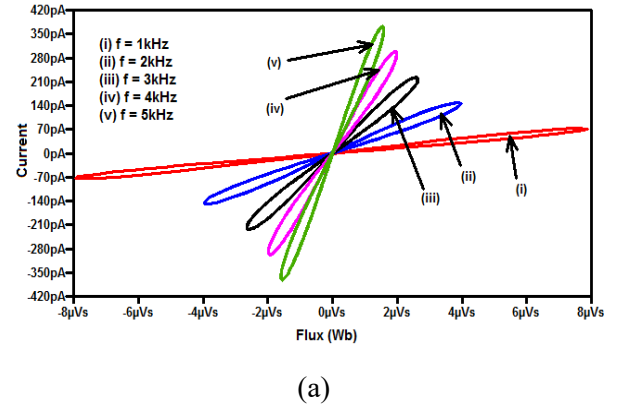


Fig. 8. A zero-crossing PHL of the meminductor under a 100 kHz input signal ($S_1 \rightarrow$ ②)



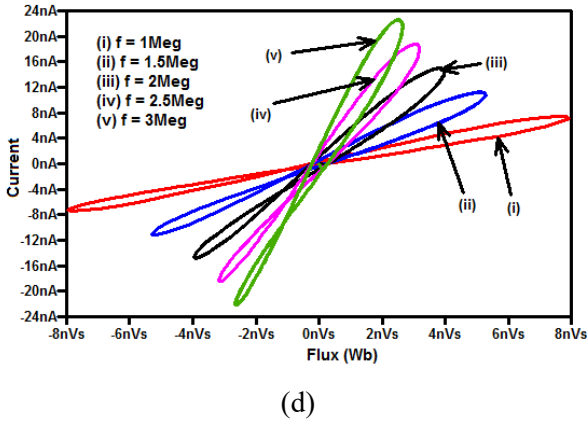


Fig. 9. PHLs at various sets of frequencies: (a) 1 kHz to 5 kHz, (b) 10 kHz to 50 kHz, (c) 100 kHz to 500 kHz, (d) 1 MHz to 3 MHz

The decremental meminductor ($S_1 \rightarrow \textcircled{2}$) emulator's functionality is examined at different frequencies and observed hysteresis graphs are displayed in Fig. 9. The frequency range captured in these curves are: (a) 1 kHz to 5 kHz, (b) 10 kHz to 50 kHz, (c) 100 kHz to 500 kHz, (d) 1 MHz to 3 MHz. A sinusoidal signal pulsating at the designated frequency with an amplitude of ± 50 mV and a phase shift of 90° has been used to plot all these graphs. Except for the hysteresis curves for frequency 1 MHz to 3 MHz that are displayed in Fig. 9(d) and have been drawn using $C_2 = 1$ pF, the parameter values are the same as previously stated. These curves demonstrate how the meminductor works in the broad frequency range, from kHz to MHz. Additionally, it has been shown that hysteresis loops begin to skew after 3 MHz, with the pinch-off point moving to one side of the loop.

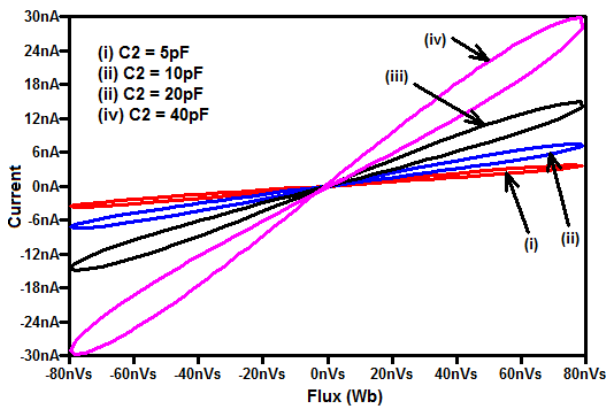


Fig. 10. PHLs of the proposed meminductor (decremental, $S_1 \rightarrow \textcircled{2}$) observed at different values of C_2 , with a 50 mV, 100 kHz sinusoidal input signal

Figure 10 displays the hysteresis curves that were produced for various values of capacitor C_2 . These curves were plotted for a sinusoidal signal with 100 kHz,

± 50 mV. As anticipated, these curves show that the area inside the lobe expands as the capacitor value rises. Furthermore, it is examined that low values of C_2 can be used to create hysteresis loops for higher frequencies.

Additionally, the suggested incremental meminductor's behavior has been investigated. Figure 11 shows the response seen on the ϕ vs. i plane for sinusoidal signals oscillating at various frequencies with an amplitude of ± 50 mV and a phase shift of 90° , with S_1 placed at position $\textcircled{1}$. The analysis of different waveforms depicts that the proposed circuit enjoys a wide bandwidth and works in the frequency range of 1 kHz to 3 MHz. It is observed that the pinched point shifts with an increase in frequency and this is displayed in Fig. 9(d). Beyond 3 MHz, the hysteresis graph gets distorted, due to excessive shifting of the pinched point. The simulated graphs were obtained to verify theoretical working of the meminductor emulator.

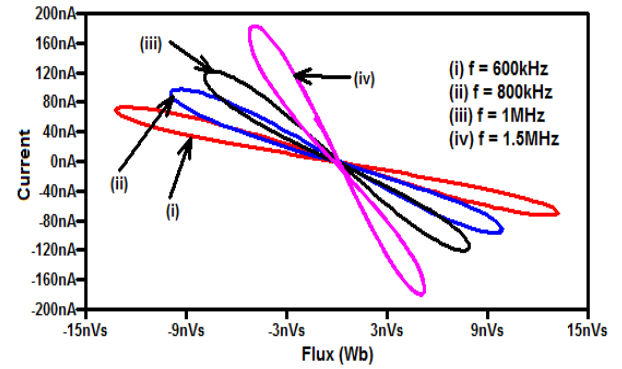


Fig. 11. PHLs with zero-crossing are observed in the proposed incremental meminductor ($S_1 \rightarrow \textcircled{1}$) across different input frequencies

4.3 Process-Voltage-Temperature (PVT) analysis

To demonstrate the reliability of the proposed emulator under realistic operating conditions, its behaviour has been examined under various variables conditions of process-voltage and temperature (PVT). To analyze the tolerance of the designed system under process variations, corner and Monte Carlo (MC) simulations have been carried out. A sinusoidal signal of ± 50 mV with 100 kHz frequency was applied in the suggested meminductor connected in decremental configuration and the circuit was tested for standard process corners (FF $\rightarrow$ fast-fast, FS $\rightarrow$ fast-slow, SF $\rightarrow$ slow-fast and SS $\rightarrow$ slow-slow). The observed results are shown in Fig. 12(a). Additionally, the results for same input signal for 200 runs of MC analysis for $\pm 10\%$ Gaussian deviations in MOSFETs threshold voltage and component parameters (resistor and capacitor values) have been illustrated in Fig. 12(b). The PHLs observed in Fig. 12

show minor fluctuations around the ϕ - i curve obtained for exact parameter values, thereby confirming the robust behaviour of the proposed system under process variations.

To verify the reliability of the system under voltage variations, the circuit has been subjected to sinusoidal signal of ± 50 mV with 100 kHz frequency, while the supply voltage is swept by $\pm 10\%$ around its nominal value. The PHL waveforms in ϕ - i plane are plotted in Fig. 13(a). Furthermore, these waveforms for temperature fluctuations in a range of -40°C to $+100^\circ\text{C}$ have been illustrated in Fig. 13(b). All these curves, shown in Figs. 12 and 13 confirm the stable and reliable operation of the proposed emulator under practical environmental conditions.

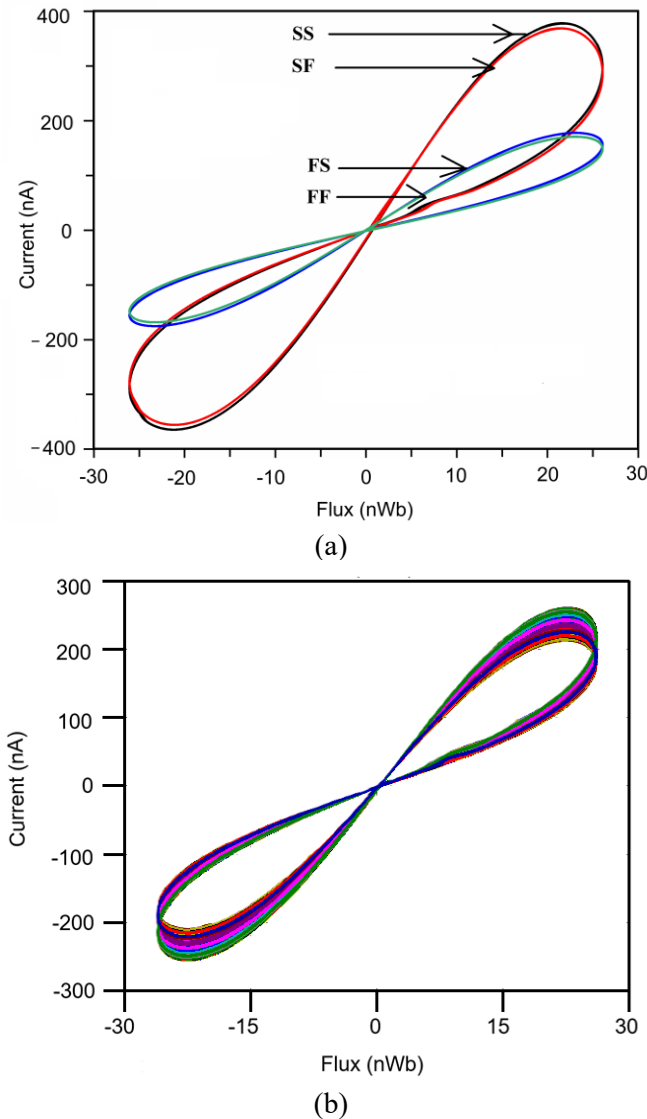


Fig. 12. PHLs obtained with ± 50 mV, 100 kHz sinusoidal signal under (a) standard process corners (FF, FS, SF, and SS), (b) MC analysis for 200 runs for $\pm 10\%$ variations in threshold voltage and parameter values

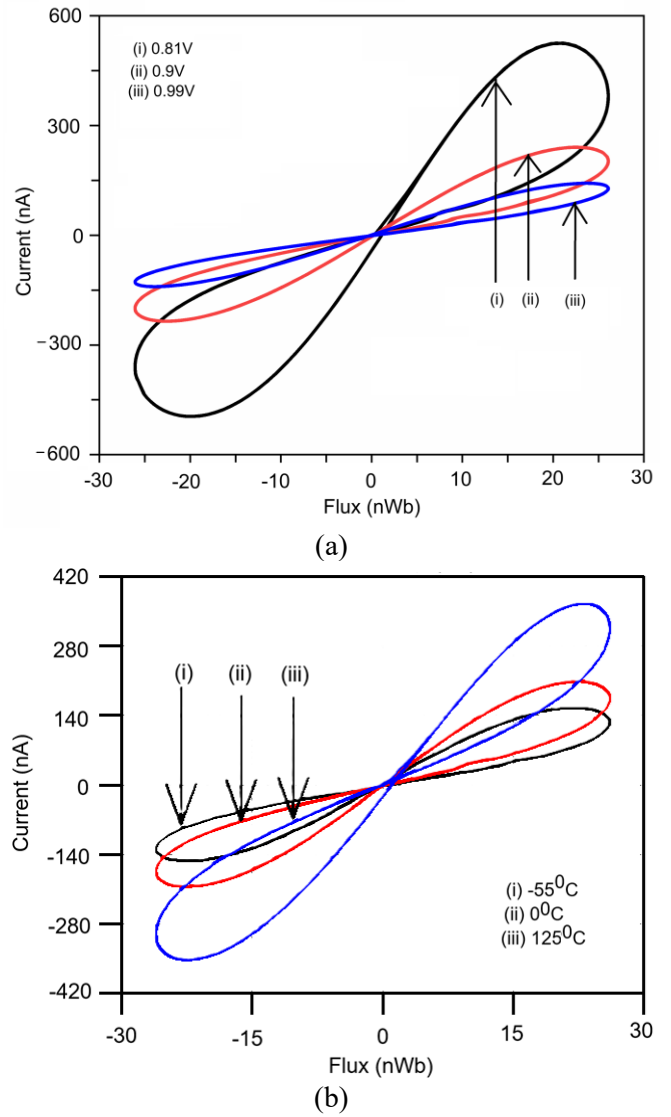


Fig. 13. PHLs obtained with ± 50 mV, 100 kHz sinusoidal signal under (a) supply voltage variations by $\pm 10\%$ around its nominal value, (b) temperature fluctuations in a range of -40°C to $+100^\circ\text{C}$

5 Non-ideal analysis

The derivation carried out in Section 4 for mathematical analysis of the proposed emulator ignores the presence of parasitic elements and tracking errors of the active blocks. The study of these non-ideal elements is important, especially at high frequency operation. The equivalent circuit of the proposed emulator incorporating non-ideal elements at different ports of VDBA and CDBA has been depicted in Fig. 14. For ease of understanding, all the parasitic elements (resistors, capacitors and inductors) appearing at various ports have been denoted by a subscript representing the port and block name. The voltage tracking errors have been denoted by α with a subscript representing the block name and current tracking errors have been denoted by β with a similar subscript. An analysis analogous to that performed for the ideal case has been carried out and is briefly presented below.

Table 3. Comparison with circuits existing in literature

Ref.	Active blocks/Components	Passive components	Memristor-less	Operating frequency	Electronic tunability	Floating (F)/Grounded (G)	Sim. (S) /Exp. (E)
[25]	1 OP-AMP	1 M_R , 1R, 1C	No	8 Hz	No	G	S
[27]	2 CCIIIs	1 M_R , 1R, 1C	No	-	No	F	-
[28]	2 AD844s	1 M_R , 1R, 1C	No	1 kHz	No	F	Both
[29]	4 CCII+s, 2 OP-AMPs	8R, 2C	Yes	36.9 Hz	No	F	S
[30]	3 OP-AMPs, 1 Multiplier, 10 MOS transistors	2R, 2C, 1L	Yes	300 Hz	No	F	S
[31]	3 CCII+s, 1 multiplier, 1 adder, 1 divider	3R, 2C	Yes	5 Hz	No	G	S
[32]	2 CCII+s, 4 OP-AMPs, 1 Multiplier	7R, 2C	Yes	800 Hz	No	F	S
[33]	1 CCII+, 3 OP-AMPs	1 M_R , 1C, 3 R,	No	400 Hz	Yes	Both	Both
[34]	3 OP-AMPs, 3 AD844s, 1 AD633	10R, 2C	Yes	16 Hz	No	F	Both
[35]	3 CCII+, 3 OP-AMPs, 1 Multiplier	1 M_R , 3R, 1C	No	21.1 Hz	No	F	E
[36]	3 CCII+s, 1 Multiplier, 1 Adder	3R, 2C	Yes	10 Hz	No	F	S
[37]	3 OP-AMPs, 1 Integrator	3R, 2C	Yes	10 Hz	No	F	Both
[38]	4 AD844s, 1 OP-AMP, Varactor diode	5R, 1C	Yes	8 kHz	No	Both	Both
[39]	7 CCII, 2 Multipliers, 1 OP-AMP	6R, 2C	Yes	5 kHz	No	F	Both
[40]	7 OP-AMPs	14R, 3C	Yes	200 Hz	No	F	E
[41]	2 VDTA	1R, 2C	Yes	1 MHz	Yes	Both	Both
[42]	1 CBTA	1 M_R , 1C	No	250 Hz	Yes	F	S
[43]	9 OP-AMPs, 11 Multipliers	26R	Yes	140 Hz	No	F	Both
[44]	1 OTA, 1 CFOA, 2 CCIIIs, 1 Multiplier	7R, 2C	Yes	5 kHz	Yes	Both	Both
[45]	3 OP-AMPs	1 M_R , 6R, 1C	No	10 kHz	No	F	Both
[46]	2 VDTAs	2C	Yes	1.5 MHz	Yes	F	S
[47]	1 VDTA, 1 OTA	2C	Yes	3 MHz	Yes	G	S
[48]	3 OTAs	2C	Yes	10 MHz	Yes	G	S
[49]	2 CCIIIs	2R, 2C	Yes	700 kHz	Yes	G	Both
[50]	2 OP-AMPs	1 M_R , 3R, 1C	No	2 MHz	No	G	Both
[51]	1 VDCC	1 M_R , 1C	No	700 kHz	Yes	F	S
Proposed	1 VDBA, 1 CDBA	2C	Yes	3 MHz	Yes	G	S

6 Comparison

Table 3 shows a comparison of the meminductor and previously published circuits. Following key observations have been made:

1. The reported meminductor emulators in [25, 27, 28, 33, 35, 43, 50, 51] employ memristor, whereas the proposed meminductor design of the emulator is memristor-less.
2. Although the meminductor emulators suggested in [30-32, 34, 36, 39, 44] do not employ a memristor, they rely on analog multipliers and numerous other components, resulting in significant structural complexity. In contrast, the proposed meminductor emulator features a much simpler design.
3. The emulator designs demonstrated in [25, 33, 36, 37, 42, 44, 45, 49, 51] are simple but their frequency of operation is limited up to few Hz or kHz range while the meminductor emulator suggested in this paper, operates satisfactorily up to 3 MHz frequency, which is superior to the operating frequencies of most of the meminductors in Tab. 3.

7 Implementation of chaotic oscillator using meminductor

This section assesses the functionality of the suggested meminductor emulator by incorporating it into Chua's chaotic oscillator. This oscillator is recognized as one of the simplest electronic circuits capable of demonstrating chaotic behavior, which arises due to the inclusion of a nonlinear component [63]. In this study, the conventional nonlinear element is substituted with the proposed meminductor emulator, realized using CDBA and VDBA, to produce chaotic dynamics.

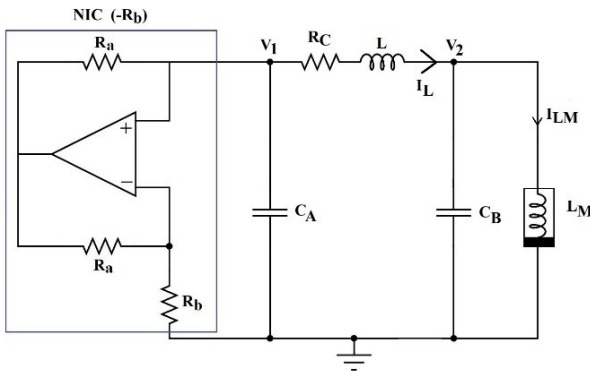


Fig. 15. Proposed chaotic oscillator

Figure 15 depicts the canonical configuration of Chua's oscillator constructed with the proposed meminductor, adopted form [64]. The circuit consists of a nonlinear element L_M , one resistor R_C , two capacitors C_A and C_B , an inductor L , and a negative resistor $-R_b$. The negative resistor has been implemented by op-amp based negative impedance converter (NIC) employing two equal resistors R_a , another resistor R_b and an op-amp. The NIC implementation for $-R_b$ resistor is depicted inside the black box in Fig. 15. For simulations, the nonlinear element L_M is replaced by the meminductor.

The state space dynamics of Chua's oscillator illustrated in Fig. 15 using 1st order differential analysis can be represented as follows:

$$\left. \begin{aligned} C_B \frac{dV_2}{dt} &= I_L - I_{LM}; & C_A \frac{dV_1}{dt} &= V_1 G - I_L \\ L \frac{dI_L}{dt} &= V_1 - R_C I_L - V_2; & \frac{d\phi_{LM}}{dt} &= V_2 \\ \frac{d\rho_{LM}}{dt} &= \phi_{LM} \end{aligned} \right\} \quad (29)$$

Here, C_A , C_B , L , R_C , and $G=1/R_b$ denote the capacitance, inductance, resistance, and conductance values of the respective components illustrated in Fig. 15. The current through meminductor I_{LM} is a function of ϕ and ρ , as derived in Eqn. (17) and can be represented as $I_{LM} = (A+B \rho_{LM})\phi_{LM}$. Here, A and B can be defined as:

$$A = \frac{K}{R_P C_1} (V_{SS} + V_{th}), \quad B = -\frac{K G_m}{R_P^2 C_1^2 C_2} \quad (30)$$

As depicted in Eqns. (29) and (30), replacing the conventional nonlinear element in a chaotic circuit with a meminductor enriches the state space dynamics, naturally increasing the system order without requiring additional discrete elements. This happens as a meminductor exhibits a flux-current relationship with inherent energy storage capability, which not only contributes nonlinearity but also adds a dynamic state associated with magnetic energy that depends on the past history of the system. This dual role enhances the system's effective dimensionality more naturally than any static nonlinear component (such as diodes or piecewise-linear resistors) or even compared to memristor, which is fundamentally resistive and dissipative in nature [63]. Meminductors based chaotic systems lead to more complex behaviors, including enhanced multi-stability and the possibility of rich dynamics, which are highly desirable for applications like secure communications. Moreover, meminductors enable compact circuit realization by reducing component count while still achieving strong nonlinearity, making them suitable for integrated and low-power designs. Their inherent tunability allows dynamic control over system para-

meters, facilitating flexible adjustment of chaotic regimes [64]. Overall, the introduction of a mem-inductor improves unpredictability, increases design efficiency, and enhances the robustness of chaotic circuits compared to traditional nonlinear implementations.

Assuming, $V_2=x$, $V_1=y$, $I_L=z$, $\phi_{LM}=w$, and $\rho_{LM}=v$, alongside mathematical manipulation leads to the modification in differential representation of Eqn. (29) as:

$$\left. \begin{aligned} \frac{dx}{dt} &= \frac{z}{C_B} - \frac{1}{C_B}(A + Bv)w; & \frac{dy}{dt} &= \frac{1}{C_A}(yG - z) \\ \frac{dz}{dt} &= \frac{1}{L}(y - R_C z - x); & \frac{d\omega}{dt} &= x; & \frac{dv}{dt} &= w \end{aligned} \right\} \quad (31)$$

Equation (31) can be represented in a simplified form as:

$$\left. \begin{aligned} \frac{dx}{dt} &= \alpha z - \xi w - \zeta v w; & \frac{dy}{dt} &= \beta y - \lambda z \\ \frac{dz}{dt} &= \gamma y - \delta z - \gamma x; & \frac{d\omega}{dt} &= x; & \frac{dv}{dt} &= w \end{aligned} \right\} \quad (32)$$

Here, $\alpha=1/C_B$, $\xi=A/C_B$, $\zeta=B/C_B$, $\beta=G/C_A$, $\lambda=1/C_A$, $\gamma=1/L$ and $\delta=R_C/L$.

Let Γ be the set that defines the equilibrium state of Eqn. (32). Then set Γ is defined as:

$$\Gamma = \{(x, y, z, \omega, v) | x = y = z = w = 0, v = c \text{ (any constant)}\} \quad (33)$$

The Jacobian matrix J associated with Eqn. (32) at equilibrium point given by Eqn. (33) is given as follows:

$$J = \begin{bmatrix} 0 & 0 & \alpha & -(\xi + \zeta c) & 0 \\ 0 & \beta & -\lambda & 0 & 0 \\ -\gamma & \gamma & -\delta & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \quad (34)$$

The Jacobian matrix, as defined in Eqn. (34), yields a characteristic equation as follows:

$$a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0 s^0 = 0 \quad (35)$$

where

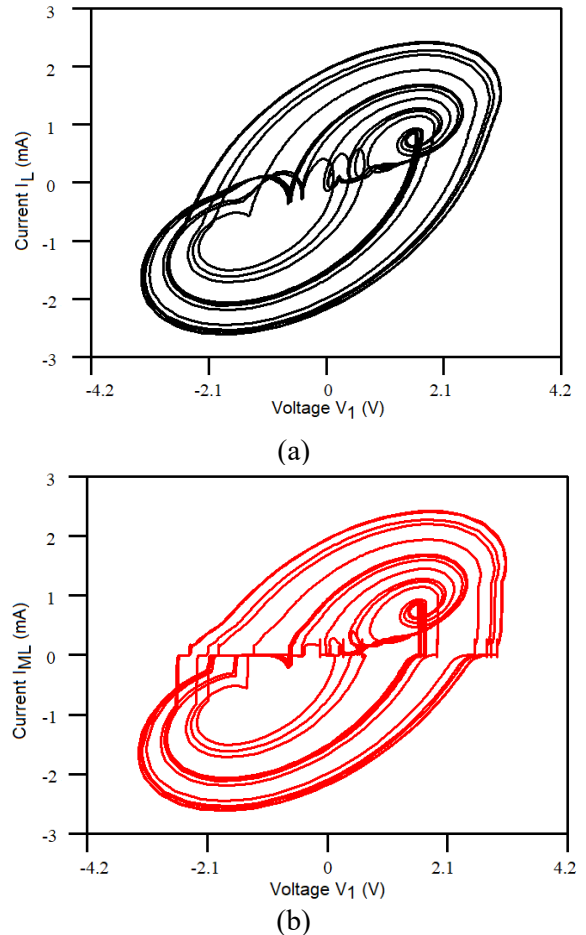
$$\begin{aligned} a_5 &= 1; & a_4 &= (\delta - \beta); & a_3 &= (\xi - \beta\delta + \alpha\gamma + \gamma\lambda + \zeta c); \\ a_2 &= (\delta\{\xi + \zeta c\} - \beta\{\xi + \alpha\gamma + \zeta c\}); & & & & \\ a_1 &= (\gamma\lambda\{\xi + \zeta c\} - \beta\delta\{\xi + \zeta c\}); & a_0 &= 0. \end{aligned} \quad (36)$$

The eigen values obtained from the characteristic equation of a chaotic oscillator are helpful in determining its chaotic behaviour. If the real parts of all eigen values are negative the trajectories of the system converge leading to a stable non-chaotic system. From Eqn. (36), it can be analyzed that the eigen values of the

introduced chaotic oscillator can be easily adjusted by choosing proper values of chaotic oscillator components (R_C , G , L , C_A , and C_B) to ensure non-negative real parts of one or more eigen values, producing chaos in the designed system. The characteristic equation can be further utilized to obtain the Routh-Hurwitz column values to determine instability of the system. For the system defined by Eqn. (35), the first column values of Routh array are specified by Eqn. (37).

$$\begin{aligned} \Delta_1 &= a_1, \\ \Delta_2 &= \frac{(a_1 a_2 - a_3)}{a_1}, \\ \Delta_3 &= \frac{(a_3 - a_1^2 a_4)}{(a_1 a_2 - a_3)}, \\ \Delta_4 &= a_4 \end{aligned} \quad (37)$$

The values (Δ_1 to Δ_4) represented by Eqn. (37) must be of same polarity for the system to be stable. Any change in the sign of the terms lead to an unstable system, a must characteristic for a system to be chaotic. By selecting appropriate component values, chaotic outputs are observed in the system. LTspice simulated outputs, illustrating the phase space trajectories for the variable pairs I_L-V_1 , $I_{LM}-V_1$, V_2-V_1 and V_2-I_L are presented in Fig. 16. The chosen component values for the simulation are $R_a=R_b=2 \text{ k}\Omega$, $C_A=65 \text{ nF}$, $C_B=10 \text{ nF}$, $L=120 \text{ mH}$, and $R_C=100 \Omega$.



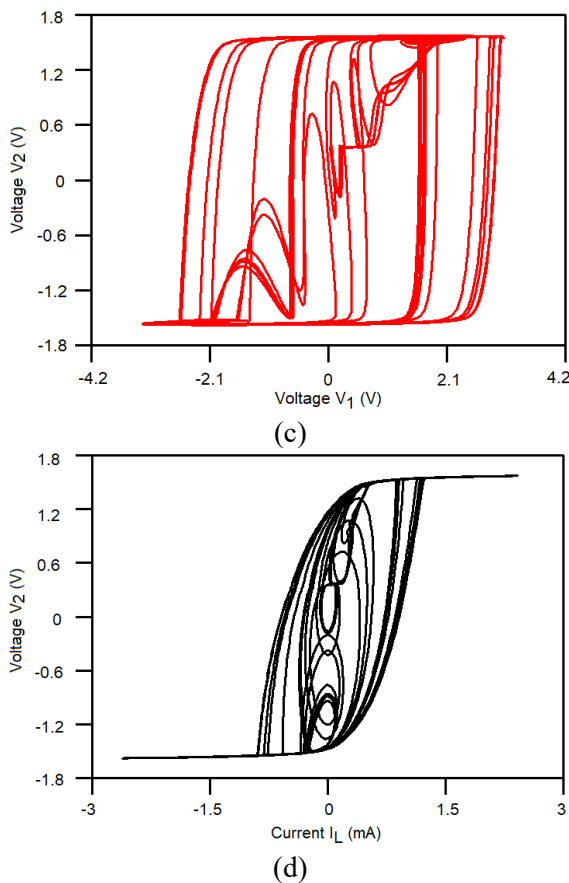


Fig. 16. Single-scroll phase space trajectories representing the dynamic behavior of the chaotic oscillator for (a) I_L vs. V_1 , (b) I_{LM} vs. V_1 , (c) V_2 vs. V_1 , (d) V_2 vs. I_L

8 Conclusion

In this study, a relatively simple and compact design for both incremental and decremental grounded meminductor emulator has been proposed. The suggested meminductor requires two grounded capacitors, VDBA and CDBA, while utilizing the internal parasitic resistances of the ABBs for its operation. Notably, the design avoids the use of analog multipliers or memristors. The correct functionality of the meminductor emulator has been verified through non-volatility tests, transient analysis, and the observation of pinched hysteresis loops. These hysteresis loops were obtained across various frequencies and capacitor values, demonstrating the emulator's dynamic behavior. Furthermore, a performance comparison with existing meminductor-based emulators highlights the key contributions in terms of design flexibility to switch between incremental and decremental modes, grounded external passive elements, usage of internal parasitic resistors, wide operational bandwidth up to 3 MHz, electronic tunability, and free from the requirement of bulky multipliers, complex memristors and passive resistors. The PVT and non-ideal analyses demonstrate the reliability of the design in real environment. The suc-

cessful integration of the emulator into a chaotic oscillator further confirms its practical viability. Moreover, the chaotic system mathematical analysis confirms its complex behavior and rich dynamics depicting a realization of 5th order chaotic system, while utilizing only three passive storage elements. Future work may focus on implementation of neuromorphic circuits and other memory-centric applications. Moreover, extending the proposed design for fractional domain can lead to realization of more complex futuristic paradigms.

References

- [1] L. Chua, "Memristor – the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.
- [2] M. Di Ventra, Y. V. Pershin and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, Oct. 2009.
- [3] Knowm, Inc.: Memristors: Knowm memristor technology. <https://knowm.org/memristors>. Accessed May 2024.
- [4] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurcation Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008.
- [5] T. Driscoll *et al.*, "Memristive adaptive filters," *Appl. Phys. Lett.*, vol. 97, no. 9, p. 093502, 2010.
- [6] F. Merrikh-Bayat and S. B. Shouraki, "Memristor-based circuits for performing basic arithmetic operations," *Procedia Comput. Sci.*, vol. 3, pp. 128–132, 2011.
- [7] J. Borghetti *et al.*, "Memristive switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.
- [8] W. Robinett *et al.*, "A memristor-based nonvolatile latch circuit," *Nanotechnology*, vol. 21, no. 23, pp. 235203, 2010.
- [9] H. Cao, Y. Wang, S. Banerjee, Y. Cao and J. Mou, "A discrete Chialvo-Rulkov neuron network coupled with a novel memristor model: Design, Dynamical analysis, DSP implementation and its application", *Chaos, Solitons & Fractals*, 179, pp. 114466, 2024.
- [10] Romero, F. J., Ohata, A., Toral-Lopez, A., Godoy, A., Morales, D. P., and N. Rodriguez, "Memcapacitor and meminductor circuit emulators: A review," *Electronics*, vol. 10, no. 11, 1225, 2021.
- [11] X. Liu, J. Mou, Y. Zhang and Y. Cao, "A new hyperchaotic map based on discrete memristor and meminductor: dynamics analysis, encryption application, and DSP implementation," *IEEE Transactions on Industrial Electronics*, 71(5), pp. 5094–5104, 2023.
- [12] F. Z. Wang, "Beyond memristors: Neuromorphic computing using meminductors," *Micromachines*, vol. 14, no. 2, pp. 486, 2023.
- [13] J. Wang, W. Huang, Z. Wang, J. Wang, and K. Chen, "DNA dynamic coding image encryption algorithm with a meminductor chaotic system," *Physica Scripta*, vol. 99, no. 9, p. 095231, 2024.
- [14] N. Yadav, S. K. Rai, and R. Pandey, "An electronically tunable meminductor emulator and its application in chaotic oscillator and adaptive learning circuit", *Journal of Circuits, Systems, and Computers*, vol. 32, no. 2, pp. 2350031-1-26, 2023.
- [15] A. Singh, D. Kim, H. Lee, and B.-G. Lee, "A high-frequency CMOS meminductor emulator for spiking neuron," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 72, no. 3, pp. 1056–1067, 2024.

- [16] A. Kalra, N. Pandey, and S. K. Rai, "Compact design of MOSFET-only meminductor emulator and its application in chaos and neural spike generator," *Integration*, p. 102740, 2026.
- [17] Y. Yin and Z. Li, "Meminductor synaptic coupling in a heterogeneous HR-FHN neuron network: Model, dynamics, and DSP implementation," *Chinese Physics B*, 2026.
- [18] H. Kim, M. P. Sah, C. Yang, S. Cho and L. O. Chua, "Memristor emulator for memristor circuit applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2422–2431, Oct. 2012.
- [19] C. Sánchez-López, J. Mendoza-López, M. A. Carrasco-Aguilar and C. Muñoz-Montero, "A floating analog memristor emulator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 309–313, 2014.
- [20] S. Gupta and S. K. Rai, "New grounded and floating decremental/incremental memristor emulators based on CDTA and its application," *Wireless Pers. Commun.*, vol. 113, pp. 773–798, 2020.
- [21] N. Yadav, S. K. Rai and R. Pandey, "Novel memristor emulators using fully-balanced VDBA and grounded capacitor," *Iran. J. Sci. Technol. Trans. Electr. Eng.*, 2021.
- [22] N. Yadav, S. K. Rai and R. Pandey, "New grounded and floating memristor emulators using OTA and CDBA," *Int. J. Circuit Theory Appl.*, vol. 48, pp. 1154–1179, 2020.
- [23] N. Yadav, S. K. Rai and R. Pandey, "High frequency electronically tunable floating memristor emulators employing VDGA and grounded capacitor," *Wireless Pers. Commun.*, 2021.
- [24] L. Chua, "If it's pinched it's a memristor," *Semicond. Sci. Technol.*, vol. 29, pp. 1–42, 2014.
- [25] Y. V. Pershin and M. D. Ventra, "Memristive circuits simulate memcapacitors and meminductors," *Electron. Lett.*, vol. 46, no. 7, pp. 517–518, 2009.
- [26] D. Biolek, V. Biolková and Z. Kolka, "Mutators simulating memcapacitors and meminductors," in *Proc. IEEE Asia Pacific Conf. Circuits Syst.*, pp. 800–804, 2010.
- [27] Y. V. Pershin and M. D. Ventra, "Emulation of floating memcapacitors and meminductors using current conveyors," *Electron. Lett.*, vol. 47, no. 4, pp. 243–244, 2011.
- [28] D. S. Yu, Y. Liang, H. H. C. Lu, and Y. H. Hu, "Mutator for transferring a memristor emulator into meminductive and memcapacitive circuits," *Chin. Phys. B*, vol. 23, no. 7, p. 070702, 2014.
- [29] Y. Liang, H. Chen, and D. S. Yu, "A practical implementation of a floating memristor-less meminductor emulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 299–303, 2014.
- [30] M. P. Sah, R. K. Budhathoki, C. Yang and H. Kim, "Charge controlled meminductor emulator," *J. Semicond. Technol. Sci.*, vol. 14, no. 6, pp. 750–754, 2014.
- [31] M. E. Fouda and A. G. Radwan, "Memristor-less current- and voltage-controlled meminductor emulators," in *Proc. 21st IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, pp. 279–282, 2014.
- [32] M. P. Sah, R. K. Budhathoki, C. Yang and H. Kim, "A mutator-based meminductor emulator circuit," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, pp. 2249–2252, 2014.
- [33] M. P. Sah, R. K. Budhathoki, C. Yang and H. Kim, "Mutator-based meminductor emulator for circuit applications," *Circuits Syst. Signal Process.*, vol. 33, pp. 2363–2383, 2014.
- [34] D. S. Yu, H. Chen and H. H. C. Lu, "A meminductive circuit based on floating memristive emulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, pp. 1692–1695, 2013.
- [35] D. Yu, Y. Liang, H. H. Lu and L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 758–762, 2014.
- [36] M. E. Fouda and A. G. Radwan, "Memristor-less current- and voltage-controlled meminductor emulators," in *Proc. 21st IEEE Int. Conf. Electron. Circuits Syst. (ICECS)* pp. 279–282, 2014.
- [37] S.-F. Wang, "The gyrator for transforming nano memristor into meminductor," *Circuit World*, vol. 42, no. 4, pp. 197–200, 2016.
- [38] D. Yu, X. Zhao, T. Sun, H. H. Lu, and T. Fernando, "A simple floating mutator for emulating memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1334–1338, 2019.
- [39] Q. Zhao, C. Wang, and X. Zhang, "A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit," *Chaos*, vol. 29, no. 1, p. 013141, 2019.
- [40] F. Yuan and Y. Li, "A chaotic circuit constructed by a memristor, a memcapacitor and a meminductor," *Chaos*, vol. 29, no. 10, p. 101101, 2019.
- [41] J. Vista and A. Ranjan, "High frequency meminductor emulator employing VDTA and its application," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 39, no. 10, pp. 2020–2028, 2019.
- [42] Z. G. C. Taşkıran, M. Sağbaş, U. E. Ayten, and H. Sedef, "A new universal mutator circuit for memcapacitor and meminductor elements," *AEU-Int. J. Electron. Commun.*, vol. 119, p. 153180, 2020.
- [43] F. Yuan, Y. Jin, and Y. Li, "Self-reproducing chaos and bursting oscillation analysis in a meminductor-based conservative system," *Chaos*, vol. 30, no. 5, p. 053127, 2020.
- [44] H. Sozen and U. Cam, "A novel floating/grounded meminductor emulator," *J. Circuits Syst. Comput.*, vol. 29, no. 15, p. 2050247, 2020.
- [45] F. J. Romero, A. M. Garcia, M. Escudero, D. P. Morales, and N. Rodriguez, "Design and implementation of a floating meminductor emulator upon Riordan gyrator," *AEU-Int. J. Electron. Commun.*, vol. 133, p. 153180, 2021.
- [46] K. Bhardwaj and M. Srivastava, "New electronically adjustable memelement emulator for realizing the behaviour of fully-floating meminductor and memristor," *Microelectron. J.*, vol. 114, 2021.
- [47] K. Kumar and B. C. Nagar, "New tunable resistorless grounded meminductor emulator," *J. Comput. Electron.*, vol. 20, pp. 1452–1460, 2021.
- [48] A. Raj, K. Kumar, and P. Kumar, "CMOS realization of OTA based tunable grounded meminductor," *Analog Integr. Circuits Signal Process.*, vol. 107, pp. 475–482, 2021.
- [49] N. Raj, R. K. Ranjan, F. Khateb, and M. Kumngern, "Mem-elements emulator design with experimental validation and its application," *IEEE Access*, 2021, doi: 10.1109/ACCESS.2021.3078189.
- [50] A. Singh and S. K. Rai, "Novel meminductor emulators using operational amplifiers and their applications in chaotic oscillators," *J. Circuits Syst. Comput.*, vol. 30, no. 12, pp. 2150219–1–20, 2021.
- [51] A. Singh and S. K. Rai, "VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit," *Iran. J. Sci. Technol. Trans. Electr. Eng.*, 2021, doi: 10.1007/s40998-021-00440-x.
- [52] N. Yadav, S. K. Rai, and R. Pandey, "New grounded and floating memristor-less meminductor emulators using VDTA and CDBA," *J. Circuits Syst. Comput.*, vol. 30, no. 15, 2021.
- [53] F. Kaçar and A. Yeşil, "New CMOS realization of voltage differencing buffered amplifier and its biquad filter applications," *Radioengineering*, vol. 21, no. 1, pp. 333–339, 2012.
- [54] B. Metin, K. Pal, and O. Cicekoglu, "CMOS-controlled inverting CDBA with a new all-pass filter application," *Int. J. Circuit Theory Appl.*, vol. 39, no. 4, pp. 417–425, 2011.

- [55] M. Faseehuiddin, N. Herencsar, S. Shireen, W. Tangsrirat and S. H. Md Ali, "Voltage Differencing Buffered Amplifier-Based Novel Truly Mixed-Mode Biquadratic Universal Filter with Versatile Input/Output Features", *Applied Sciences*, vol. 12, no. 3, pp. 1229, 2022. <https://doi.org/10.3390/app12031229>
- [56] T. S. Arora and S. Gupta "A new voltage mode quadrature oscillator using grounded capacitors: An application of CDBA," *Engineering science and technology, an International Journal*, vol. 21, no. 1, pp. 43-49, Feb. 2018.
- [57] D. M. Binkley, *Tradeoffs and optimization in Analog CMOS Design*. Wiley, New York, pp 377–476, 2008.
- [58] A. A. Tammam, K. Hayatleh, M. Ben-Esmael, N. Terzopoulos, and C. Sebu, "Critical review of the circuit architecture of CFOA", *International Journal of Electronics*, vol. 101, no. 4, pp. 441–451, 2014.
- [59] R. Chaisricharoen, B. Chipipop, & B. Sirinaovakul, "CMOS CCCII: Structures, characteristics, and considerations," *AEU - International Journal of Electronics and Communications*, vol. 64, no. 6, pp. 540–557, 2010.
- [60] A. Yeşil, F. Kaçar, and H. Kuntman, "New simple CMOS realization of voltage differencing transconductance amplifier and its RF filter application," *Radioengineering*, vol. 20, no. 3, pp. 632–637, Sep. 2011.
- [61] C. Acar and S. Ozoguz, "A new versatile building block: Current differencing buffered amplifier suitable for analog signal-processing filters," *Microelectronics Journal*, vol. 30, no. 2, pp. 157–160, 1999.
- [62] D. Biolek, Z. Biolek, and V. Biolkova, "SPICE modeling of memristive, memcapacitive and meminductive systems," in *Proc. Eur. Conf. Circuit Theory Design*, pp. 249–252, 2009.
- [63] B. Muthuswamy and L. O. Chua, "Simplest chaotic circuit," *Int. J. Bifurcation Chaos*, vol. 20, no. 5, pp. 1567–1580, 2010.
- [64] M. Itoh and L. O. Chua, "Memristor oscillators," *Int. J. Bifurcation Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008.

Received 5 February 2026