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Mutually coupled body bias low noise amplifier using output transformer matching for 5G communication

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This manuscript presents the realization of low noise amplifier (LNA) for the sub 6 GHz applications having frequency range of 5.7 to 7 GHz with the bandwidth 1.3 GHz. The realized LNA uses the common gate topology decreasing the reflections at the input, i.e., to decrease the S_{11} parameter, cascode topology is used to enhance the gain of the circuit while source follower topology is used to for the output impedance matching and transformer matching is employed to further enhance the S_{22} parameter. The body biasing for the connected MOS is done through the RL circuit connected between body and drain. The realized LNA has a maximum gain value of 11.35 dB, minimum S_{11} value of –22.35 dB, minimum NF value of 2.08 dB and minimum S_{22} value of –10.06 dB at 6.03 GHz. The process corner simulation for the slow-slow and fast-fast corners are also done and observed that LNA parameters values are under the range. The realized LNA consumes V_{DD}=1.8 V, with current consumption of 11.40 mA, i.e., having power consumption of 20.52 mW.

Keywords: Common Gate, Body Bias Noise Figure

1 Introduction

The researchers are focusing on the development of LNA circuits which consume low power, high gain, wide bandwidth, low NF and small area. Although there is always trade-off between these parameters, the overall figure of merit should be as high as possible. In [1], the proposed LNA uses active and passive enhancement techniques for 6 GHz band. The LNA has an area of 0.42 mm^2, a gain of 14.5 dB with NF of 3.2 dB. In [2], the 6 GHz LNA uses a simultaneous input and noise matching technique. The LNA has a 27.6 dB peak gain and 0.66 dB NF for 4.2-5.2 GHz range. In [3], the realized LNA simulated using 22 nm CMOS technology has a gain of 15.7 dB with NF of 1.46-1.96 dB. The realized LNA proposed a magnetically coupled resonator matching network in which the impedance rises with frequency. Paper [4] presented a balun LNA which included an inductive source degenerated LNA with active feedback circuit. The LNA attained gain was 25.9 dB with NF of 4.25 dB. In [5], the inductor-less gm-boosted LNA was proposed which uses NMOS-PMOS configurations for increasing the transconductance and henceforth the gain of circuit. The 0.18 µm CMOS process technology was used for fabrication and the maximum gain achieved was 19.6 dB with NF of 3.6 dB. In [6], the common source resistive feedback with a series inductive peaking technique was proposed. The realized LNA [6] had a variable gain circuit, the gain is varied according to the input power level. The achieved gain is 15-25 dB while NF is 2-3.8 dB depending on the power level at input. The bandwidth is 2.5-6.5 GHz with chip area of 0.35 mm^2. In [7], the CS and CG balun LNA was proposed for 2.4 GHz applications. The LNA uses current reuse circuit to lower the power consumption and inductive source degeneration to linearize the circuit, i.e., to increase the third order input intercept point. The realized LNA occupied an area of 1.3 mm^2. In [8], the resistive-feedback-tuning technique was proposed of the realized LNA which a gain of 106 dB in 6 dB steps with NF of 2.1 dB and 37.1 dB image rejection ratio. In [9], cascode and folded-cascode inductor source degeneration LNA was proposed for 2.4 GHz frequency. The proposed LNA has improved the IIP3 value having the functionality of variable gain circuit. The gain is 11.8 dB, input reflection coefficient is −31.8 dB NF of 1.1 dB for the high gain condition while having gain of 5.0 dB. The input reflection coefficient is −14.4 dB, NF is 1.96 dB for the low gain condition. In [10], the authors proposed gain variable circuits and an automatic gain control circuit to make the output voltage constant. The resistive feedback LNA topology is used to optimize the input matching as well as Butterworth filter is used to attenuate the interferences. The receiver has a gain in the range of 9.1-91.9 dB and NF ranges from 2.4-3.4 dB for 2-6 GHz frequency range. In [11], the current reuse LNA is proposed for 5-6 GHz frequency used in the wireless local area network. The realized LNA has a gain of 39 dB and NF of 1.9 dB. In [12], the LNA uses two circuits named diode connected and cascode post

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distortion circuits are used differently to check their performances in linearity. The cascode post distortion circuit has IIP3 of 1.5 dBm while the diode connected post distortion circuit has IIP3 of 10 dBm. There is a trade-off between the LNA parameters [13-14].

In this paper, circuit design is discussed in Section 2 and elaborates the parameters discussion along with their mathematical analysis. Simulation results are discussed in Section 4.

2 Circuit design

The realized mutually coupled body bias LNA using transformer matching at the output is shown in Fig. 1. The common gate configuration is used at the input to improve the input impedance matching. MOS M_2 is connected in the common gate configuration with body to drain biasing using L_5 and R_3. The buffer circuit is used at the output using M_3 MOS. R_1 and L_1 combinations are used at drain of MOS M_1 for bias stabilization and high impedance at RF, thus to prevent the signal leakage to V_{DD}. M_1 is also acting as a transconductance boosting and noise cancellation stage. Inductor L_2 serves as a source degeneration circuit so as to linearize, thus to cancel out the parasitic capacitances. Inductors L_3 and L_4 act as inductor matching at the input side so as to reduce the input reflections. MOS M_3 serves as a buffer circuit. Common collector configuration is used for output impedance matching. There is a coupling between inductors L_1 and L_7 with a coupling coefficient of 0.66.

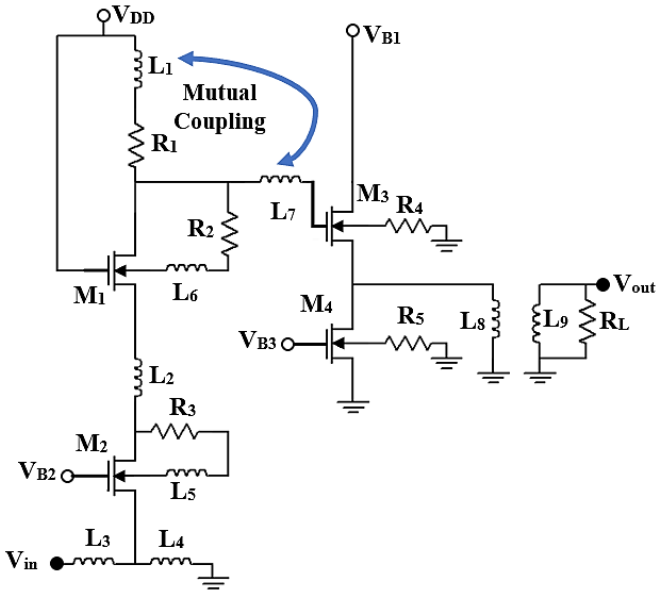

Fig. 1. Realized mutually coupled body bias LNA circuit

Figure 2 shows the small signal model for the realized LNA. Here, $i_x=g_{mx}v_{gsx}$ and $i_y=g_{mby}v_{bsy}$ where x=1,2,3,4 and y=1,2,3,4.

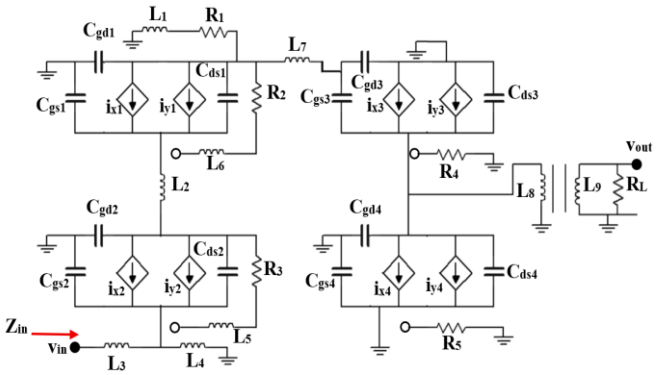

Fig. 2. Small signal model of realized LNA

Table 1 lists the components used in the realized low noise amplifier.

Table 1. Component dimensions for the realized LNA

M_1	(42×2) µm/180 µm	R_1	30 Ω
M_2	(53×4) µm/180 µm	R_2	11 kΩ
M_3	(32×2) µm /180 µm	R_3	11 k Ω
M_4	(32×2) µm /180 µm	R_4	1.3 kΩ
L_1	3.2 nH	R_5	1.3 kΩ
L_2	2.85 nH	V_{DD}	1.8 V
L_3	260 pH	L_5	80 pH
L_4	6.3 nH	L_6	80 pH
k	0.66	L_7	1.2 nH

2.1 Input impedance

The input impedance for the realized LNA looking into MOS M_2 is given as

$$Z_{in,M2} = \frac{1}{(g_{m2} + g_{mb2}) + j\omega C_{gs2}} \tag{1}$$

where

$$\omega C_{gs2} \ll (g_{m2} + g_{mb2})$$

$$Z_{in,M2} \approx \frac{1}{g_{m2} + g_{mb2}} \tag{2}$$

and hence

$$Z_{in}(\omega) = j\omega L_4 || \left(\frac{1}{g_{m2} + g_{mb2}} + \frac{1}{g_{m1} + g_{mb1}} + j\omega L_2\right) + j\omega L_3 \tag{3}$$

The effective transconductance of MOS M_1 and M_2 is given $g_{m,\text{eff}} = g_{m2} + g_{mb2}$. As given in equations, the input impedance for common gate MOS M_2 is approximately a real part which make sense of using this topology for wideband input impedance matching. Now real part can be adjusted to get the 50 Ω impedance matching.

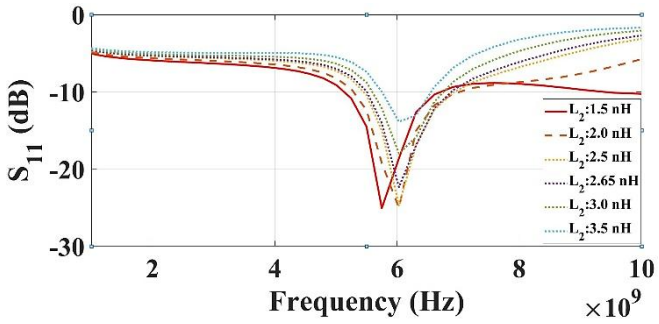

Fig. 3. S_{11} vs frequency with respect to inductor L_2

Figure 3 shows S_{11} with respect to variations in the values of inductor L_2. It can be observed that for L_2=2.5 nH, the input reflection coefficient is less than –9 dB for the frequency range of 5.3 GHz to 7.5 GHz, i.e., having the bandwidth of 2.2 GHz. For the lower values of L_2 the input reflection coefficient has a smaller bandwidth while for the higher values of L_2 the input reflection coefficient gets degraded. Hence, the optimum value is obtained for L_2=2.5 nH.

2.2 Gain calculations

The voltage gain expression for the realized LNA is given as

$$A_v = g_{m,\text{eff}} Z_L \tag{4}$$

where Z_L is the load impedance looking at the drain of MOS M_1 which is given as $Z_L = j\omega L_7 + (R_L||r_{o3}||r_{o4})$. So, putting all the values, the gain is calculated as

$$A_v = (g_{m2} + g_{mb2} + \alpha g_{m1})\left(j\omega L_7 + (R_L||r_{o3}||r_{o4})\right) \tag{5}$$

where α is the coupling via inductor L_2. As shown in Fig. 4, the gain has a maximum value with maximum bandwidth for L_2=2.5 nH while for lower and higher values of L_2, the obtained gain decreases for higher frequencies.

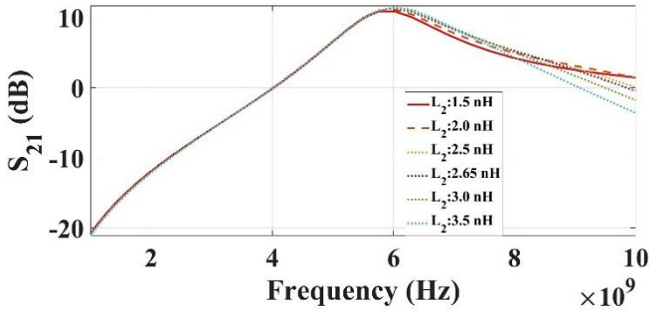

Fig. 4. S_{21} vs frequency with respect to inductor L_2

2.3 Noise analysis

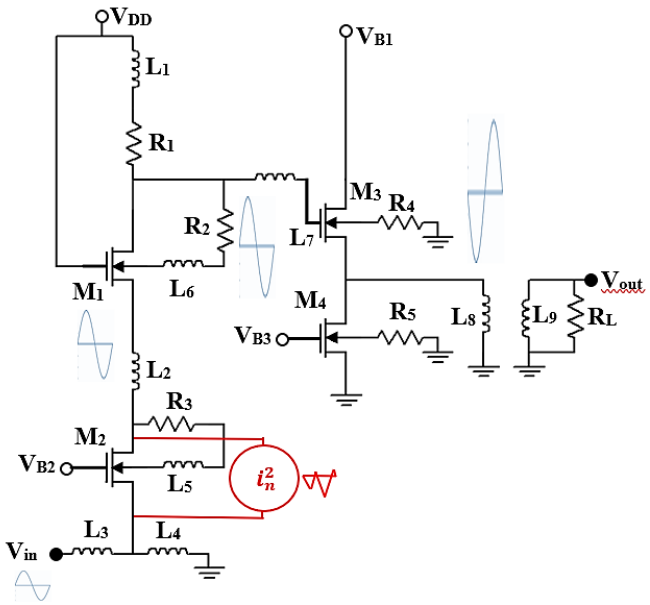

Fig. 5. Noise analysis for realized LNA

The noise analysis for the realized LNA is shown in Fig. 5. The thermal drain noise current of MOS M_2 is given by $\overline{i_n^2} = 4KT\gamma g_{m2}$, while the input referred noise voltage is given by

$$\overline{v_{n,in}^2} = \frac{4KT\gamma\Delta f}{g_{m2}}.$$

Similarly, the noise analysis can be done for the realized LNA through the calculation of noise contribution of all connected noise generated components. The noise factor is given by

$$NF = 1 + \frac{\text{noise added by circuit}}{\text{source noise}} \tag{6}$$

$$NF = 1 + \frac{\dfrac{4kT\gamma(g_{m2} + g_{mb2})}{\left(g_{m,\text{ eff}}\right)^2}}{4kTR_S} \tag{7}$$

$$NF = 1 + \frac{\gamma(g_{m2} + g_{mb2})}{(g_{m2} + g_{mb2} + \alpha g_{m1})^2 R_S} \tag{8}$$

The NF obtained for different values of L_2 is depicted in Fig. 6. One can see that for higher values of L_2 the bandwidth is getting decreased while for lower values also the bandwidth is smaller. For L_2=2.5 nH, the optimum value of NF is obtained.

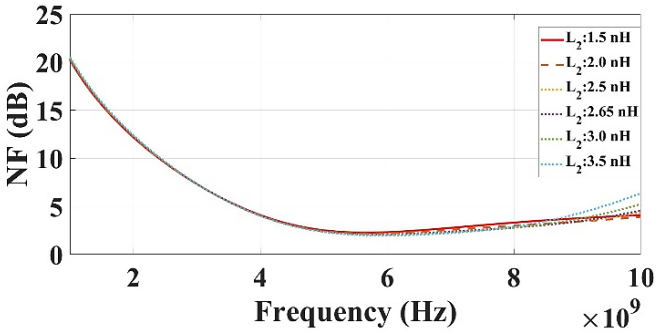

Fig. 6. NF vs frequency with respect to inductor L_2

2.4 Linearity analysis

The non-linear terms in the circuit changes the output voltage of the circuit. The output voltage for an amplifier is given as

$$v_o = c_o + c_1 v_{in} + c_2 v_{in}^2 + c_3 v_{in}^3 + \cdots \quad (9)$$

where

$$v_{in} = y_1 + y_2 = A\cos(2\pi f_1 t) + B\cos(2\pi f_2 t) \quad (10)$$

Equation (9) can be written as

$$v_o = c_o + c_1(y_1 + y_2) + c_2(y_1 + y_2)^2 + c_3(y_1 + y_2)^3 + \cdots \quad (11)$$

$$v_o = c_o + c_1(y_1 + y_2) + c_2({y_1}^2 + {y_2}^2 + 2y_1y_2) + c_3({y_1}^3 + {y_2}^3 + 3{y_1}^2y_2 + 3y_1{y_2}^2) + \cdots \quad (12)$$

The cubic term generates IM3 components at $2f_1 - f_2$ and $2f_2 - f_1$. Hence, the IIP3 value can be given as

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{c_1}{c_3}\right|} \quad (13)$$

3 Simulation environment and biasing details

The realized circuit is simulated using GPDK 0.18 µm CMOS technology in Cadence Virtuoso Software. The realized LNA has these biasing details: V_{DD}=1.8 V, I_{M1}=I_{M2}=11.40 mA, I_{M3}=2.81 mA. The circuit is drawn on Virtuoso Schematic Editor. MOSFETs M_1, M_2 and M_3 are operating in the saturation region, i.e., having region 2 for DC analysis in Analog Design Environment setup in Cadence. The 0.18 µm CMOS technology is used because of its high reliability, stability, lower leakage power, ease of design and debugging, better tolerance to high voltage, temperature, etc.

4 Results and discussion

Figure 7(a) shows the NF simulation results for the realized LNA. The minimum NF value is 2.15 dB at 6.03 GHz for Slow-Slow corner while for Fast-Fast corner, its value is 2.93 dB, and 2.08 dB for typical corners.

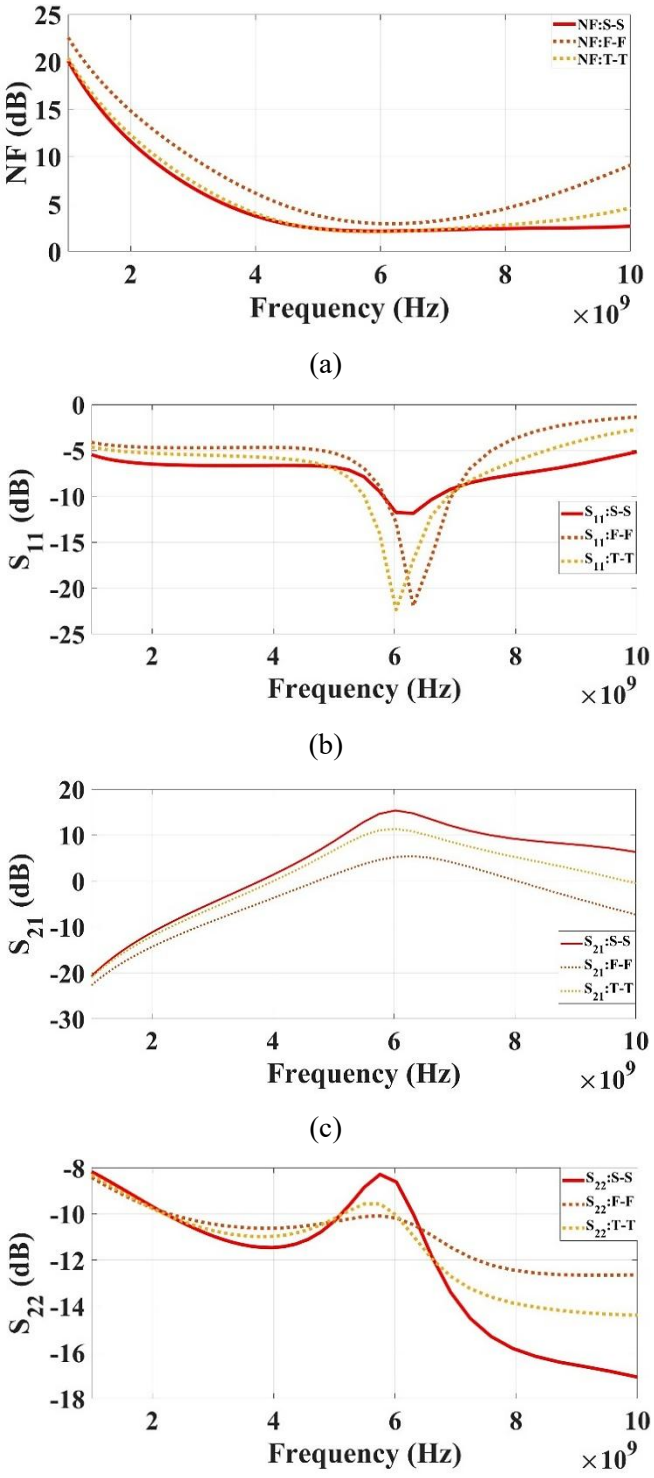

Fig. 7. Process corner simulation results: (a) NF, (b) S_{11}, (c) S_{21}, (d) S_{22} for the realized LNA

Figure 7(b) depicts the input reflection coefficient for the realized LNA circuit. The S_{11} value is less than –9 dB for the 5.7 to 7 GHz, i.e., having a bandwidth of 1.3 GHz for the typical corner while having minimum value of –22.35 dB at 6.03 GHz. The Slow-Slow and Fast-Fast corners also have the S_{11} values in the limited range.

The gain of the realized LNA is displayed in Fig. 7(c) which shows that the maximum value of gain is 15.36 dB at 6.03 GHz for Slow-Slow corner and 11.35 dB for a typical corner. The output reflection coefficient is also lower than –9 dB for the desired band of interest.

The layout for the realized LNA is shown in Fig. 8. The realized LNA has an area of 471.70×280.40 μm^2, thus 0.132 mm^2.

Table 2 shows the comparison of realized LNA parameters with other references.

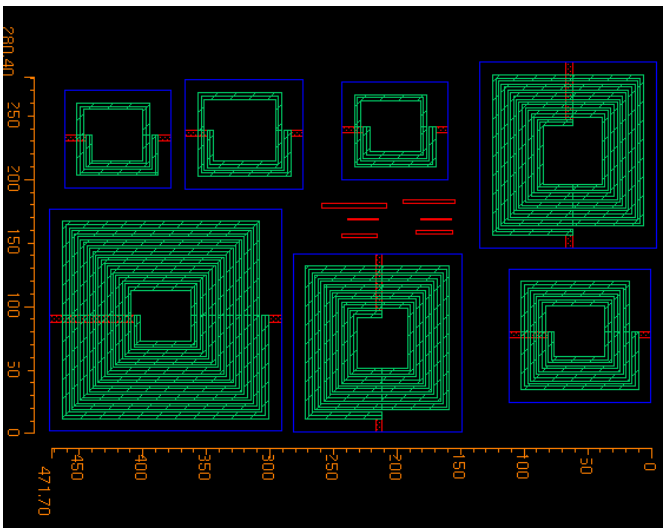

Fig. 8. Layout of the realized LNA

Table 2. Comparison with other references

Reference	Bandwidth (GHz)	V_{DD} (V)	Maximum gain (dB)	NF (dB)	Power (mW)	Technology
[15]	0.2-3.8	1	19	2.8-3.4	5.7	130 nm
[16]	0.1-5.3	1	10.5	2.7-3.3	13.7	65 nm
[17]	0.1-1.3	2	10	2.9-3.2	18	180 nm
[18]	0.6-4.2	0.5	14	4-4.5	0.25	130 nm
[19]	2-5	1.8	13	6-8	1.8	180 nm
This work	5.7-7	1.8	11.35	2.07-2.32	20.52	180 nm

5 Conclusion

The realized LNA suitable for sub-6 GHz applications has been analysed for frequency range of 5.7-7 GHz with a bandwidth of 1.3 GHz. The LNA combines a common-gate input stage for effective input impedance matching and reduced reflection coefficient, a cascode configuration to enhance the overall gain, and a source-follower stage for output impedance matching. Transformer-based matching further improves the output return loss, while RL-based body biasing ensures to decrease the threshold voltage of MOS. Simulation results demonstrate that the LNA achieves a maximum gain of 11.35 dB, a minimum input reflection coefficient S_{11} of –22.35 dB, a minimum NF of 2.08 dB, and a minimum output reflection coefficient S_{22} of –10.06 dB at 6.03 GHz. Process corner analysis under slow-slow and fast-fast conditions checked the robustness of the LNA design, with all key performance parameters remaining within acceptable limits. The LNA operates from a 1.8 V supply, consuming 11.40 mA of current, resulting in a total power consumption of 20.52 mW.

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