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Design and stochastic performance analysis of non-ideal ultra-lift Luo converter: A Monte Carlo approach

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This paper presents the design and a comprehensive stochastic performance assessment of the non-ideal Ultra-Lift Luo (ULL) converter. The study emphasizes the impact of component tolerances and non-idealities on the uncertainties induced in the overall performance of the ULL converter, which is systematically evaluated using a Monte Carlo-based simulation framework. Unlike conventional deterministic analyses based on nominal component values, the proposed methodology develops a non-ideal model of the ULL converter by accounting for inductor winding resistance R_L, capacitor equivalent series resistance r_C, and MOSFET non-idealities, such as ON-state resistance $R_{DS_{\mathrm{ON}}}$, gate charge Q_G, drain-source voltage V_{DS}, drain-source current I_{DS} and load resistance R_0. Monte Carlo analysis is employed to evaluate the effects of component tolerances and non-idealities on the output voltage ripple, output-voltage stress and efficiency of the non-ideal ULL converter, demonstrating the sensitivity and robustness of the non-ideal ultra-lift topology under practical manufacturing variations.

Keywords: stochastic analysis, ultra-lift Luo converter, Monte Carlo, non-idealities

1 Introduction

High-step-up non-isolated DC-DC converters are widely used in photovoltaic (PV) interfaces, fuel cell systems, electric vehicle (EV) auxiliaries, and distributed DC buses. Conventional boost and cascaded/stacked topologies suffer from large duty cycles, high switch stress, and poor efficiency at high gain, motivating the development of advanced architectures, such as switched-inductor, switched-capacitor, and Luo-type converters. Luo introduced the voltage-lift (VL) technique as a systematic method to enhance the voltage transfer ratio by successively lifting the output through capacitive stages. This approach led to a family of Luo converters, including positive and negative output, self-lift, re-lift, and multiple-lift structures, all targeting higher gain with improved dynamic behavior and reduced parasitic effects compared to the classical boost converter [1]. Building on the VL and super-lift (SL) concepts [2-3], the Ultra-Lift Luo (ULL) converter was proposed as a topology capable of extremely high voltage gain using cascaded lift cells, without proportionally increasing the device voltage stress. Luo and Ye demonstrated that the ultra-lift (UL) technique yields a gain that grows faster than linearly with the number of stages, making the topology attractive for high step-up applications where efficiency and stress constraints are critical [4]. Recently, Sahoo et al. developed a non-ideal mathematical model of the ULL converter that systematically incorporates the parasitic resistances of inductors and capacitors, as well as switch and diode non-idealities, and other practical effects. Their work provides averaged models and small-signal representations suitable for control and performance analysis under realistic conditions [5]. On the control side, multiple works have proposed advanced controllers for ULL converters. In addition, Sharifian et al. introduced a type-2 fuzzy neural controller to enhance the transient performance and robustness of a ULL converter, demonstrating a faster response and reduced overshoot compared to conventional controllers [6]. Gani proposed a robust adaptive DC-voltage regulator based on a PD interval type-2 TSK fuzzy controller for the ULL converter, targeting uncertain input and load variations. Simulation results showed improved dynamic behavior and robustness compared to a type-1 fuzzy controller [7]. In the context of sustainable energy applications, Kumar and Jayalakshmi modeled an ULL converter controlled by a conventional PI regulator for stand-alone operation [8]. In a broader perspective, Kevat et al. presented a comprehensive, design-oriented study on non-isolated DC-DC converters for maximum power point tracking (MPPT) in stand-alone photo-

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voltaic systems, emphasizing voltage gain capability, efficiency, and MPPT suitability [9]. Other studies have analyzed the stability and dynamic behavior of ultra-lift and related Luo converters, including chaos suppression and bifurcation analysis, further confirming that high-gain Luo topologies can exhibit complex dynamics when operated near their limits [10]. However, even in these works, component tolerances are typically treated deterministically or through limited parametric sweeps, rather than via a rigorous stochastic framework. In practical converters, component values often deviate from their nominal values due to manufacturing tolerances, temperature variations, aging, and environmental effects. These parametric uncertainties affect voltage gain, ripple, efficiency, and stress margins. Traditional tolerance analysis in analog and power circuits has relied on worst-case or root-sum-square (RSS) methods, which provide conservative bounds but do not reveal the full probabilistic behavior of the system. Application notes from industry (e.g., Texas Instruments, Analog Devices) discuss worst-case, RSS, and Monte Carlo tolerance methods and highlight that Monte Carlo simulations are often more realistic for design centering and yield estimation [11]. In the context of DC-DC converters, recent work has addressed tolerance analysis explicitly [12]. Vacheva et al. conducted a detailed tolerance analysis of a boost DC-DC converter, highlighting the impact of component spreads on output behavior and stability, and explicitly employed Monte Carlo simulation as one of the core techniques [13]. Similar methodologies have been used in resonant and inductive power transfer (IPT) converters, where detuning due to tolerances can severely degrade performance. López-Alcolea et al. employed Monte Carlo simulation to investigate the impact of component tolerances on series and inductor-capacitor-capacitor (LCC) compensation networks in IPT systems, demonstrating how statistical analysis reveals performance dispersion and informs robust design [14]. Beyond single converters, reliability-oriented research in power electronics increasingly employs stochastic models and Monte Carlo simulation for lifetime and failure-rate estimation of semiconductor devices and converter systems [15]. Novak et al. reviewed Monte Carlo-based reliability estimation methods for power devices, comparing static and dynamic parameter variation approaches and showing that simplistic static methods can significantly misestimate lifetime distributions [16]. Similar Monte Carlo frameworks have been applied to modular multilevel converters and DC shipboard power systems to capture the impact of uncertainty on system reliability [17, 18]. These works demonstrate a growing awareness that probabilistic, rather than purely deterministic, analysis is necessary to assess converter performance and reliability under real-world variations accurately. Gajda and Sidor presented one of the earlier practical demonstrations of Monte Carlo analysis for electronic converters, using it to compare the sensitivity of different converter structures to component tolerances and to identify architectures with lower error under variation [19]. In power electronics and power systems, Monte Carlo-based stochastic analysis has been employed for probabilistic power flow analysis, voltage variation assessment, and techno-economic evaluation under uncertainty, thereby reinforcing the method's suitability for complex nonlinear systems with multiple uncertain parameters [20-22].However, most of these Monte Carlo applications target system-level networks (microgrids, feeders, PV inverters, IPT systems) or generic electronic structures, rather than high-gain, strongly nonlinear DC-DC converters such as the ULL. At the converter level, published work tends to focus on time-domain simulations with fixed parameter sets, small-signal models around nominal points, or limited parametric sweeps, which do not fully exploit the power of stochastic simulation. Despite these developments, no comprehensive Monte Carlo based stochastic analysis of the ULL converter exists in the literature. Existing ULL converter studies primarily focus on control, modeling, or steady-state analysis at nominal conditions. From the literature, these are summarized:

- High-gain Luo type converters are well established with numerous analyses on topology, non-ideality, and control.
- Component tolerance and non-ideality analysis using the Monte Carlo method provides superior insight compared with deterministic analyses.
- No study has systematically applied a Monte Carlo component tolerance framework to the non-ideal ULL converter.

These gaps motivate the contributions of this work as follows:

- developing a rigorous Monte Carlo component tolerance analysis for the non-ideal ULL converter,
- quantifying variations in output voltage ripple, output voltage stress and efficiency,
- component selection is of critical importance.

The remainder of this paper is organized as follows. Section 2 presents the non-ideal ULL converter model. Section 3 details the Monte Carlo Simulation procedure. In Section 4, a comprehensive simulation framework is developed to validate the Monte Carlo Simulation procedure for the non-ideal ULL converter. Finally, Section 5 concludes the paper and outlines directions for future research.

2 Non-ideal ULL converter model

This section presents the basic circuit analysis and operating principle of the non-ideal ULL converter, which constitutes a fourth-order dynamic system comprising two inductors and two capacitors. The schematic diagram of the non-ideal ULL converter is illustrated in Fig. 1. Throughout the analysis, the converter is assumed to operate in continuous conduction mode (CCM) with duty cycle d and switching period T_s [4].

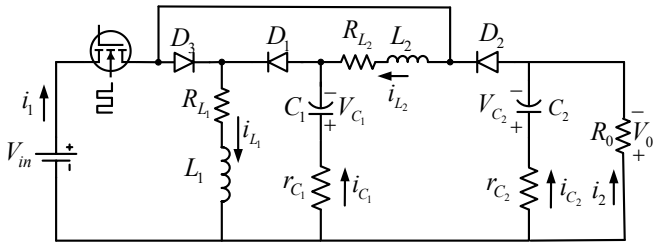

Fig. 1. The basic circuit topology of a non-ideal ULL converter

The converter comprises inductors L_1 and L_2, diodes D_1, D_2, and D_3, capacitors C_1 and C_2, an input voltage source V_{in}, and a load resistance R_0. The non-idealities considered in this analysis include the inductor winding resistances R_{L1} and R_{L2} associated with inductors L_1 and L_2, respectively. The equivalent series resistances (ESRs) of capacitors C_1 and C_2 are denoted by r_{C1} and r_{C2}, respectively. MOSFET non-idealities are represented by ON-state resistance $R_{DS\,ON}$, gate charge Q_G, drain-source voltage V_{DS}, and drain-source current I_{DS}. Under CCM operation, the converter exhibits two distinct switching intervals: (i) the ON state and (ii) the OFF state.

ON State: During the interval $0 \le t < dT_s$, the power switch is turned ON, causing diodes D_1 and D_2 to become reverse biased, while diode D_3 is forward biased**.** During this interval, the switch on-state resistance $R_{DS\,ON}$ is also effective. Inductors L_1 and L_2 are energized (charged), whereas the capacitor C_2 supplies energy to the load resistance R_0. The equivalent circuit corresponding to the ON state is depicted in Fig. 1(a).

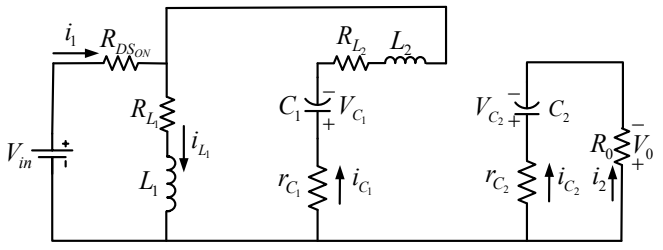

Fig. 1(a). Equivalent circuit during ON state

OFF State**:** During the interval $dT_s \le t < T_s$, the power switch is turned OFF, resulting in diodes D_1 and D_2 becoming forward biased, while diode D_3 is reverse biased. In this interval, inductors L_1 and L_2 release their stored energy, thereby charging capacitors C_1 and C_2 and simultaneously supplying energy to the load resistance R_0. The equivalent circuit corresponding to the OFF state is illustrated in Fig. 1(b) [5].

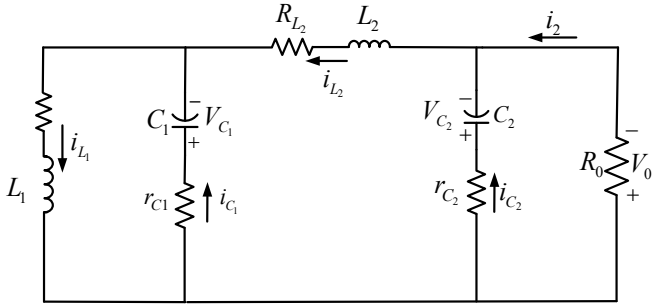

Fig. 1(b). Equivalent circuit during the OFF state

The ULL converter is modeled using its switching behavior under CCM. For a converter containing *N* lift stages, the static gain under ideal conditions is given by:

$$G_{ideal} = \frac{V_0}{V_{in}} = 1 + \frac{d}{1+d}\sum_{k=1}^{N} a_k \tag{1}$$

where d is the duty cycle and α_k represents the lift coefficient contributed by stage k. The expression for the efficiency of the non-ideal ULL converter in terms of the non-idealities present in the converter can be derived as follows:

$$\eta = \frac{P_0}{P_{in}} = \frac{V_0 i_2}{V_{in} i_1} \tag{2}$$

3 Monte Carlo simulation procedure

For manufacturing tolerances of ULL converter, capacitors C_1 and C_2 and equivalent series resistances ESRs r_{C1} and r_{C2}, inductors L_1 and L_2 and winding resistances R_{L1} and R_{L2}, and load resistance R_0 are modeled with manufacturing random tolerance deviations as follows:

$$L'_1 = L_1(1 + \delta_{L_1}) \tag{3}$$

$$L'_2 = L_2(1 + \delta_{L_2}) \tag{4}$$

$$C'_1 = C_1(1 + \delta_{C_1}) \tag{5}$$

$$C'_2 = C_2(1 + \delta_{C_2}) \tag{6}$$

$$R_{L'_1} = R_{L_1}(1 + \delta_{R_{L_1}}) \quad (7)$$

$$R_{L'_2} = R_{L_2}\left(1 + \delta_{R_{L_2}}\right) \quad (8)$$

$$ESR'_{C_1} = ESR_{C_1}(1 + \delta_{C_1}) \quad (9)$$

$$ESR'_{C_2} = ESR_{C_2}(1 + \delta_{C_2}) \quad (10)$$

$$R'_0 = R_0(1 + \delta_{R_0}) \quad (11)$$

where δ terms represent random tolerance deviations. Circuit components of a non-ideal ULL converter with nominal and manufacturing tolerance values are given in Tab. 1.

Table 1. The circuit components of a non-ideal ULL converter with nominal and manufacturing tolerance values

Components	Symbol	Nominal	Tolerance
Inductor	L_1	1 mH	%20
Winding resistance	R_{L_1}	20 mΩ	%20
Inductor	L_2	1 mH	%20
Winding resistance	R_{L_2}	20 mΩ	%20
Capacitor	C_1	1 µF	%20
ESR	r_{C_1}	2×10^{-4} Ω	%20
Capacitor	C_2	1 µF	%20
ESR	r_{C_2}	2×10^{-4} Ω	%20
Input voltage	V_{in}	12 V	-
Nominal output voltage	V_0	– 63 V	-
Load	R_0	500 Ω	%5
Switching frequency	f	50 kHz	-
Duty cycle	d	0.6	-
Nominal output current	I_0	126 mA	-

The manufacturing component tolerances were assigned based on manufacturer specifications.

4 Monte Carlo simulation procedure for non-ideal ULL converter

The flowchart for the Monte Carlo Simulation procedure of the non-ideal ULL converter is presented below.

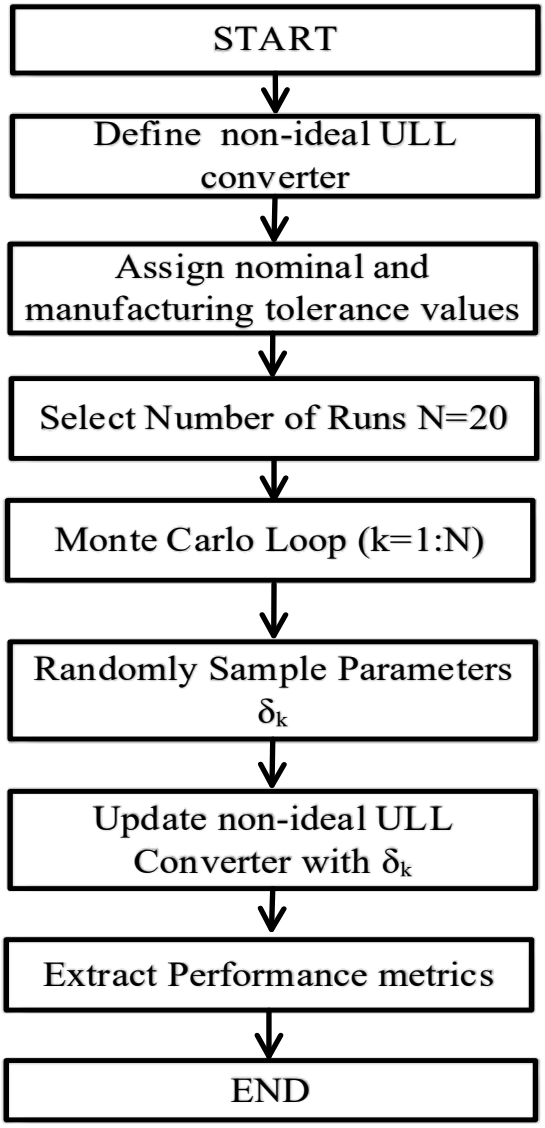

Fig. 2. The flowchart of the Monte Carlo simulation procedure for the non-ideal ULL converter

For each Monte Carlo run, the following performance metrics, such as output-voltage ripple, output-voltage stress and efficiency, are computed as follows:

Output-voltage ripple: The output-voltage ripple is typically expressed as a peak-to-peak value

$$\Delta V_0 = V_{0,max} - V_{0,min} \quad (12)$$

measured over one switching period around the nominal output voltage. The output-voltage ripple percentage expresses how large the output-voltage ripple is relative to the nominal (average) output voltage.

$$\%Voltage\ Ripple = \frac{\Delta V_0}{V_{0\ nominal}} \times 100 \quad (13)$$

It is a normalized metric and is widely used for performance comparison.

Output-voltage stress: The peak value of the output voltage waveform over time:

$$V_{0-str} = V_{0,max} \quad (14)$$

A detailed Monte Carlo Simulation procedure for the non-ideal ULL converter was performed in the LTspice Analog Devices simulation platform with manufacturing values. The Monte Carlo simulation studies were performed using a PC with an AMD Ryzen 9 7900X processor at 4.7 GHz and 32 GB of RAM, with a sampling time of 0.1 µs. The detailed modeling scenarios considered for the stochastic performance analysis of a non-ideal ULL converter are given in Tab. 2.

Table 2. Detailed modeling scenarios considered for stochastic performance analysis of a non-ideal ULL converter

Scenarios	**Passive component tolerances**	**MOSFET non-idealities**
MOSFET non-ideal model	Fixed at nominal values	$R_{DS_{ON}}$, Q_G, V_{DS}, I_{DS}
Passive tolerance model	L_1 , L_2 C_1 , C_2 , r_{C1} , r_{C2} R_{L1}, R_{L2} and R_0 varied within tolerance limits	MOSFET non-ideal parameters remain fixed

4.1 MOSFET non-ideal model scenario

This scenario incorporates various MOSFET non-ideal models, including IPI041N12N3, IRFP4668, AOB2500L, AOB66518L, and FDB2532, while passive component tolerances are set to nominal values. This scenario isolates the effect of passive component tolerances on output voltage ripple and efficiency. The non-ideal model parameters of the MOSFET are given in Tab. 3.

Table 3. MOSFET non-ideal model parameters

Model	V_{DS} (V)	I_{DS} (A)	$R_{DS\ ON}$ (mΩ)	Q_G (nC)
IPI041N12N3	120	120	4.1	158
IRFP4668	200	130	8.0	161
AOB2500L	150	152	5.1	97
AOB66518L	150	120	4.2	80
FDB2532	150	79	16	82

In the selection of the optimal MOSFET model, the on-state resistance $R_{DS\ ON}$ is the dominant factor in conduction losses. In contrast, the gate charge Q_G plays a decisive role in switching losses. In this scenario, total simulation time is 60 ms and is labeled as 'Time' in Fig. 3. This figure the effect of different MOSFET non-ideal models on the output voltage ripple and efficiency of ULL converter, where the duty cycle is fixed at d = 0.6.

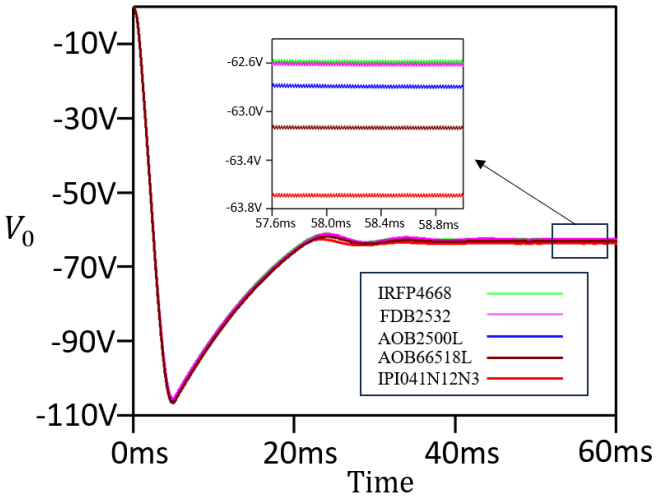

Fig. 3. The effect of different MOSFET non-ideal models on the output voltage ripple and efficiency of ULL converter

As clearly observed in Fig. 3, the output voltage is depicted in a zoomed-in view for effect of different MOSFET non-ideal models on the output voltage ripple and efficiency of ULL converter and the output voltage value closest to the nominal level (– 63V) is obtained using the non-ideal AOB66518L MOSFET model. The percentage voltage ripple and efficiency results from all MOSFET non-ideal models of ULL converter are presented in Tab. 4.

Table 4. The percentage voltage ripple and efficiency results for all MOSFET non-ideal models of ULL converter

Model	Voltage ripple (%)	Efficiency (%)
IPI041N12N3	0.0409	93.39
IRFP4668	0.0447	90.57
AOB2500L	0.0423	93.31
AOB66518L	0.0405	93.94
FDB2532	0.0442	92.90

From Tab. 4, it is observed that the improvement percentages in voltage ripple for the AOB66518L non-ideal MOSFET model are 0.97%, 9.39%, 4.25%, and 8.37%, respectively. Similarly, the corresponding improvement percentages in efficiency are 0.59%, 3.72%, 0.67%, and 1.77%, respectively for the AOB66518L non-ideal MOSFET model.

4.2 Passive tolerance model

In this scenario, L_1, L_2, C_1, C_2, r_{C1}, r_{C2}, R_{L1}, R_{L2}, and R_0 are modeled as random variables within their manufacturing tolerance ranges according to datasheet specifications using a 20-iteration Monte Carlo simulation separately. In contrast, the MOSFET non-ideal model parameters are kept fixed. For this scenario, the AOB66518L non-ideal MOSFET model is adopted to represent the switching device. Furthermore, the non-ideal inductor, capacitor, and resistor component technology, along with their maximum values, is provided in Tab. 5.

Table 5. The non-ideal inductor, capacitor, and resistance components technology, along with their maximum values

Components technology	**Maximum value**
Kemet X7R/ capacitor	200 V
Kemet SC10-100/ inductor	250 V/10 A
Aluminum heat/sink resistor	2 kW

This scenario isolates the effect of MOSFET non-idealities on output voltage ripple and efficiency of ULL converter. This scenario enables the separate analysis of passive element tolerance. To evaluate the impact of passive component manufacturing separately, a three-stage randomization procedure is adopted in this scenario as follows:

4.2.1 First stage

Inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2} are treated as stochastic variables. In contrast, capacitors C_1, C_2 and their equivalent series resistances r_{C1}, r_{C2} and load resistance R_0 are fixed at nominal values. This stage facilitates direct sensitivity ranking of L_1, L_2, R_{L1}, and R_{L2} under a fixed duty cycle of $d = 0.6$ using a 20-iteration Monte Carlo simulation. The total duration of the simulation is 60 ms and is labeled as 'Time' in this stage. Figure 4 illustrates the effect of the inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2}, considering tolerance variations on the output voltage ripple and efficiency of ULL converter during the first stage.

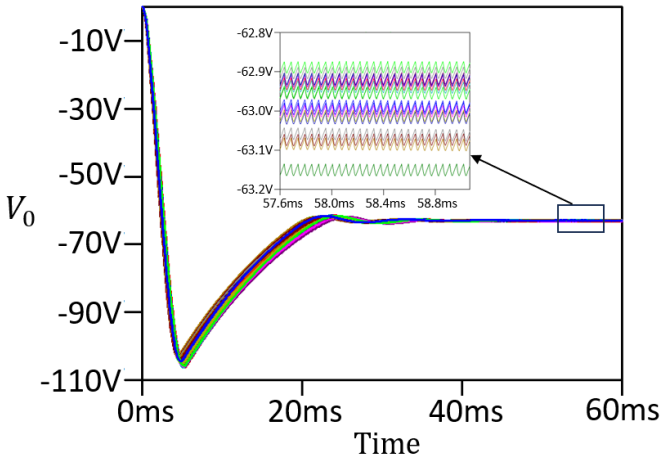

Fig. 4. The tolerance effect of the inductors L_1 and L_2 along with their winding resistances R_{L1} and R_{L2} on the output voltage ripple and efficiency of ULL converter

As shown in Fig. 4, the output voltage is illustrated in a zoomed-in view for tolerance effect of the inductors L_1 and L_2 along with their winding resistances R_{L1} and R_{L2} on the output voltage ripple and efficiency of ULL converter and the output voltage ripple is computed as 0.0003%. The output voltage stress reaches – 108V, while the conversion efficiency is 91.20%.

4.2.2 Second stage

In the second stage, the capacitors C_1 and C_2 and their equivalent series resistances r_{C1} and r_{C2} are randomized, while inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2} and load resistance R_0 are fixed nominal values. In this stage, the simulation runs for a total of 60 ms and is labeled as 'Time' in Fig. 5. With the duty cycle held constant at $d = 0.6$, this stage employs a 20-iteration Monte Carlo simulation to evaluate the sensitivity of the output voltage ripple and efficiency on ULL converter to tolerances in C_1, C_2 and their equivalent series resistances r_{C1} and r_{C2}, as illustrated in Fig. 5.

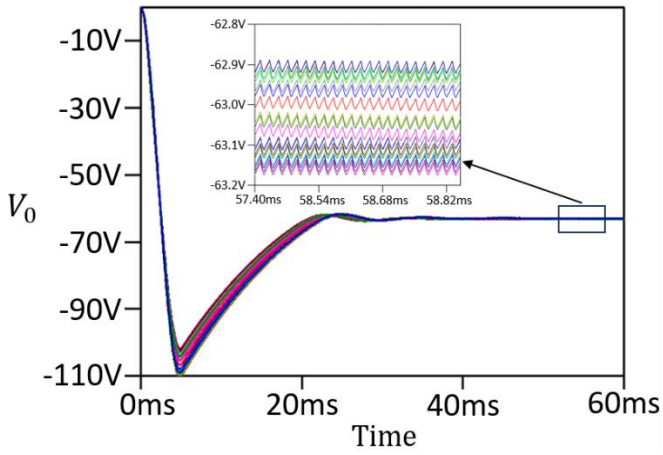

Fig. 5. The effects of tolerances in capacitors C_1 and C_2 and their equivalent series resistances r_{C1} and r_{C2} on the output voltage ripple and efficiency of ULL converter

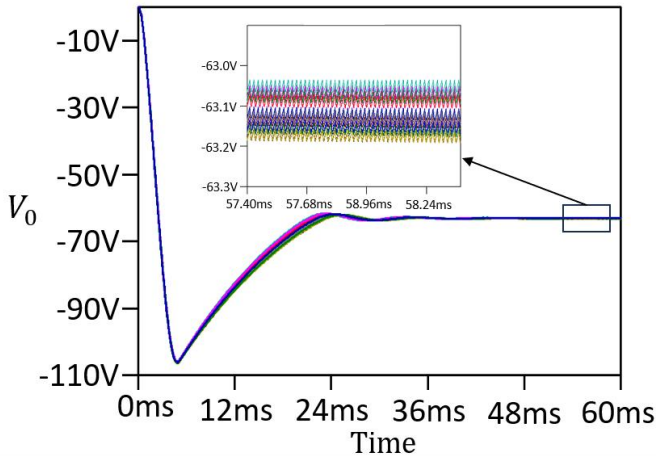

Fig. 6. The effects of tolerances in the load resistance R_0 on the output voltage and efficiency of ULL converter

As clearly shown in Fig. 5, the output voltage is shown in a zoomed-in view for the effects of tolerances in capacitors C_1 and C_2 and their equivalent series resistances r_{C1} and r_{C2} on the output voltage ripple and efficiency of ULL converter. The output voltage ripple, output voltage stress and efficiency are calculated as 0.0016%, – 110 V, and 90.58%, respectively.

4.2.3 Third stage

In the third stage, only the load resistance R_0 is randomized, while the inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2}, as well as the capacitors C_1 and C_2 and their equivalent series resistances r_{C1} and r_{C2}, are fixed at their nominal values. In this stage, total simulation time is 60 ms and is labeled as 'Time' in Fig. 6. This figure illustrates the sensitivity of the output voltage ripple and efficiency on ULL converter to tolerances in the load resistance R_0 obtained from a 20-iteration Monte Carlo simulation with the duty cycle fixed at $d = 0.6$.

Figure 6 indicates that the output voltage is illustrated in a zoomed-in view for the effects of tolerances in the load resistance R_0 on the output voltage and efficiency of ULL converter. The output voltage ripple, output voltage stress reach 0.0076% and – 107 V, respectively, whereas the efficiency is 89.72%.

From the simulation results obtained in Figs. 3-6, the following observations can be made.

- As observed in Fig. 3, MOSFET non-idealities such as the on-state resistance $R_{DS\,ON}$, gate charge Q_G, drain-source voltage V_{DS}, and drain-source current I_{DS} variations are also non-negligible.
- As observed in Figs. 4-5, the tolerance effects of the capacitors C_1, C_2 and their equivalent series resistances r_{C1} and r_{C2} lead to a greater reduction in efficiency compared to the tolerance effects of the inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2}, primarily due to the increased voltage ripple. Thus, the inductors L_1 and $L_2$and their winding resistances R_{L1} and R_{L2} exhibit low sensitivity to tolerance variations.
- As observed in Fig. 6, despite using a smaller tolerance range for the load resistance R_0 than for capacitors C_1 and C_2 and their equivalent series resistances r_{C1} and r_{C2}, as well as inductors L_1 and L_2 and their winding resistances R_{L1} and R_{L2}, a larger voltage ripple and lower efficiency are obtained. This result demonstrates the high sensitivity of the converter performance to variations in the load resistance R_0.
- As observed in Figs. 4-6, the capacitor tolerance variations lead to a higher sensitivity and variance in the output-voltage stress relative to inductor and resistance tolerances.

5 Conclusion

This paper presents a Monte Carlo based stochastic analysis to evaluate the effects of component tolerances and non-idealities on the ULL converter. The results demonstrate that the non-ideal ULL converter maintains stable operation under realistic parametric variations. The Monte Carlo analysis reveals that the output voltage ripple and efficiency remain within acceptable limits, thereby confirming the robustness of the designed topology. The designed topology provides actionable insights for reliable converter design under manufacturing-induced variations. It is also concluded that the selection of the MOSFET model and the

tolerance range of the load resistance R_0 have a critical impact on the output voltage ripple and efficiency. In future studies, it is aimed to integrate intelligent control strategies with deep learning techniques and to conduct experimental validations using other DC-DC converter topologies.

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