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Design of a class E RF power amplifier with shunt capacitance and shunt filter using a modified load network

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Class E switching-mode RF power amplifiers have been extensively utilized in contemporary wireless transmitting systems to provide high efficiency and long battery life. The class-E power amplifier with an output network constituted from a parallel capacitor, series inductor, and shunt resonant circuit provides a replacement for the original class E power amplifier with shunt capacitance by offering the same circuit simplicity and performance predictability in addition to wide frequency band capability. This paper presents a new transmission-line load network topology for the class-E power amplifier with shunt capacitance and shunt filter by introducing an alternative method for evaluating the optimum load resistance for maximized efficiency, and integrating a low-pass Chebyshev transforming network for better harmonic suppression. This circuit is first mathematically analyzed and then simulated by means of the ADS software. A prototype power amplifier model is also fabricated based on the ATF-34143 GaAs pHEMT low cost transistor to operate at 1 GHz. Experimental results show that a dc-to-RF efficiency of 61%, output RF power of 23 dBm, and power gain of 11 dB have been obtained at input power level of 12 dBm.

Keywords: class-E PA, GaAs pHEMT, Chebyshev filter, transmission-line load network

1 Introduction

Microwave power amplifiers are fundamental elements in modern radio transmitters. The desired characteristics of power amplifiers include high efficiency, low distortion, high stability, and broad operating bandwidth. Highly efficient power amplifiers are required to ensure long battery life in portable wireless systems. There are several power amplifier modes that can achieve efficient operation including class-E [1], class-F [2], inverse class-F [3], class-J [4], and extended class-J configurations [5]. At UHF and microwave frequencies, lumped-element matching networks become of limited use due to parasitic effects and power loss and therefore transmission-line networks are preferable.

The class-E power amplifier with shunt capacitance and shunt filter represents a promising technique with simple structure and high efficiency that is comparable with the original switching-mode class-E power amplifier invented by Sokal [1]. A load network using transmission lines was introduced to present inductive load impedance at the fundamental frequency and pure inductive reactance at the second and third harmonic components beyond the shunt capacitance [6]. The analysis of this configuration has been done for any duty cycle of the input signal [7]. Further topologies of the class-E PA with shunt filter are discussed and analyzed in [8]. The class-E power amplifier with shunt capacitor and shunt resonator can be used in an outphasing transmitter for improved system linearity [9].

In this work, a modified transmission line load network is proposed with a technique for evaluating the optimum load resistance that gives the maximum power efficiency. The harmonic suppression capability of the class-E PA with shunt capacitance and shunt filter has also been improved by using a low-pass Chebyshev filter as a transforming network to match the 50 Ω system impedance with the optimum load resistance.

2 Conventional class-E power amplifier with shunt capacitance and shunt filter

The schematic diagram for the class E RF power amplifier with shunt capacitor and shunt resonator is depicted in Fig. 1 [6]. The output matching network of this amplifier involves a shunt capacitor C, series inductor L, parallel resonator L_o and C_o, optimum load resistance R, in addition to DC blocking capacitor and DC feeding RF choke. For ideal analysis of the circuit, it is assumed that the field effect transistor (FET) operates as an electronic switch presenting very low on-resistance (R_{on}) during conduction and a very high resistance when driven into cut-off. The gate bias voltage is usually chosen near threshold with very low quiescent drain current to drive the active device at 50% duty cycle. The parallel tuned circuit constructed from L_o and C_o presents high impedance to the fundamental frequency current component and very low impedance for higher-order harmonics.

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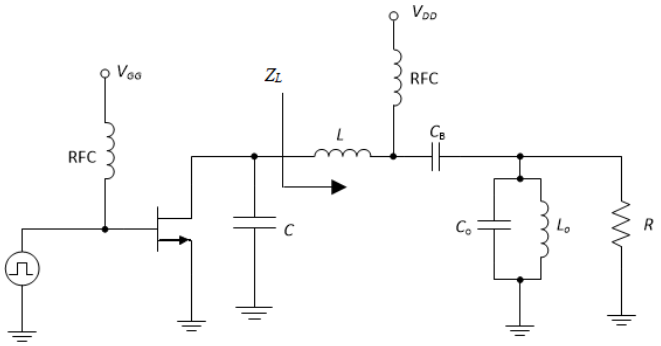


Fig. 1. Simplified structure of the class-E RF power amplifier with shunt capacitor and parallel resonator

When the active device turns on, the supply current passes through the transistor while when the device is non-conducting, then the current passes through the shunt capacitor *C*. This capacitor may be represented by the internal parasitic capacitance of the transistor.

The optimum parameter values of the load network are evaluated by setting the necessary class E idealized conditions with zero drain voltage and zero derivative drain voltage at the instant when the device is turned on. These values are given by [6]:

$$R = 0.4281\frac{{V_{DD}}^2}{P_{out}} \tag{1}$$

$$L = 1.4836\frac{R}{\omega} \tag{2}$$

$$C = \frac{0.261}{\omega R} \tag{3}$$

where P_{out} is the desired output RF power, ω is the frequency of operation, and V_{DD} is the drain supply voltage.

The ideal drain voltage and current waveforms are sketched in Fig. 2.

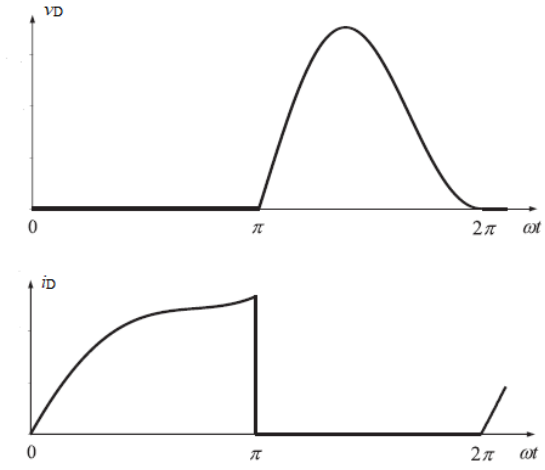


Fig. 2. Ideal shapes of the drain voltage and current signals [10]

3 Proposed transmission line load network

At microwave frequencies, microstrip lines are preferred over lumped elements in the realization of the matching circuits of power amplifiers due to ease of implementation, design predictability, lower power losses, and lower parasitic elements. Ideal transmission lines can give acceptable prediction of the response for the power amplifier circuit before converting them to practical microstrip lines. The analysis of the class E power amplifier can be performed in the frequency domain by identifying the desired loading impedance at the first three harmonics as a good approximation.

From Fig. 1, the parallel resonant circuit, constituted from L_o and C_o, presents open circuit condition at the fundamental frequency f_0, and short circuit at the second and third harmonics. Therefore, the load impedance Z_L seen beyond the shunt capacitor *C* at the first three harmonics is described by:

$$Z_L(\omega_0) = R + j\omega_0 L \tag{4}$$

$$Z_L(2\omega_0) = j2\omega_0 L \tag{5}$$

$$Z_L(3\omega_0) = j3\omega_0 L \tag{6}$$

Substituting for $\omega_0 L = 1.4836\ R$ from Eqn. (2), the above three equations are re-written in the form:

$$Z_L(\omega_0) = R + j\ 1.4836\ R \tag{7}$$

$$Z_L(2\omega_0) = j\ 2.9672\ R \tag{8}$$

$$Z_L(3\omega_0) = j\ 4.45\ R \tag{9}$$

So, the optimum load resistance *R* becomes a critical design parameter in the evaluation of the harmonic load impedances of the class E power amplifier with shunt capacitance and shunt filter.

The proposed transmission-line loading network for the class-E power amplifier with shunt capacitance and shunt filter is illustrated in Fig. 3.

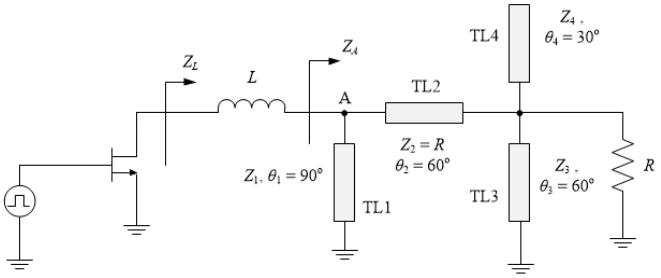


Fig. 3. The proposed transmission-line load network

In this network, the shunt capacitor is embedded with the internal drain-to-source output capacitance of the GaAs pHEMT. At the fundamental frequency compo-

nent, the λ/4 short-circuited shunt stub TL1 behaves as an open circuit to the RF signal. The admittances of TL3 and TL4 are of equal magnitude with opposite signs at the fundamental frequency and omit each other, leaving the resistance R to terminate the transmission line TL2. Since the characteristic impedance of TL2 is set $Z_2 = R$, then the impedance at node A is purely resistive and is set to $Z_A = R + j0$. Therefore, the load impedance is $Z_L = R + j\,\omega_0 L$ at the fundamental frequency, which is identical with Eqn. (4). In the second harmonic component the parallel stub TL1 presents a short circuit, thereby resulting in $Z_A = 0$ and $Z_L = j\,2\omega_0 L$ which is equivalent to Eqn. (5). At the third harmonic frequency, TL1 acts again as an open circuit while the open stub TL4 and shorted stub TL3 present short circuit path for the signal. In this case, the λ/6 transmission line TL2 will be terminated with a short circuit and therefore presents zero impedance at node A. Hence, $Z_A = 0$ and $Z_L = j\,3\omega_0 L$ at the third harmonic frequency in consis-tence with Eqn. (6).

An impedance transforming network is needed to match the 50 Ω load impedance with the desired optimum resistance R. This network can be designed using a low-pass filter structure to reduce the harmonics in the output signal. A block diagram for the proposed class E power amplifier is depicted in Fig. 4. The filter can be synthesized as a broadband Chebyshev matching network of low pass topology [11].

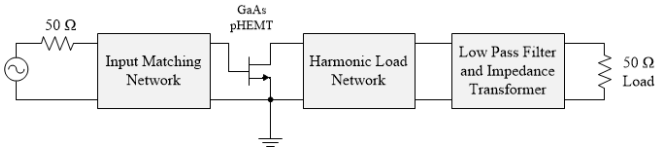


Fig. 4. Block diagram for the proposed class-E power amplifier

4 Design and implementation of a 1 GHz class-E power amplifier

For the sake of verifying the proposed design technique, a medium power amplifier circuit has been designed, simulated, and fabricated to operate at 1 GHz. The low cost GaAs pseudomorphic high electron mobility transistor (pHEMT) ATF-34134 has been selected in this design. The desired output RF power is 23 dBm (0.2 W) and the operating frequency band is from 950 MHz to 1050 MHz. The drain supply voltage V_{DD} is set to 3V and the active device is operated with a quiescent drain current of 20 mA.

4.1 Simulation of the harmonic load impedances

The power amplifier's load resistance R can be estimated from Eqn. (1) and is approximately equal to 20 Ω for $P_{out} = 0.2$ W and $V_{DD} = 3$ V. Consequently, the series inductance L is calculated from Eqn. (2) to be 4.7 nH. The harmonic load impedances at the first three harmonics are simulated on a Smith chart in Fig. 5. It can be seen that the three harmonic impedances are inductive due to the existence of the series inductance L. The fundamental harmonic impedance has a real part equal to R, while the second and third harmonic impedances have zero real part and are reactive.

The series inductance L can be substituted by short segment of a transmission-line having an electric length of [10]:

$$\theta \simeq \tan^{-1}\left(\frac{\omega_0 L}{Z_o}\right) \tag{10}$$

where Z_o is the line impedance.

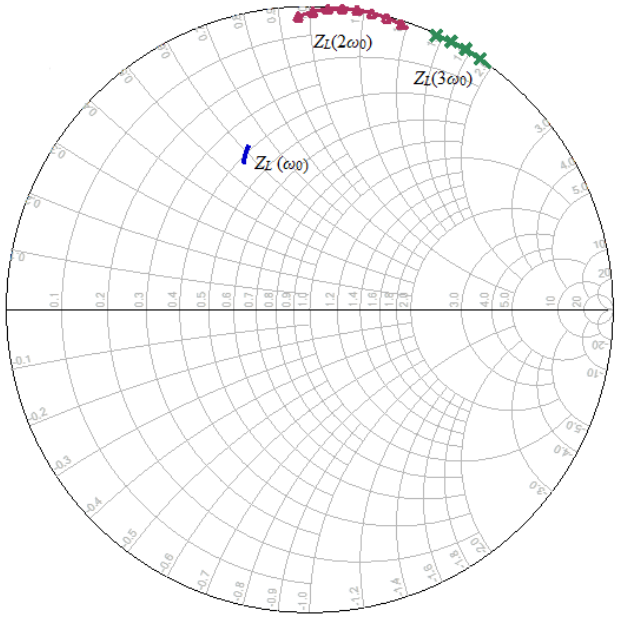


Fig. 5. Harmonic load impedances for a fundamental frequency range from 950 MHz to 1050 MHz

4.2 Evaluation of the optimum load resistance

Although the optimum load resistance, which is a critical design parameter, can be roughly estimated from Eqn. (1) but this value cannot ensure maximum conversion efficiency practically due to the parasitic elements of the active device and the change of its output capacitance with voltage level in addition to the existence of the drain to source on-resistance R_{on}. A new method is proposed to find the optimum value of R that can give peak drain efficiency. This technique is performed by terminating the pHEMT device with the proposed load network and biasing it with the nominated current and supply voltage at the desired input RF power and frequency and sweeping the parameter R for a specified range of values while evaluating the drain efficiency, output RF power and power gain. The proposed procedure is implemented using the harmonic-

balance simulation capabilities of ADS with five harmonics together with the nonlinear transistor model of ATF-34143. This device has an approximate ohmic resistance R_{on} of 6 Ω, which is extracted from its output characteristics. Figure 6 presents the schematic diagram of the test circuit. It can be seen that the series inductance is substituted by a transmission-line of electrical length θ_0, where:

$$\theta_0 = \tan^{-1}\left(\frac{1.4836R}{Z_0}\right) \quad (11)$$

Z_0 is chosen to be equal to 30 Ω.

The circuit has been excited with an input signal level of +12 dBm at 1 GHz.

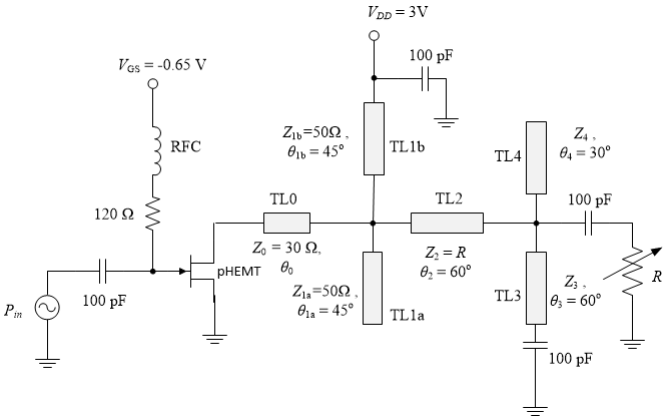


Fig. 6. Schematic of the testing circuit for finding the optimum load impedance

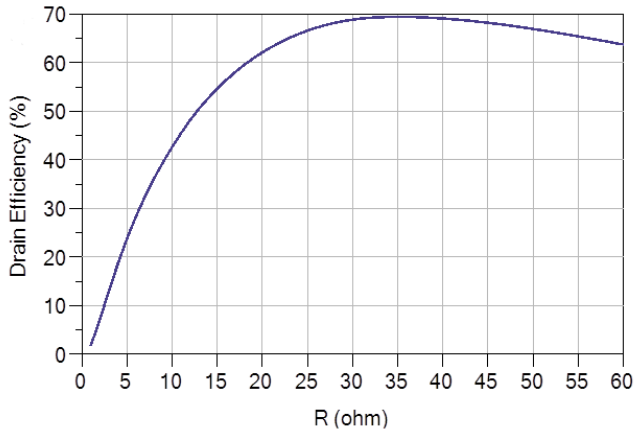


Fig. 7. Drain efficiency versus load resistance

The parallel λ/4 short-circuited stub is replaced by two equivalent open and shorted λ/8 stubs for symmetry and to reduce line lengths [12]. Bypass capacitors are used to provide RF ground for the shorted stubs while blocking the DC current. The variation of the drain efficiency with values of R ranging from 0 to 60 Ω is depicted in Fig. 7. It can be shown that a peak efficiency of about 70% is obtained when R = 35 Ω. Likewise, the output RF power and power gain are sketched in Fig. 8. The power gain is compressed to 13 dB when R exceeds 30 Ω. An optimum value of 30 Ω has been selected in this design.

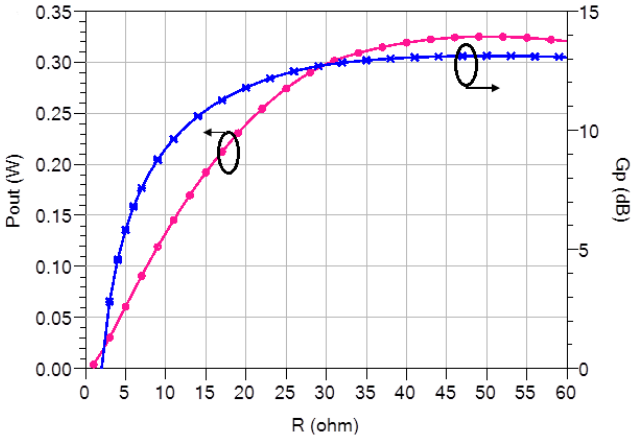


Fig. 8. Variation of output RF power and power gain against load resistance

4.3 Design of the impedance transforming filter

The low pass filter can be synthesized as a ladder network using series inductors and parallel capacitors with different terminations at its input and output ports. In addition to the filtering property, the network is utilized to transfer the 50 Ω system impedance into the 30 Ω desired resistance. The transformation ratio is r = 50/30 = 1.6 ≈ 1.5. For a filter order n = 4 and a fractional bandwidth w = 0.1, the normalized prototype elements of the filter are g_1 = 0.65, g_2 = 0.88, $g_3 = r.\ g_2$ = 1.32, $g_4 = g_1/r$ = 0.44 and g_5 =1.50. The actual elements are calculated from [11]:

$$L_1 = g_1.\frac{1}{\omega_0}.\frac{Z_o}{g_5} \quad (12)$$

$$C_2 = g_2.\frac{1}{\omega_0}.\frac{g_5}{Z_o} \quad (13)$$

$$L_3 = g_3.\frac{1}{\omega_0}.\frac{g_5}{Z_o} \quad (14)$$

$$C_4 = g_4.\frac{1}{\omega_0}.\frac{g_5}{Z_o} \quad (15)$$

Substituting for f_0 = 1 GHz and Z_o = 50 Ω gives L_1 = 3.47 nH, C_2 = 4.2 pF, L_3 = 7 nH, C_4 = 2.084 nH.

The filter schematic diagram is shown in Fig. 9 and its insertion and return losses are presented in Fig. 10.

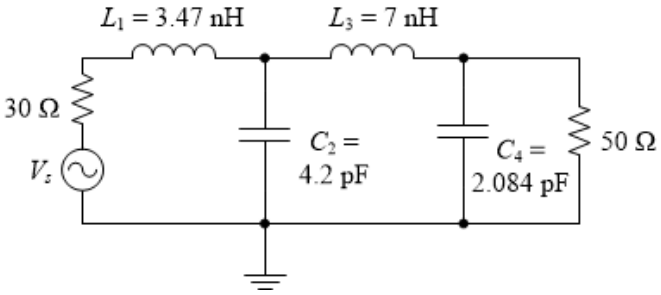


Fig. 9. Lumped element impedance transforming low pass network

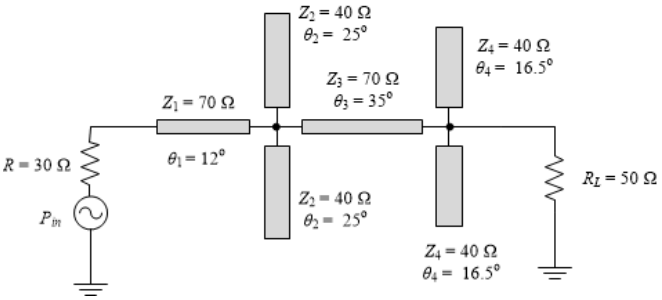


Fig. 11. Transmission line impedance transforming low pass network

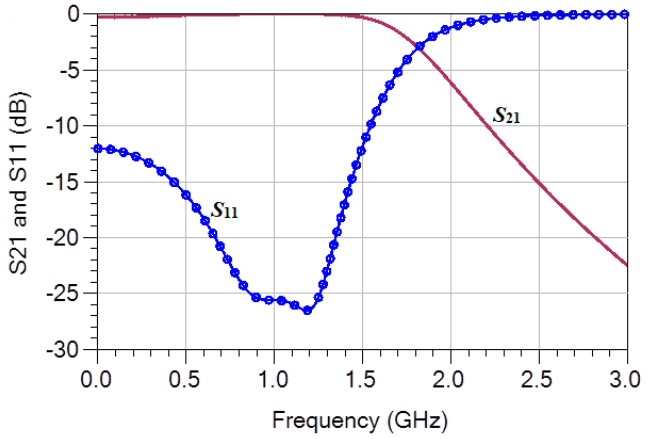


Fig. 10. Insertion and return losses of the lumped-element low-pass filter

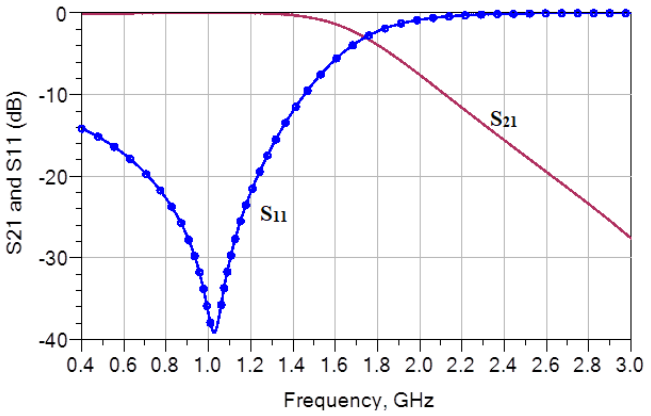


Fig. 12. Insertion and return losses of the transmission line impedance transformer

The lumped elements can be converted to transmission line sections. The inductors are approximated by series transmission lines with high characteristic impedance and the capacitors are represented by open-circuited stubs with low characteristic impedance. The parameters of the series line can be estimated from [13]:

$$\omega_0 L = Z_o.\tan(\theta) \tag{16}$$

If two identical parallel open stubs are used, then their parameters can be found from [13]:

$$\omega_0 C = \frac{\tan(\theta)}{2Z_o} \tag{17}$$

Based on the above relations and using ADS optimization capabilities, the schematic diagram of the impedance transforming low pass network is presented in Fig. 11, while its response is displayed in Fig. 12.

4.4 Power amplifier circuit simulation and testing

According to the proposed power amplifier structure presented in Fig. 4, the low pass Chebyshev transforming network is cascaded with the load network of Fig. 6. In order to prevent low frequency oscillations and ensure stable operation, a stabilizing network constituted from a series transmission line section and a 22 Ω resistor is inserted at the gate circuit of the pHEMT. Afterwards, the input impedance of the active device has been evaluated by means of source-pull ADS simulation at a frequency of 1 GHz. An input matching network has then been designed using a series transmission line and a parallel short-circuited stub to minimize the input VSWR and increase the power gain. The ideal transmission line sections are then converted to microstrip-lines using the RO4350B dielectric substrate of Rogers. A schematic diagram for the designed class E power amplifier circuit is shown in Fig. 13.

The circuit is first simulated using the large-signal *S*-parameter test to examine the stability factor. Figure 14 displays the stability factor *K* against input signal level for a power sweep from 0 to 16 dBm at 1 GHz. It is clear that the circuit is inherently stable and the stability factor *K* is greater than 1.

The drain voltage and current waveforms are sketched in Fig. 15 for a drive power of +12 dBm. It is shown that there is some overlapping between the two waveforms due to the nonlinearity and parasitic elements of the active device model. However, the waveforms present an acceptable approximation to the ideal current and voltage signals of the class E power amplifier depicted in Fig. 2. The simulated peak drain voltage V_{DP} is 9 V and the peak drain current I_{DP} is 300 mA.

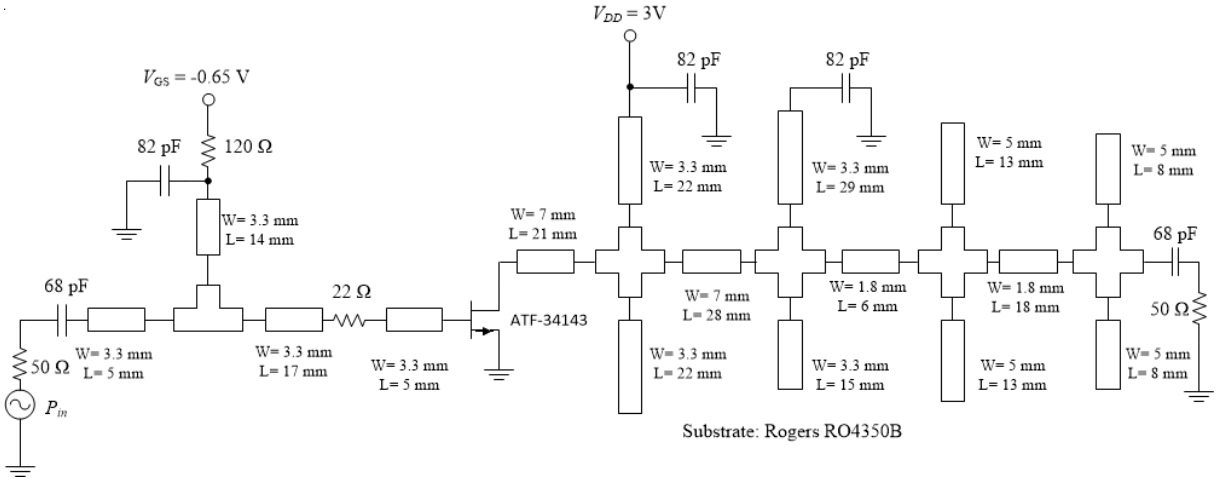


Fig. 13. Circuit diagram of the completed power amplifier

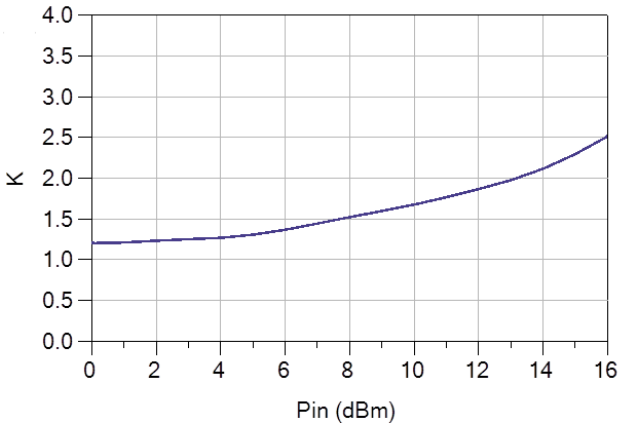


Fig. 14. Stability factor versus input drive level

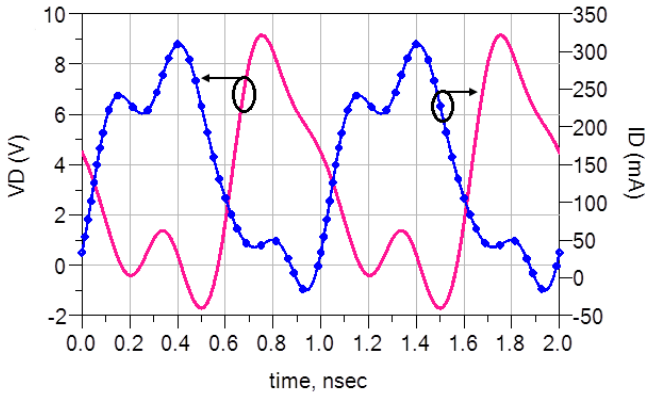


Fig. 15. Simulated drain current and voltage signals

In Fig. 16, the simulated input reflection coefficient is presented against input power level at 1 GHz, showing a good matching at the amplifier's input network.

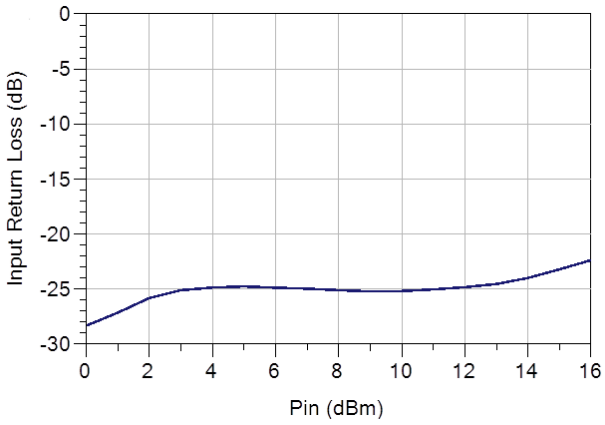
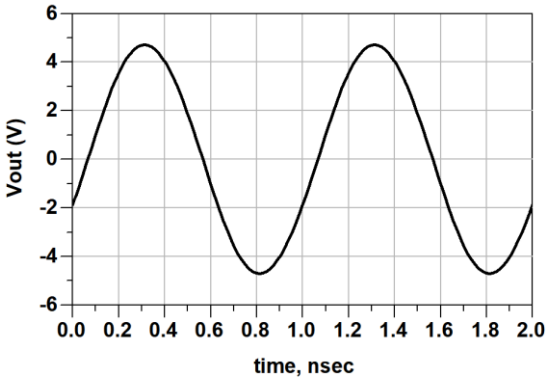


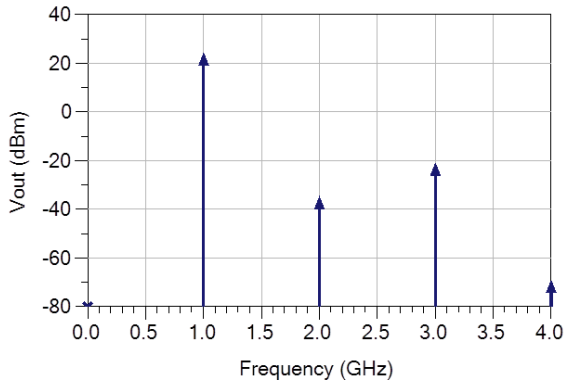
Fig. 16. Simulated input reflection coefficient versus input power

The simulated output signal and its spectrum are displayed in Fig. 17, indicating a second harmonic level of 59 dBc and a third order harmonic component of greater than 45 dBc below the fundamental signal power due to the filtering effect of the Chebyshev low pass transformer integrated with the power amplifier circuit.

The amplifier circuit has been constructed on an RO4350B ceramic substrate of Rogers with dielectric constant of 3.66, board thickness of 1.524 mm, and a dielectric loss-tangent of 0.0031. Figure 18 depicts the assembled power amplifier circuit. The circuit was tested in the laboratory using an RF signal generator, driver power amplifier module, attenuator, and a spectrum analyzer.



(a)



(b)

Fig. 17. Output signal in time domain (a), and its spectrum (b)

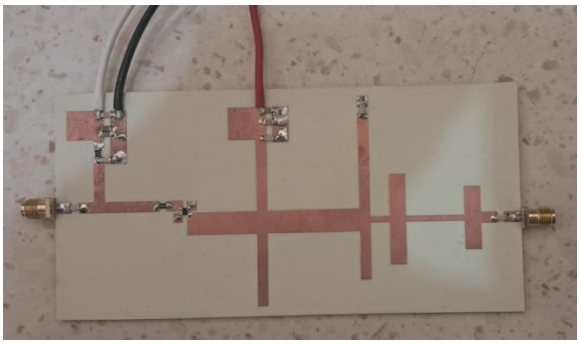


Fig. 18. A photograph for the implemented class E power amplifier

Figure 19 presents the simulated and measured drain efficiency of the power amplifier circuit against input power. At a typical input power of 12 dBm, the simulated efficiency is about 65% while the measured value is about 61%. The saturated drain efficiency reaches to about 68% with an input drive power of 16 dBm.

In Fig. 20, the output RF power is displayed with a sweep of input power level from 0 to 16 dBm at a center frequency of 1 GHz. The simulated output RF power is +25 dBm, while the measured value is about 23 dBm are obtained at input level of 12 dBm. The deviation of the measured characteristics from the simulated response may be referred to the losses in matching elements and the parasitic components of the packaged transistor. Figure 21 presents both the simulated and measured power-gain of the circuit versus input power. A practical power-gain of about 11 dB is obtained at an input power level of 12 dBm. Beyond input power of +10 dBm, the power gain drops significantly due to the transistor nonlinear operation under large signal input levels.

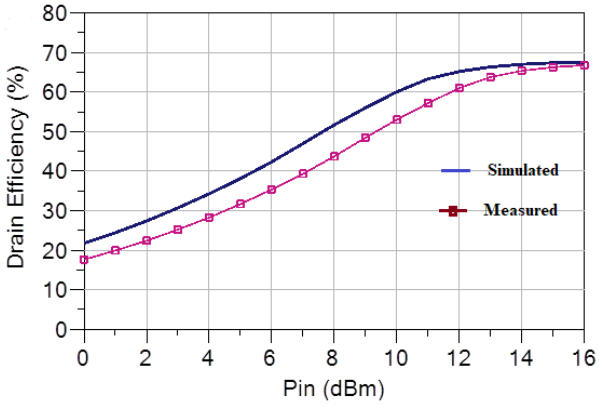


Fig. 19. Drain efficiency versus input power

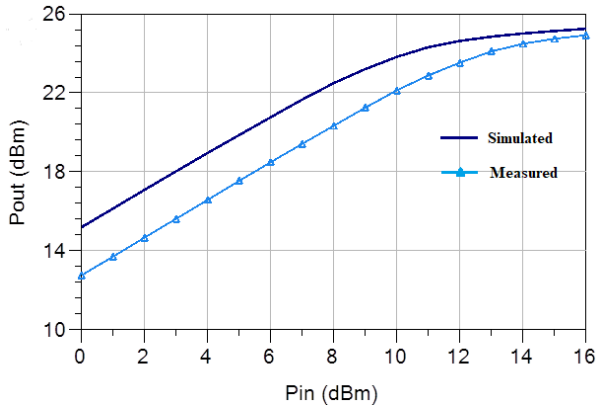


Fig. 20. Output RF power versus input level

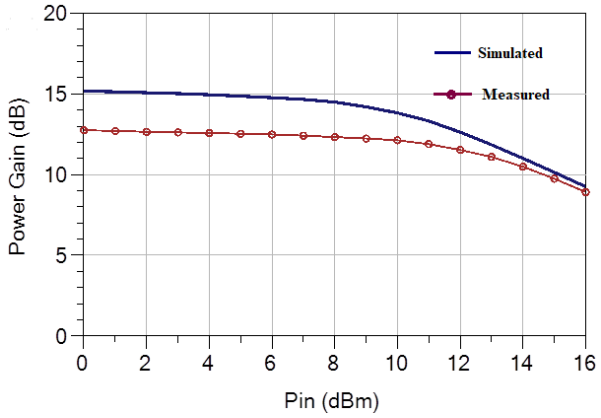


Fig. 21. Power gain versus input power

The output power capability C_P of the amplifier can be calculated from [14]:

$$C_P = \frac{P_{out}}{V_{DP}.I_{DP}} \tag{18}$$

where V_{DP} is the peak drain voltage and I_{DP} is the peak drain current. From the results of simulation depicted in Fig. 15 and Fig. 20, it can be proved that $C_P = 0.117$.

The amplifier circuit has also been tested over a frequency range from 950 MHz to 1050 MHz to monitor the changes in power-gain and efficiency with frequency for a typical input power level of 12 dBm. Figure 22 displays both the simulated and measured power gain over the desired frequency band. The reduction in practical power gain when compared with the simulated gain is referred to the parasitic elements, tolerances in components, imperfect manufacturing, and fringing fields. In Fig. 23, the simulated and measured drain efficiency of the circuit are presented, showing acceptable agreement.

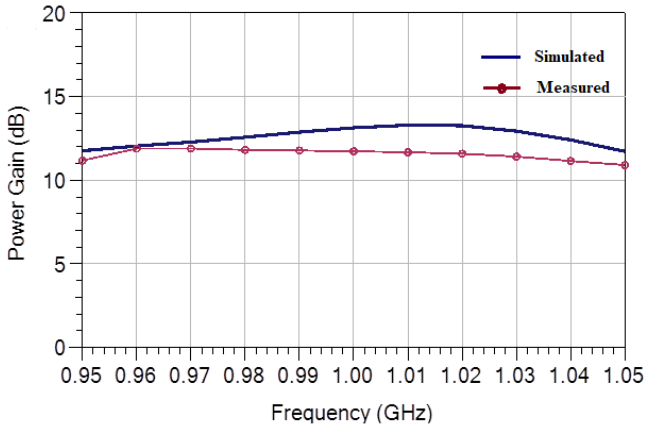


Fig. 22. Power gain versus frequency

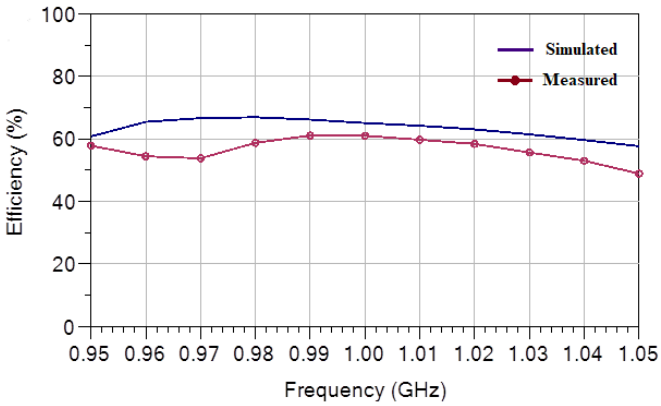


Fig. 23. Drain efficiency versus frequency

Table 1 summarizes a comparison of the performance parameters for the designed class E power amplifier with those of other published works using the same ATF-34143 GaAs pHEMT device. Higher efficiency can be obtained by driving the amplifier with greater input power level at the expense of reducing the power gain due to transistor saturation.

The proposed power amplifier shows competitive performance characteristics in terms of power gain and power-output capability.

Table 1. Comparison of the power amplifier's metrics with other published articles.

Ref.	f (GHz)	P_{in} (dBm)	G_p (dB)	P_{out} (dBm)	Efficiency (%)	C_P	Class
[15]	0.74	12	10.7	22.7	66.5 (PAE)	0.147	Class E
[16]	2.4	10	10	20	74 (PAE)	0.145	Class F
[17]	1.8	11.6	10.8	22.4	76.6 (PAE)	0.143	Class F
[18]	1.8	19	8.2	27.2	75 (PAE)	0.085	Class F
[19]	2.4	16	9	25	72 (PAE)	0.075	Class E
This work	1	12	11	23	61 (Drain)	0.117	Class E

5 Conclusion

A new transmission-line load network topology for the class-E RF power amplifier with parallel capacitor and parallel resonant circuit is developed in this work. A Chebyshev impedance transforming network is also integrated with the load circuit to enable the reduction in the harmonic distortion of the output signal and present the desired optimum load resistance concurrently. To overcome the problem of the device's parasitic components and their effects on the calculation of the load network parameters, a new method has been developed for finding the optimum load resistance that can produce maximum efficiency based on the transistor nonlinear model and the ADS harmonic-balance large signal simulation at the nominal operating frequency and input power level. This method is based on sweeping the load resistance R over a specified range while evaluating the circuit efficiency and output RF power at each value. The optimum load resistance value is selected to fulfill maximum drain efficiency and high output power. In order to verify the suggested design technique, a medium power amplifier circuit has been designed, simulated, and constructed practically. The experimental results confirm that an output RF power of 23 dBm, drain efficiency of 61%, and power-gain of 11 dB have been obtained at an operating frequency of 1 GHz and input drive power of 12 dBm.

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