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Mitigating destabilizing effects of CPLs through fractional order DC/DC buck converter for enhanced energy conversion efficiency

Youcef Djourni[1], Khatir Khettab[1], Yassine Bensafia[2], Abderrahmane Moussaoui[3]

In DC microgrids (MG), the fractional order (FO) model of DC/DC converter is more accurate than an integer order (IO) version because the capacitor and inductor orders have a great effect on the converter performance. On this basis, a FO DC/DC buck converter is constructed to deal with the instability issues associated with a constant power load (CPL), which has the possibility of destabilizing DC microgrids. In this context, Oustaloup recursive approximation method (ORA) is employed to establish the FO converter's components, and the dynamic equations of the FO buck converter are developed by means of the average method. As the CPLs have nonlinear characteristics, a FO nonlinear backstepping controller (BSC) is presented to effectively avoid the instability problem of the DC bus voltage. Furthermore, the asymptotic stability is proved using the fractional Lyapunov function. Finally, numerical results demonstrate the superiority of the fractional order controller over the integer order version of the backstepping control when the system faces all possible perturbations or disturbances.

Keywords: microgrid, fractional order buck converter, constant power load, fractional order backstepping controller, Oustaloup recursive approximation

1 Introduction

Although fractional calculus (FC) has a long history, it has recently been recognized as the calculus of the century. Currently, there is increasing interest in exploring new concepts and potential advantages of FC, especially in its engineering applications, such as control systems [1-3]. Fractional calculus is renowned for its capability to model non-smooth physical phenomena and complex systems with greater accuracy. Due to these unique characteristics, many physical phenomena are best modelled and described using fractional calculus [4, 5].

Several studies indicate that a FO model provides an accurate analysis of the actual dynamic behaviour of electronic components, as compared to an integer order model. In [6], the authors used the FO capacitor and inductor to build a new fractional double inductor LC filter, providing rich features of the constructed filter. Therefore, fractional models can be considered as a significant contribution in the field of electrical engineering for constructing power converters [7].

DC MGs, used in multi-source power generation like offshore wind [8], consist of interconnected generators, loads, and storage units [9]. They surpass AC MGs in efficiency, reliability, and stability, avoiding reactive current and phase imbalance issues. With fewer conversion steps and simpler control, DC MGs ensure stable voltage. Storage devices play a key role in maintaining bus stability during energy fluctuations, balancing power output [10].

Ensuring DC bus stability in a DC MG supplying CPLs is challenging due to instability caused by their incremental negative impedance (INI) [11]. This reduces system damping, leading to oscillations and potential equipment failure, limiting linear control methods [12, 13]. Additionally, voltage perturbations further degrade stability [14, 15]. Researchers are thus exploring advanced control strategies to mitigate CPL instability. Based on Golver Doyle Optimization Algorithm and small-signal method, H_∞ controller [16] is proposed to control a buck converter connected to CPL. DC bus perturbations caused by load-side converter and parameters variations are successfully rejected, reaching the desired system stability in the DC MG.

As seen, the most widely used controllers for dealing with common instability problems in DC microgrids are controllers of integer orders [15, 17]. However, it is noticing that the FO controllers have also received much attention. The FO controller is known for its extra design parameters, the latter provide a higher degree of freedom [18-21]. In [18], use of FO terminal sliding mode controller minimizes the instability effect in MG, which in turn weakens the chatter phenomenon brought on by constant power loading.

[12]Department of Electrical Engineering, Laboratoire de Génie Electrique, Mohamed Boudiaf University of M'sila, 28000, Algeria
[2]Department of Electrical Engineering, University of Bouira, 10000, Algeria
[3]Department of Electrical Engineering, LAAS Laboratory, National Polytechnic School of Oran- Maurice Audin, Oran, Algeria.
khatir.khettab@univ-msila.dz, youcefdjourni@gmail.com

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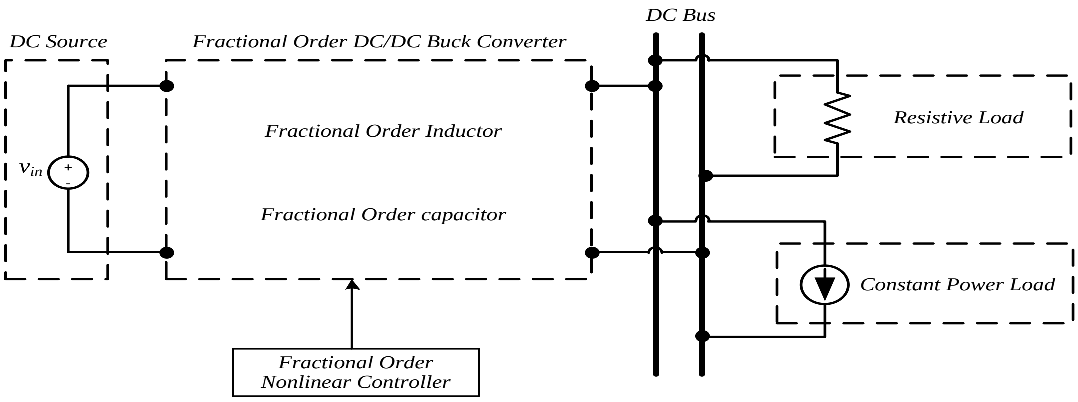


Fig. 1. FO DC/DC buck converter based CPL and damping resistor

To effectively control the output voltage of the FO power converter, it is important to take into account the fractional behaviour of the converter's components by using an adequate approximation method [20]. Therefore, a FO nonlinear controller is more appropriate for ensuring the DC bus stabilization in order to achieve optimal performance in DC MGs. As far as we are aware, this problem is not addressed in the literature in terms of applying an incommensurate FO nonlinear controller for a FO DC/DC converter, which is regulated to feed CPL.

In this context, an incommensurate FO backstepping-based controller has been built for guaranteeing the DC bus stability even in the presence of a CPL. The proposed controller has been designed to tightly control the output voltage of a fractional order DC/DC buck converters via the fractional Lyapunov function. ORA method has been used to establish the fractional converter's components. Then, based on the average method [22], the dynamic equations of the FO constructed converter feeding a CPL and a resistive load have been derived.

The rest of this article is arranged into several sections. The second section introduces the modelling of the proposed system that mainly consists of fractional capacitor and fractional inductor, and explains the Grünwald-Letnikov (G-L) fractional definition [23]. Section 3 presents the design procedure of the non-linear FO backstepping controller. The stabilization issue is also studied, in this section, using the Lyapunov fractional function. In the following section, The FO buck converter circuit is created using ORA, and the numerical simulation is about validating the system effectiveness. Finally, the article concludes with a summary of the main findings.

2 Modeling of FO buck converter feeding CPL

In the branch of FC, the G-L fractional definition is employed. It is regarded as one of the commonly used definitions that is applied to engineering fields [24, 25]. Therefore, all calculations are carried out based on G-L fractional derivative.

Definition 1

The α^{th}-order G-L fractional derivative of function $x(t)$ is depicted by

$$ {}_{t_0}^{GL}D_t^{\alpha} x(t) = \lim_{h \to 0} h^{-\alpha} \sum_{j=0}^{k} (-1)^j \binom{\alpha}{j} x(kh - jh) \quad \text{for}(\alpha \in R), \tag{1} $$

where ${}_{t_0}^{GL}D_t^{\alpha}$ is the G-L derivative operator, and D^{α} is its abbreviation at $t_0 = 0$. The binomial coefficient $\binom{\alpha}{j}$ in terms of Gamma function $\Gamma(.)$ is given by

$$ \binom{\alpha}{j} = \frac{\Gamma(\alpha+1)}{\Gamma(j+1)\,\Gamma(\alpha-j+1)}. $$

As mentioned previously, the characteristics of an inductor and a capacitor are essentially non-integer in nature. Hence, the fractional order components have been applied to power converters in order to increase the design's flexibility, and it has been found that this has further stabilized the system's overall closed-loop response. Therefore, the designed power converter should be modelled by FC to ensure high performance [26].

For a fractional order capacitor, with the proposed model [27, 28], the current-voltage relationship (i_C, v_c) in a real capacitor can be expressed by

$$ i_C(t) = C\frac{d^{q_1} v_c}{dt^{q_1}} \tag{2} $$

in which q_1 represents the FO of a capacitor and C is the capacitor's capacitance.

In addition, for a fractional order inductor, the voltage-current relationship (v_L, i_L) in a real inductor can be expressed as

$$v_L(t) = L\frac{d^{q_2} i_L}{dt^{q_2}} \tag{3}$$

where q_2 represents the FO of the inductor and L is the inductor's inductance.

As illustrated in Fig. 1, the proposed FO buck converter is mainly constituted of FO capacitor C^{q_1}, FO inductor L^{q_2}, DC power source and a resistive load R. It is worth noting the switch S and diode D are considered as ideal devices. In this study, the FO buck converter functions in continuous current mode feeding a CPL. The CPL is represented by a controlled current source. Hence, we can modify the output power P_{CPL} absorbed by the CPL. Moreover, for a linear relationship between $v_C$andi_P, P_{CPL} will be constant and it can be given by the relation

$$P_{CPL} = v_C . i_P \quad \text{and} \quad -i_P = C\frac{dv_C}{dt} \tag{4}$$

According to the linear models proposed by Westerlund as well as the fact that the converter is assumed to be operating in continuous conduction mode [29], the dynamic equations of the FO buck converter feeding a CPL and a resistive load is expressed bellow

$$\begin{cases} \dfrac{d^{q_1} v_C}{dt^{q_1}} = \dfrac{i_L}{C} - \dfrac{i_R}{C} - \dfrac{i_P}{C} \\ \dfrac{d^{q_2} i_L}{dt^{q_2}} = \dfrac{v_{in}}{L} d - \dfrac{v_C}{L} \end{cases} \tag{5}$$

in which q_1 and q_2 represent the FO of capacitor and inductor, respectively. i_L and v_C are the moving averages of the inductor current and of the capacitor voltage. v_{in} is the voltage of a DC source. i_P represents the current of CPL and i_R is the resistive load. d is the operational duty ration of the PWM signal, which is our desired objective.

In this paper, let us consider that the FOs $q_1, q_2 \in (0,1)$ are different, which means degrading the system (5) under non-commensurate FO nonlinear system[30].

The negative incremental impedance caused by CPL, as is well known, can affect the stability of DC MG or even cause it to malfunction [15, 31, 32]. Indeed, the worst case in terms of reducing system damping occurs when the DC load is pure CPL. Nonetheless, many developed nonlinear controllers, whether integer or fractional, guarantee system stability, preventing the entire DC MG and its elements from unexpected collapse or damage [11, 14].

3 Controller design for FO buck converter with CPL

The fractional order nonlinear control is more suitable for the fractional order nonlinear system such as FO BSC and FO sliding mode controller. For overcoming the instability issues caused by CPL, a FO nonlinear controller is designed according the idea of backstepping. As the resistive load causes power loss, the FO backstepping controller ensures a large signal stability of the FO buck converter under large CPL variations even without using passive load.

Lemma 1 [20]

If $x = 0$ is an equilibrium point of the fractional order system defined as below

$$D_t^{\beta} x(t) = f\big(t, x(t)\big), \tag{6}$$

where$f(t)$ is Lipschitz continuous. Let us consider a Lyapunov function $\mathcal{V}(t, x(t))$ and class-K functions $\delta_i(\ i = 1, 2, 3)$ which satisfy

$$\delta_1(\|x(t)\|) \le \mathcal{V}\big(t, x(t)\big) \le \delta_2(\|x(t)\|) \tag{7}$$

$$_{t_0}^{GL}D_t^{\alpha}\mathcal{V}\big(t, x(t)\big) \le -\delta_3(\|x(t)\|) \tag{8}$$

in which $\alpha \in (0,1)$. Then the FO system (6) is stable, asymptotically.

Theorem

For the state equations of FO buck converter, in (5), the operational duty $d \in (0,1)$ that leads to stabilizing asymptotically the states of the system (5), is expressed below

$$d = \frac{1}{v_{in}}\Big[e_1 + \tilde{v}_C + LD^{q_2}\beta - \frac{L}{C}e_2 \text{sign}(D^{q_1-\alpha}e_1)\text{sign}(D^{q_2-\alpha}e_2) - LK_2 D^{q_2-\alpha}e_2\Big] \tag{9}$$

in which the tracking error dynamics e_1 and e_2 are chosen as

$$e_1 = v_C - \tilde{v}_C, \tag{10}$$

$$e_2 = i_L - \beta. \tag{11}$$

In addition, the virtual controller is as

$$\rho = -CK_1 D^{q_1-\alpha}e_1 + CD^{q_1}\tilde{v}_C + i_R + i_P \tag{12}$$

where $\tilde{v}_C$ is the desired output voltage. From the incommensurate FO system (5), $\alpha = \min\,[q_1, q_2]$ is the smallest fractional order.

Proof

To understand the designed controller, one has the following recursive steps as stated below.

Step 1

We start with the first subsystem of system (5),

$$\frac{d^{q1}v_C}{dt^{q1}} = \frac{i_L}{C} - \frac{i_R}{C} - \frac{i_P}{C} \tag{13}$$

Taking the q_1 order derivative of the tracking error e_1

$$D^{q_1}e_1 = D^{q_1}(v_C - \tilde{v}_C) \tag{14}$$

Using the linear property of the fractional derivative [23], Eqn. (14) becomes

$$D^{q_1}e_1 = D^{q_1}v_C - D^{q_1}\tilde{v}_C \tag{15}$$

Now, define the Lyapunov function as

$$V_1 = |D^{q_1-\alpha}e_1| \tag{16}$$

By applying the additive law property of exponent and taking the α order derivative of Lyapunov function (16), we get

$$\begin{aligned} D^{\alpha}V_1 &= D^{\alpha}|D^{q_1-\alpha}e_1| \\ &\le D^{q_1}e_1\text{sign}(D^{q_1-\alpha}e_1). \end{aligned} \tag{17}$$

Using Eqn. (13) and Eqn. (15) into Eqn. (17) we obtain

$$\begin{aligned} &D^{\alpha}V_1 \le (D^{q_1}v_C - D^{q_1}\tilde{v}_C)\ \text{sign}(D^{q_1-\alpha}e_1) \\ &\le \left(\frac{1}{C}(i_L - i_R - i_P) - D^{q_1}\tilde{v}_C\right)\text{sign}(D^{q_1-\alpha}e_1) \end{aligned} \tag{18}$$

Let choose β as the virtual controller of the inductor currenti_L. Now, simplifying Eqn. (18) using Eqn. (11)

$$\begin{aligned} D^{\alpha}V_1 &\le (\tfrac{1}{C}(e_2 + \beta - i_R - i_P) - \\ &\quad D^{q_1}\tilde{v}_C)\ \text{sign}(D^{q_1-\alpha}e_1) \\ &\le \frac{1}{C}(\beta + e_{2)}\ \text{sign}(D^{q_1-\alpha}e_1) \\ &\quad + \left(\frac{1}{C}(i_R - i_P) - D^{q_1}\tilde{v}_C\right)\text{sign}(D^{q_1-\alpha}e_1) \end{aligned} \tag{19}$$

To eliminate the second term of expression (19), the stabilizing controller β that leads to desirable convergence with time of the second subsystem (5) is chosen as $\beta = -CK_1D^{q_1-\alpha}e_1 + CD^{q_1}\tilde{v}_C + i_R + i_P$.

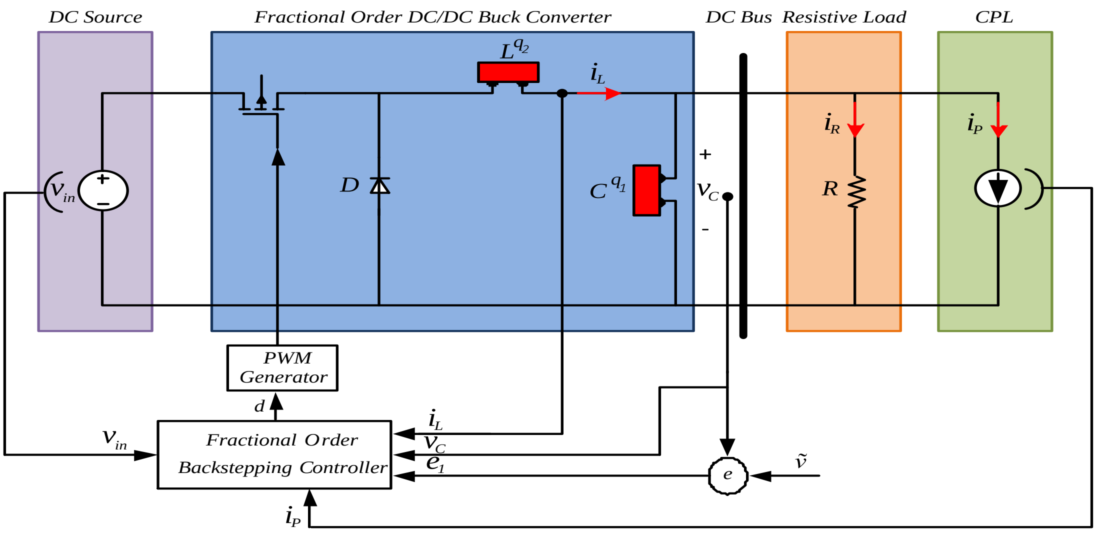


Fig. 2. Control architecture of the FO BSC for FO buck converter with a CPL

Then, the first fractional Lyapunov function can be rewritten as

$$\begin{aligned} D^{\alpha}V_1 &\le -K_1D^{q_1-\alpha}e_1\text{sign}(D^{q_1-\alpha}e_1) \\ &\quad + \frac{1}{C}e_2\text{sign}(D^{q_1-\alpha}e_1) \\ &\le -K_1|D^{q_1-\alpha}e_1| + \tfrac{1}{C}e_2\text{sign}(D^{q_1-\alpha}e_1) \end{aligned} \tag{20}$$

Step 2

Taking the second subsystem of system (5)

$$\frac{d^{q2}i_L}{dt^{q2}} = \frac{v_{in}}{L}d - \frac{v_C}{L}. \tag{21}$$

Again, taking the q_2 order derivative of the second tracking error e_2 and using the linear property, Eqn. (11) is expressed as

$$D^{q_2}e_2 = D^{q_2}i_L - D^{q_2} \tag{22}$$

Now, a new Lyapunov function for subsystem (21) is selected as

$$V_2 = V_1 + |D^{q_2-\alpha} e_2| \tag{23}$$

whose α order derivative is expressed as

$$\begin{aligned} D^{\alpha} V_2 &= D^{\alpha} V_1 + D^{\alpha} |D^{q_2-\alpha} e_2| \\ &\leq D^{\alpha} V_1 + D^{q_2} e_2 \text{sign}(D^{q_2-\alpha} e_2) \end{aligned} \tag{24}$$

Then, using Eqn. (20) into Eqn. (24), we get

$$\begin{aligned} D^{\alpha} V_2 \leq -K_1 |D^{q_1-\alpha} e_1| + \frac{1}{C} e_2 \text{sign}(D^{q_1-\alpha} e_1) \\ + D^{q_2} e_2 \text{sign}(D^{q_2-\alpha} e_2) \end{aligned} \tag{25}$$

By inserting e_2 from Eqn. (22) and substituting Eqn. (21) into Eqn. (25) one has

$$\begin{aligned} D^{\alpha} V_2 &\leq -K_1 |D^{q_1-\alpha} e_1| + \frac{1}{C} e_2 \text{sign}(D^{q_1-\alpha} e_1) \\ &\quad + D^{q_2}(i_L - \beta) \text{sign}(D^{q_2-\alpha} e_2) \\ &\leq -K_1 |D^{q_1-\alpha} e_1| + \frac{1}{C} e_2 \text{sign}(D^{q_1-\alpha} e_1) \\ &\quad + (D^{q_2} i_L - D^{q_2} \beta) \text{sign}(D^{q_2-\alpha} e_2) \\ &\leq -K_1 |D^{q_1-\alpha} e_1| + \frac{1}{C} e_2 \text{sign}(D^{q_1-\alpha} e_1) \\ &\quad - D^{q_2} \beta \text{sign}(D^{q_2-\alpha} e_2) \\ &\quad + \left[\frac{v_{in}}{L} d - \frac{v_C}{L}\right] \text{sign}(D^{q_2-\alpha} e_2) \end{aligned} \tag{26}$$

The main objective is to enforce DC bus voltage v_C to track its reference value $\tilde{v}_C$, which means the error e_1 converges to zero as $t \to \infty$. By using the above lemma, the FO time derivative of Lyapunov function (26) should reduce to: $D^{\alpha} V_2 \leq -K_1 |D^{q_1-\alpha} e_1| - K_2 |D^{q_2-\alpha} e_2|$ with K_1 and K_2 are positive constants. Thus, the overall controller d that ensures an asymptotic tracking for the FO system (5), can finally be expressed as

$$\begin{aligned} d = \frac{1}{v_{in}} \Big[& e_1 + \tilde{v}_C + L D^{q_2} \beta \\ & - \frac{L}{C} e_2 \text{ sign}(D^{q_1-\alpha} e_1) \text{sign}(D^{q_2-\alpha} e_2) \\ & - L K_2 D^{q_2-\alpha} e_2 \Big] \end{aligned} \tag{27}$$

Remark 1

As indicated above, system (5) degrades under incommensurate fractional order system because it has arbitrary orders ($q_1 \neq q_2$). That is why we proposed an unsmooth Lyapunov function in the form as $V_n = V_{n-1} + |D^{q_n-\alpha} e_n|$ in order to prove the system's stability. furthermore, this function is still validated for a commensurate FO buck converter.

Remark 2

As many works were used the IO version of DC/DC converter feeding CPL to derive the traditional back-stepping controller based on integer Lyapunov function. However, the controller and the converter performances are still limited. In this work, a FO buck converter is considered. Extending the FO backstepping control via a FO Lyapunov function to control the FO converter is our main aim, for totally overcoming the instability caused by CPL. It is worth mentioning that when the system's orders satisfy ($q_1 = q_2 = 1$), it gives the same results as of the integer version.

Table 1. Simulation setup parameters

System parameters	Description	Value	Unit
f	Switching frequency	25	kHz
C^{q_1}	Capacitor	200	$\mu F/s^{1-q_1}$
L^{q_2}	Inductor	20	mH/s^{1-q_2}
v_{in}	Converter input voltage	100	V
R	Damping resistor	5	Ω
q_1	Capacitor's fractional order	0.96	
q_2	Capacitor's fractional order	0.97	
K_1	Controller parameter	1000	
K_2	Controller parameter	500	

4 Simulation results

In this section, MATLAB /Simulink is used as a platform to validate the obtained results. Figure 2 shows the system model with the derived controller where the CPL is presented by a controlled current source, hence the CPL value can be controlled easily. The details of the designed system are stated in Tab. 1. Currently, fractional order components of specific order are not directly presented in Simulink environment. Therefore, in this paper, ORA method is employed to construct the real FO devices of the buck converter by integer order well-known components. Then, the closed-loop response is assessed under four scenarios, the worst-case of which would occur when the load is pure CPL (the resistive load is unloaded).

4.1 Oustaloup recursive approximation

From Tab. 1, the operating frequency of the buck converter is $f = 25$ kHz. Thus, Oustaloup approximation requirements are chosen to obtain an accurate circuit model of the FO storage elements. The Oustaloup' parameters are the fitting frequency bands $w_b = 10^{-2}\ \mathrm{rds}^{-1}$, $w_h = 10^{7}\ \mathrm{rds}^{-1}$, and the order of Oustaloup filter $N = 8$.

Applying ORA method, the integer order transfer function TFC_{ORA} of the FO capacitor C_{q_1}=200 mF/s^{1-q_1} with $q_1 = 0.96$ can be expressed as

$$TFC_{ORA} = \frac{1}{C} s^{-q_1} \tag{28}$$

To calculate the parameters of equivalent model of the FO capacitor, as shown in Fig. 3, undetermined coefficients method is used. We compare the formulas of its approximate transfer function TFC_{ORA} and the impedance of the chain circuit:

$$TFC_{ORA} \approx \sum_{i=1}^{n} \frac{{}^{1}/{}_{C_i}}{s + {}^{1}/{}_{R_{C_i} C_i}} + R_{C_{in}} \tag{29}$$

Solving Eqn. (29), calculated values $R_{C_{in}}$, R_{C_i} and C_i of the constructed chain fractance for the FO capacitor are as follows: $R_{C_{in}} = 0.95\ \mathrm{m\Omega}$, $R_{C_1} = 1\ \mathrm{m\Omega}$, $R_{C_2} = 13.46\ \mathrm{m\Omega}$, $R_{C_3} = 0.16\ \Omega$, $R_{C_4} = 1.97\ \Omega$, $R_{C_5} = 23.54\ \Omega$, $R_{C_6} = 283\ \Omega$, $R_{C_7} = 3.65\ \mathrm{k\Omega}$, $R_{C_8} = 412\ \mathrm{k\Omega}$, $C_1 = 1.21$ mF, $C_2 = 1.25$ mF, $C_3 = 1.39$ mF, $C_4 = 1.53$ mF, $C_5 = 1.7$ mF, $C_6 = 1.89$ mF, $C_7 = 1.95$ mF, $C_8 = 0.23$ mF.

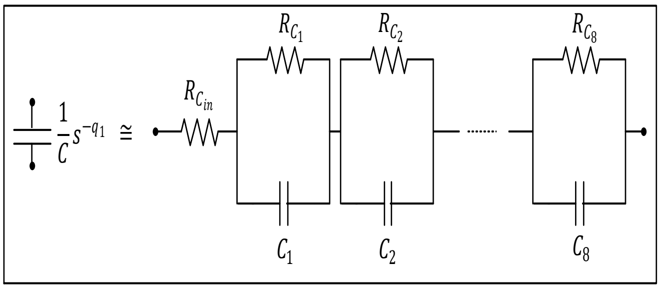


Fig. 3. Fractional order capacitor's equivalent circuit

The integer order transfer function TFL_{ORA} for the FO inductor $L_{q_2} = 20\ \mathrm{mH/s}^{1-q_2}$ with $q_2 = 0.97$ can be expressed in the same way as shown above

$$TFL_{ORA} = \frac{1}{L} s^{-q_2} \tag{30}$$

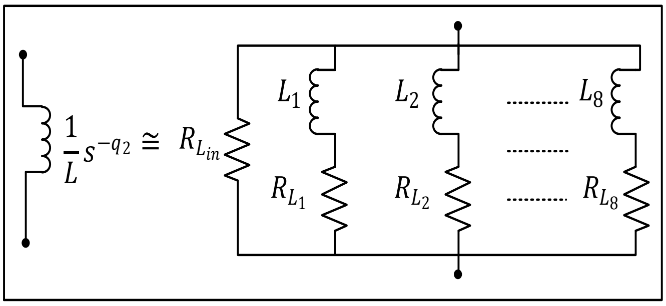


Fig. 4. Fractional order inductor's equivalent circuit

As exhibited in Fig. 4, for calculation the parameters of chain structure of the FO inductor, undetermined coefficients method is also used. We compare the formulas of its approximate transfer function TFL_{ORA} and the impedance of the chain circuit:

$$TFL_{ORA} \approx \sum_{i=1}^{n} \frac{{}^{1}/{}_{L_i}}{s + {}^{R_{L_i}}/{}_{L_i}} + \frac{1}{R_{L_{in}}} \tag{31}$$

Similarly, solving Eqn. (31), calculated values $R_{L_{in}}$, R_{L_i} and L_i of the constructed chain fractance for the FO capacitor are as follows: $R_{L_{in}} = 123\ \mathrm{k\Omega}$, $R_{L_1} = 145\ \mathrm{k\Omega}$, $R_{L_2} = 10.9\ \mathrm{k\Omega}$, $R_{L_3} = 884\ \Omega$, $R_{L_4} = 70.76\ \Omega$, $R_{L_5} = 5.8\ \Omega$, $R_{L_6} = 0.46\ \Omega$, $R_{L_7} = 35\ \mathrm{m\Omega}$, $R_{L_8} = 0.23\ \mathrm{m\Omega}$, $L_1 = 0.19$ H, $L_2 = 0.19$ H, $L_3 = 0.2$ H, $L_4 = 0.22$ H, $L_5 = 0.24$ H, $L_6 = 0.25$ H, $L_7 = 0.25$ H, $L_8 = 22.2$ mH.

Remark 3

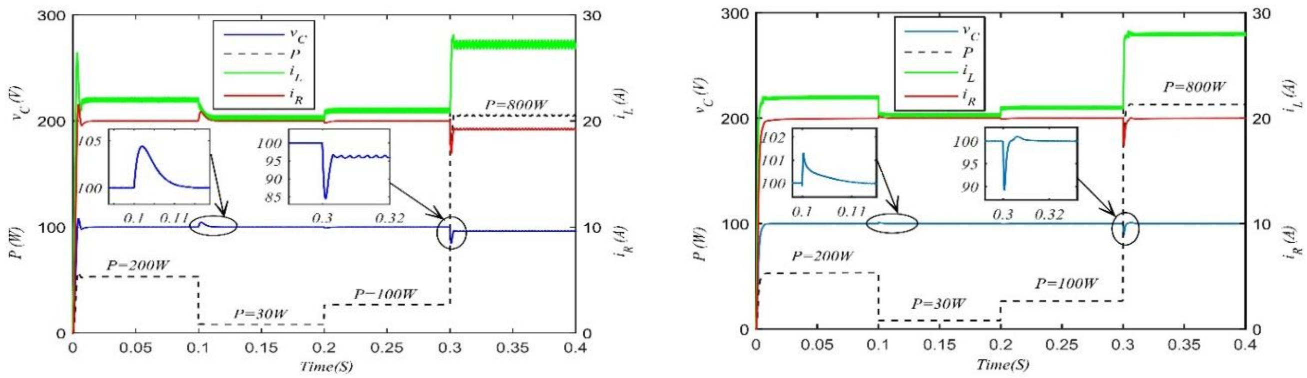
As discussed above, the FO capacitor and inductor are currently unavailable. Therefore, an approximation method should be used in the majority of cases. In our work, the aforementioned problem of building equivalent models of these FO elements has been approached by using Oustaloup recursive approximation within an appropriate frequency band. Indeed, the majority of published studies have indicated the correct model using ORA method [33, 34], confirming the accuracy of the characteristic analysis of FO inductor and capacitor in accordance with the theoretical results.

While designing the entire system depicted in Fig. 2, particularly for potential future experimental implementation, the following steps should be carefully considered to minimize limitations and maximize flexibility:

1. Select an appropriate fractional order for each energy-storage device (q_1 , q_2), which is usually close to 1, so that the fractional converter that requires a higher control performance and ripple requirement can be designed.
2. Choose an appropriate rational approximation method such as Cherff's method, Oustaloup's recursive method, etc.
3. Choose suitable Oustaloup parameters that are related to a certain frequency range (w_b , w_h , N). That is why the approximation effect will be better at the desired operating frequency.
4. Determine the parameters of the manually tuned FO BSC controller (K_1 , K_2).
5. Choose an optimal memory length: A short memory may lead to the same result as obtained in the integer systems or even some inaccuracy outcomes, approximately, and a long memory may lead to more computational burden problems as well. Evaluation focusing on the memory length of the system response was discussed in [5].

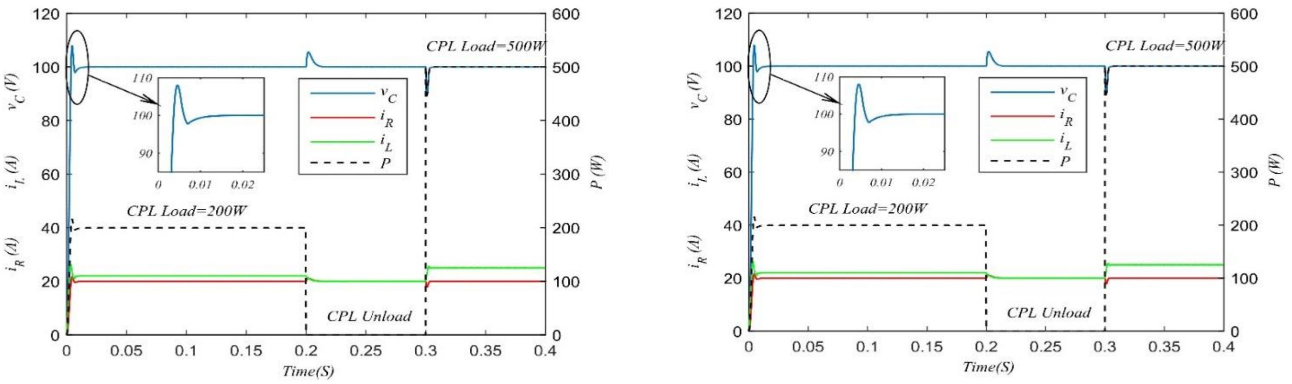
4.2 Test under CPL power variation

In the first scenario, the test is carried out to check the effect of sudden changes in CPL output on the DC bus voltage. As depicted in Fig. 5, the CPL variation values are as follows: first, the CPL value is fixed at 200 W. We noted that the FO backstepping controller reaches the DC bus voltage within the desired settling time 8.4 ms and there is no overshoot recorded. After that, a critical transition is performed from 200 W to 30 W in 0.1 s. An overshoot of 5 V is recorded for the integer order converter within 0.01 s.



(a) (b)

Fig. 5. Simulation results with a changing CPL: (a) Conventional backstepping control, (b) Fractional order backstepping control



(a) (b)

Fig. 6. Simulation results with a CPL load and unload: (a) Conventional backstepping control. (b) Fractional order backstepping control

Table 2. Comparing controllers performance under CPL change

Controller (q_1, q_2)	Settling time (ms)	Maximum overshoot (V)	Maximum undershoot (V)	Error values v_C(V)
IO (1,1)	16	8	15.53	3.5
FO $(0.96, 0.97)$	8.4	1.3	10.65	0

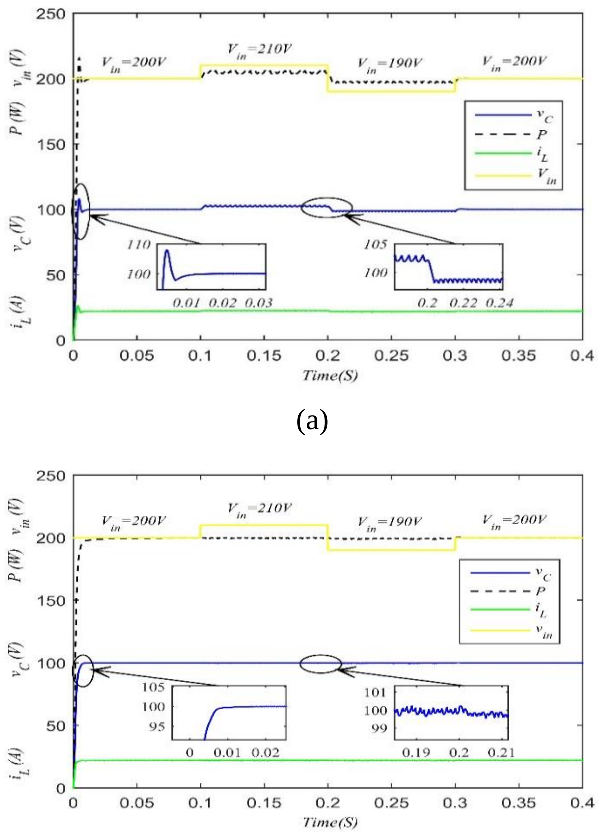
However, using a FO buck converter controlled by a FO BSC can effectively reduce the oscillation caused by even large CPL variations. Then, at time 0.2 ms, the system is reevaluated under a sudden change in CPL from 30 W to 100 W. All controllers can ensure system stability in this case, as the DC bus voltage precisely tracks its reference value. Finally, the CPL reaches a high value of 800 W at 0.3 ms. At this step of change, the IO controller is ineffective for maintaining the system performance and leads to a smaller stability margin, in which the output voltage drops by 3.8 V and interesting oscillations are observed, as noticed in Tab. 2. Furthermore, the CPL changes in a wide range with a substantial undershoot of 15.53 V. However, the system response of the FO converter is stable steadily against the disturbance caused by the large CPL current.

To further demonstrate the robustness of the designed system with a FO buck converter, another test is carried out under a sudden removal of the CPL load. As is shown in Fig. 6, the CPL is suddenly unloaded from 0.2 ms to 0.3 ms. The important thing here is that the DC bus voltage of the IO converter returns rapidly to its desired value of 100 V, but serious fluctuations are recorded, causing less stability. Besides, the DC bus voltage of FO converter has a small overshoot, and the system is always stable. Therefore, the controller's robustness in terms of stability will be ensured when a FO system controlled by a FO nonlinear controller is used.

4.3 Test under input voltage variation

The second test is used to validate the superiority of the proposed FO system when the input voltage changes from 200 V to 210 V, 210 V to 190 V, and 190 V to 200 V at moments of 0.1 ms, 0.2 ms and 0.3 ms, respectively. Figure 7 illustrates the response waveforms of the two systems. As given in Tab. 3, the conventional BSC controller reaches its steady state within 16 ms, recor-ding an overshoot of 8 V, but the FO BSC controller has a better response speed, and no overshoot is recorded. The input voltage is increased from 200 V to 210 V in 0.2 ms. It can be noted that the IO converter has a certain deviation from the voltage of the DC bus of 2.5 V, thus causing a significant fluctuation in the CPL. Moreover, at t = 0.3 ms, the voltage of the main bus also drops to 97.3 V compared to its reference voltage. Therefore, under input voltage variation, the conventional BSC controller cannot guarantee system stability. Whereas, applying the proposed control technique for the FO buck converter is effective in avoiding the system destabilization issues caused by a certain input voltage scope, providing a stable DC bus voltage.

As previously stated, the FO buck converter feeding a CPL has a smooth dynamic performance and neglected steady state error, ratifying the robustness of the suggested control method.



(a)

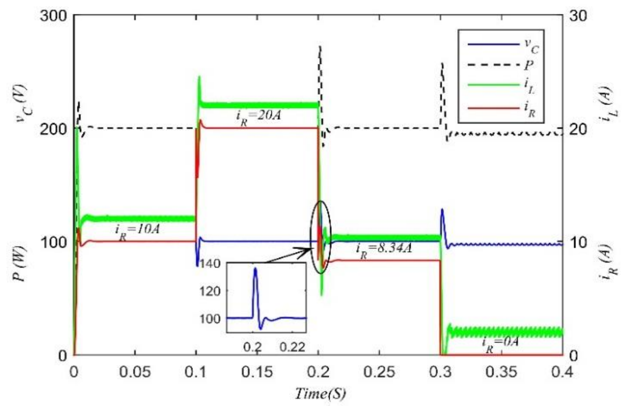
(b)

Fig. 7. Simulation results with a changing input voltage: (a) Conventional backstepping control, (b) Fractional order backstepping control

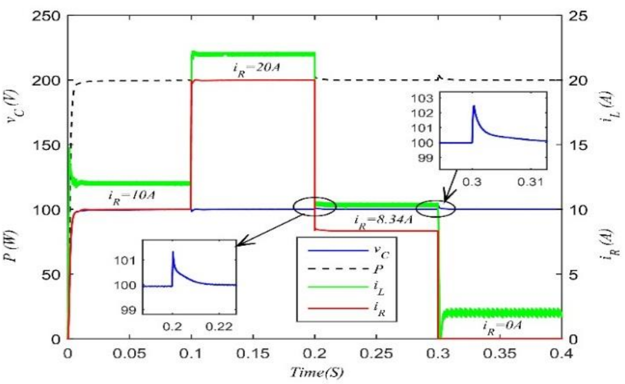
Table 3. Comparing controllers performance under input voltage variation

Controller (q_1, q_2)	Settling time (ms)	Maximum overshoot (V)	Maximum undershoot (V)	Error values v_C(V)
IO (1,1)	16	8	2.24	2
FO (0.96, 0.97)	8.4	0	0	0.05

4.4 Test under resistive load variation



(a)



(b)

Fig. 8. Simulation results with a changing resistive load: (a) Conventional backstepping control, (b) Fractional order backstepping control

The impact of resistive load variation on the response waveforms of the FO buck converter is depicted in Fig. 8. The resistive load varies from 10 Ω to 5 Ω and 5 Ω to 12 Ω at 0.1 ms and 0.2 ms, respectively. From examining Tab. 3, a serious overshoot of 36.2 V of DC bus voltage is observed for the integer order converter at 0.2 ms. Whereas, the FO buck converter has a small overshoot of 2.5 V and better response speed. The system is then loaded by a pure CPL at the moment 0.3 ms. Noticing that the IO controller is ineffective for maintaining the system performance when the resistive load is unloaded and that it leads to interesting oscillations in which the output voltage drops by 2.89 V. However, the system response of the FO converter is stable steadily with almost no error in the presence of resistive load variation. Therefore, the controller's robustness in terms of stability will be enhanced when a FO buck converter controlled via a FO BSC controller is used.

4.5 Discussion

The chief purpose of this study is to enhance the stability of DC microgrids in the presence of CPLs, which pose significant challenges due to their INI characteristics. To address these stability concerns, a FO system is implemented and evaluated under various conditions, including CPL variation, input voltage fluctuations, and resistive load changes. These variations are introduced to assess the robustness of the proposed system and controller under worst-case scenarios, such as pure CPL conditions, which are known to induce severe oscillations and potential instability in DC microgrids.

One of the primary advantages of employing a FO inductor with a suitable fractional order of 0.97 in the buck converter is the ability to finely tune the i_L ripples, offering a greater degree of control and flexibility compared to traditional IO inductors. This enhanced adaptability allows for better energy management and improved transient performance. Similarly, utilizing a FO capacitor with a suitable fractional order of 0.96 significantly mitigates DC bus voltage oscillations compared to its IO counterpart, thereby enhancing voltage regulation and system stability. These findings confirm that the fractional-order elements provide superior damping effects, reducing unwanted fluctuations and improving overall power quality.

Furthermore, the nonlinear FO backstepping controller has a better settling time, smaller overshoot, and almost no steady-state error, outperforming the IO backstepping case. In addition, the chatter caused by CPL variation is greatly suppressed, thus significantly enhancing the system's overall performance and robustness.

Table 4. Comparing controllers performance under resistive load change

Controller (q_1, q_2)	Settling time (ms)	Maximum overshoot (V)	Maximum undershoot (V)	Error values v_C(V)
IO (1,1)	18	36.2	22.07	2.89
FO (0.96, 0.97)	11	2.5	10.65	0

5 Conclusion

Based on the concept of fractional calculus, a FO DC/DC buck converter is constructed, where the Oustaloup recursive approximation method is used over a predetermined operating frequency range. The fractional order devices are designed to investigate the dynamic response of the constructed converter. Considering the shortcomings of DC MGs introduced by CPLs, a fractional order version of the nonlinear backstepping control is designed to force the DC bus voltage to follow its desired value. Then, the asymptotic stability of the FO buck converter under the proposed controller is proved via an unsmooth nonlinear Lyapunov function. Through simulations validation, it should be noted that the traditional backstepping controller could not totally guarantee stable operation in DC-MGs, which is attributed to substantial fluctuations in power supply and loads. However, we demonstrate the effectiveness of the proposed approach in mitigating the destabilizing effects of CPLs and improving energy conversion efficiency. The results indicate significant improvements in system stability and transient response compared to traditional control methods. This approach holds promise for various energy conversion applications where CPLs pose challenges to system performance and stability. It should be mentioned that the proposed method can be used to control other FO DC/DC power converters, such as boost converters and buck-boost converters, confirming the conclusion that the suggested controller is strong and efficient.

References

[1] I. Petráš, "Novel fractional-order model predictive control: State-space approach," *IEEE Access,* vol. 9, pp. 92769-92775, 2021.

[2] E. Bouguenna, S. Ladaci, and W. Merrouche, "Stability and Performance Enhancement of a Step-Down Converter in Photovoltaic Systems Using an Optimization Algorithm-Based Fractional PIλDδ Controller," in *International Conference on Artificial Intelligence in Renewable Energetic Systems,* 2024: Springer, pp. 170-178.

[3] S. Djebbri, S. Ladaci, A. Metatla, and H. Balaska, "Fractional-order model reference adaptive control of a multi-source renewable energy system with coupled DC/DC converters power compensation," *Energy Systems,* vol. 11, no. 2, pp. 315-355, 2020.

[4] J. Hidalgo-Reyes, J. F. Gómez-Aguilar, R. F. Escobar-Jiménez, V. M. Alvarado-Martínez, and M. López-López, "Classical and fractional-order modeling of equivalent electrical circuits for supercapacitors and batteries, energy management strategies for hybrid systems and methods for the state of charge estimation: A state of the art review," *Microelectronics Journal,* vol. 85, pp. 109-128, 2019.

[5] I. Petráš and J. Terpák, "Fractional calculus as a simple tool for modeling and analysis of long memory process in industry," *Mathematics,* vol. 7, no. 6, p. 511, 2019.

[6] X. Wang, R. Zhuang, and J. Cai, "Theoretical Analysis of a Fractional-Order LLCL Filter for Grid-Tied Inverters," *Fractal and Fractional,* vol. 7, no. 2, p. 135, 2023.

[7] L. Xie, Z. Liu, K. Ning, and R. Qin, "Fractional-Order Adaptive Sliding Mode Control for Fractional-Order Buck-Boost Converters," *Journal of Electrical Engineering & Technology,* vol. 17, no. 3, pp. 1693-1704, 2022.

[8] F. Tong, W. Wei, M. Jin, X. Sun, Q. Wang, and Q. Luo, "Optimal Fractional-Order Proportion Integration Differentiation Control of Proton Exchange Membrane Electrolyzer for Offshore Wind Power Hydrogen Production System," *Energy Technology,* vol. 11, no. 9, p. 2300100, 2023.

[9] X. Wang, W. Song, H. Wu, H. Liang, and A. Saboor, "Microgrid operation relying on economic problems considering renewable sources, storage system, and demand-side management using developed gray wolf optimization algorithm," *Energy,* vol. 248, p. 123472, 2022.

[10] J. J. C. Mancera *et al.*, "Experimental analysis of the effects of supercapacitor banks in a renewable DC microgrid," *Applied Energy,* vol. 308, p. 118355, 2022.

[11] B. A. Martinez-Treviño, A. El Aroudi, A. Cid-Pastor, and L. Martinez-Salamero, "Nonlinear control for output voltage regulation of a boost converter with a constant power load," *IEEE Transactions on Power Electronics,* vol. 34, no. 11, pp. 10381-10385, 2019.

[12] S. Mehta and P. Basak, "A comprehensive review on control techniques for stability improvement in microgrids," *International Transactions on Electrical Energy Systems,* vol. 31, no. 4, p. e12822, 2021.

[13] K. A. Al Sumarmad, N. Sulaiman, N. I. A. Wahab, and H. Hizam, "Energy management and voltage control in microgrids using artificial neural networks, PID, and fuzzy logic controllers," *Energies,* vol. 15, no. 1, p. 303, 2022.

[14] Z. Zhang *et al.*, "An adaptive backstepping control to ensure the stability and robustness for boost power converter in DC microgrids," *Energy Reports,* vol. 8, pp. 1110-1124, 2022.

[15] M. S. Ali, A. M. Hussein, S. A. Hawash, and M. Soliman, "Stability of DC Boost converter Feeding Constant Power Load using Fuzzy Controller Based Lyapunov," *International Journal of Electronics,* vol. 109, no. 8, pp. 1352-1373, 2022.

[16] M. Boukerdja, A. Chouder, L. Hassaine, B. O. Bouamama, W. Issa, and K. Louassaa, "H∞ based control of a DC/DC buck converter feeding a constant power load in uncertain DC microgrid system," *ISA transactions,* vol. 105, pp. 278-295, 2020.

[17] M. Irshad, N. K. Vemula, R. Devarapalli, G. V. N. Kumar, and Ł. Knypiński, "An optimized integral performance criterion based commercial PID controller design for boost converter," *Journal of Electrical Engineering,* vol. 75, no. 4, pp. 258-267, 2024.

[18] M. Asghar, A. Khattak, and M. M. Rafiq, "Comparison of integer and fractional order robust controllers for DC/DC converter feeding constant power load in a DC microgrid," *Sustainable Energy, Grids and Networks,* vol. 12, pp. 1-9, 2017.

[19] J. C. Mayo-Maldonado, G. Fernandez-Anaya, and O. F. Ruiz-Martinez, "Stability of conformable linear differential systems: a behavioural framework with applications in fractional-order control," *IET Control Theory & Applications,* vol. 14, no. 18, pp. 2900-2913, 2020.

[20] D. Youcef, K. Khatir, and B. Yassine, "Design of neural network fractional-order backstepping controller for MPPT of PV systems using fractional-order boost converter," *International Transactions on Electrical Energy Systems,* vol. 31, no. 12, p. e13188, 2021.

[21] A. J. Calderón, B. M. Vinagre, and V. Feliu, "Linear fractional order control of a DC-DC buck converter," in *2003 European Control Conference (ECC),* 2003: IEEE, pp. 1292-1297.

[22] S. Surya and S. Williamson, "Generalized circuit averaging technique for two-switch PWM DC-DC converters in CCM," *Electronics,* vol. 10, no. 4, p. 392, 2021.

[23] I. Petráš, *Fractional-order nonlinear systems: modeling, analysis and simulation*. Springer Science & Business Media, 2011.

[24] Z. Li, L. Liu, S. Dehghan, Y. Chen, and D. Xue, "A review and evaluation of numerical tools for fractional calculus and fractional order controls," *International journal of control,* vol. 90, no. 6, pp. 1165-1181, 2017.

[25] K. Khettab, Y. Bensafia, and S. Ladaci, "Chattering elimination in fuzzy sliding mode control of fractional chaotic systems using a fractional adaptive proportional integral controller," *International Journal of Intelligent Engineering and Systems,* vol. 10, no. 5, pp. 255-266, 2017.

[26] Z. Jia, L. Liu, and C. Liu, "Dynamic Analysis and Fractional-Order Terminal Sliding Mode Control of a Fractional-Order Buck Converter Operating in Discontinuous Conduction Mode," *International Journal of Bifurcation and Chaos,* vol. 32, no. 04, p. 2250045, 2022.

[27] S. Westerlund, "Dead matter has memory!," *Physica Scripta,* vol. 43, no. 2, pp. 174-179, 1991/02/01 1991, doi: 10.1088/0031-8949/43/2/011.

[28] S. Westerlund and L. Ekstam, "Capacitor theory," *IEEE Transactions on Dielectrics and Electrical Insulation,* vol. 1, no. 5, pp. 826-839, 1994.

[29] S. Fang and X. Wang, "Modeling and analysis method of fractional-order buck–boost converter," *International Journal of Circuit Theory and Applications,* vol. 48, no. 9, pp. 1493-1510, 2020.

[30] K. Khettab, S. Ladaci, and Y. Bensafia, "Fuzzy adaptive control of fractional order chaotic systems with unknown control gain sign using a fractional order Nussbaum gain," *IEEE/CAA Journal of Automatica Sinica,* vol. 6, no. 3, pp. 816-823, 2016.

[31] T. Gebremedhin Hailu, L. Mackay, L. M. Ramirez-Elizondo, and J. A. Ferreira, "Voltage weak DC distribution grids," *Electric Power Components and Systems,* vol. 45, no. 10, pp. 1091-1105, 2017.

[32] S. Singh, D. Fulwani, and V. Kumar, "Emulating DC constant power load: A robust sliding mode control approach," *International Journal of Electronics,* vol. 104, no. 9, pp. 1447-1464, 2017.

[33] A. Oustaloup, F. Levron, B. Mathieu, and F. M. Nanot, "Frequency-band complex noninteger differentiator: characterization and synthesis," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 47, no. 1, pp. 25-39, 2000.

[34] Y. Bensafia, S. Ladaci, K. Khettab, A. Chemori, " Fractional order model reference adaptive control for SCARA robot trajectory tracking," *International Journal of Industrial and Systems Engineering* vol. 30, no. 2, pp. 138-156, 2018.

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