Journal of Electrical Engineering, Vol. 76, No. 2, 2025, pp. 159-165

Transformer matching low noise amplifier with dual-mode g_m enhancement technique

Dheeraj Kalra[1], Mayank Srivastava[2]

This paper presents realization of a Low Noise Amplifier (LNA) using the transformer matching with the active and passive g_m enhancement technique. This research also falls within the domain of 5G communication system receivers. Cascode structure is used to improve the gain of the circuit while mutual coupling helped in decreasing the area of realized LNA. The input and output ports have been matched for 50 Ω termination. The realized LNA has maximum gain of 14.35 dB at 6.44 GHz while the minimum value of Noise Figure (NF) is 4.43 dB. The S_{11} value is less than –9 dB from frequency 6.2 GHz to 7.2 GHz, i.e., having the bandwidth of 1 GHz. The realized LNA is simulated on Cadence Virtuoso software using 45 nm CMOS technology. The layout for the realized LNA is drawn occupying the area of 439 μm × 373 μm, thus 0.164 mm^2. Comparison of performance parameters with other references is depicted in Tab. 2.

Keywords: LNA, cascode configuration, mutual coupling

1 Introduction

There is always demand of the wideband receiver that can consume low power so that the battery life can be increased. The research also falls in the field of 5G communication system. The second block in the receiver circuit is LNA whose function is to amplify the signal while reducing the effect of noise and there is always focus on increasing LNA's Figure of Merit (FoM). The researchers tried to incorporate various topologies to increase the FoM. In [1], the use of a multi-coupled transformer helped in boosting the gain of the LNA. This is advantageous for applications that require high signal amplification. The LNA [1] operated in the K-band frequency range which is 18 to 27 GHz.

In [2], the LNA operates in the frequency range of 76.5 to 92.6 GHz, which is suitable for millimeter-wave applications such as high-speed wireless communication and radar systems. The LNA utilizes the two-port kQ-product theory for transformer design. This approach allows for efficient impedance matching and improved signal transfer, leading to enhanced performance. In [3], the LNA covers a wide frequency range of 0.2 to 1.6 GHz, making it suitable for a variety of applications spanning different frequency bands within this range. Proposed LNA offers a bandwidth of 20 MHz, enabling it to handle signals with a relatively wide range of frequencies. The LNA exploits a passive design, eliminating the need for an active biasing circuitry and reducing power consumption. Passive LNAs are generally simpler and offer improved linearity and power efficiency. The proposed LNA utilizes an N-Path 1:3 transformer, which enables impedance transformation and signal amplification. The LNA is designed for a specific frequency range of 0.2 to 1.6 GHz.

In [4], the LNA is designed to operate in two frequency bands, 28 GHz and 39 GHz, making it suitable for multi-band applications. The LNA incorporates a shunt-series transformer feedback technique, which helps in achieving wideband impedance matching and improving gain performance. The paper reports good performance metrics such as low NF, high gain, and good input/output matching in both frequency bands. In [5], the LNA incorporates a channel-selection mechanism using a switched-capacitor-transformer network, allowing for the selection of specific frequency channels within the operating range. The LNA achieves a high output third-order intercept point (OB-IIP$_3$) of 23.5 dBm, indicating good linearity and the ability to handle high-power signals without significant distortion. The paper reports a low NF of 3.4 to 4.8 dB. The LNA utilizes an N-Path architecture, which is known for its good linearity, high dynamic range, and ability to handle large input signals.

In [6], the proposed LNA operates in a wide frequency range of 50 to 67 GHz, making it suitable for millimeter-wave applications such as high-speed wireless communication systems. The LNA utilizes a double-transformer-coupling technique, which can provide improved input/output matching and enhanced

[1] Department of ECE, GLA University, Mathura, 281406, India
[2] Department of ECE, National Institute of Technology, Jamshedpur, 831014, India
[1]dheeraj.kalra@gla.ac.in, [2]mayank.ece@nitjsr.ac.in

https://doi.org/10.2478/jee-2025-0016, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

gain performance compared to traditional coupling techniques. The LNA incorporates self-resonant matching techniques, which can simplify the design and improve the matching performance. In [7], the paper presents a CMOS LNA that integrates a transformer-based notch filter. This integrated design can provide improved rejection of unwanted signals or interference within a specific frequency range.

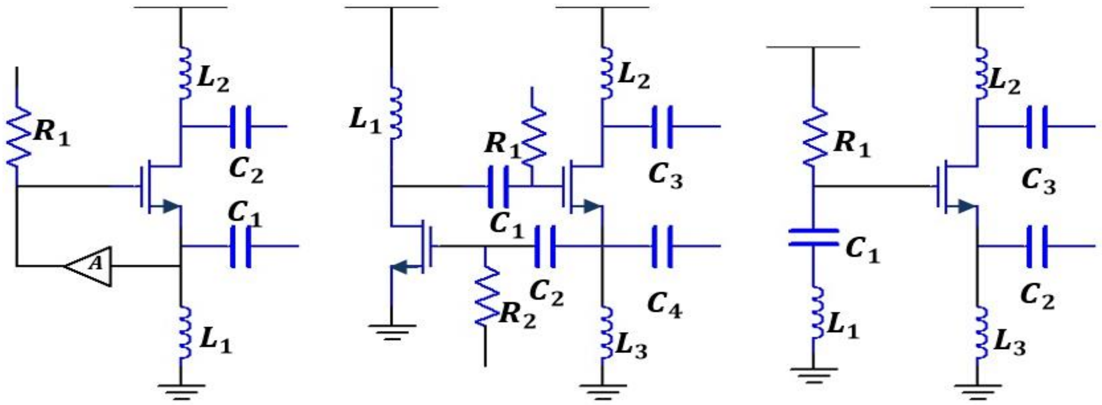

Fig. 1. (a) Generic g_m boosting, (b) CS active g_m boosting, (c) transformer based passive g_m boosting

In [8], the LNA utilizes a transformer-based input matching technique, which helps to improve impedance matching between the input signal and the amplifier. The paper introduces a pole-tuning technique, which allows for better control and optimization of the LNA's frequency response.

In [9], the paper presents a low-noise amplifier (LNA) design that operates over a wide frequency range of 27 to 46 GHz. The LNA utilizes a dual-resonant input matching technique, which helps to achieve improved impedance matching at multiple frequencies within the operating range. The paper introduces a transformer-based broadband output network, which facilitates impedance matching and power delivery to the load.

In [10], the paper presents a dual-band CMOS low-noise amplifier (LNA) design specifically tailored for 5G New Radio (NR) Frequency Range 2 (FR2) applications. It provides coverage for two frequency bands, which can enhance the versatility and compatibility of the LNA for multi-band communication systems. The LNA incorporates a transformer-based band-switchable load, which enables efficient impedance matching and power transfer at different operating frequencies. This load configuration allows for seamless switching between the two frequency bands without requiring additional circuitry. In [11], paper presents a LNA design that operates over a wide frequency range of 18 to 44 GHz. The LNA incorporates input matching techniques to achieve impedance matching between the signal source and the amplifier. The paper proposes bandwidth extension techniques to enhance the frequency range of the LNA. These techniques enable the amplifier to operate over a wider frequency band compared to traditional designs, thereby increasing its versatility [19, 20] and applicability.

The most popular g_m enhancement technique is that in which the gain is increased by improving the transconductance of the circuit.

The various g_m enhancement topology LNA circuits are shown in Fig. 1. As shown in Fig. 1(a), two Common Gate (CG) configurations are connected in cascade stage to provide the dual g_m enhancement. They do not use the CS stage in order to provide the good impedance matching. It consists of one main CG amplifier with the other g_m enhancement CG differential amplifier. The total transconductance of the circuit is increased from g_m to (1+A) g_m where A is the amplification factor. Figure 1(b) depicts the active g_m enhancement using CS amplifier. CS amplifier helped in increasing the gain of the circuit. While Figure 1(c) shows the transformer-based g_m enhancement technique.

2 Designed circuit

Figure 2 shows the steps of converting the second order band-pass filter into the transformer. Firstly, the capacitor C_2 split into the C_{21} and C_{22}. Obviously, C_{22} will be greater than C_2. Now C_{22} is converted into the parallel capacitor $C_4 = \frac{Q^2 C_{22}}{1+Q^2}$, where Q is the quality factor. In this process, the resistance R will be replaced by $(1 + Q^2)R$.

The first Norton transform is applied on the capacitor which resulted into the decrease in impedance by n_1^2 where n_1 is the capacitive transformation ratio. Similarly, next Norton transformation is applied on the inductor which resulted into an increase of the impedance by n_2^2, where n_2 is the inductive transformation ratio. Finally, an ideal transformer having turn ratio $k{:}n$ is inserted between the n_1C_4 and n_2L_1/n_1^2.

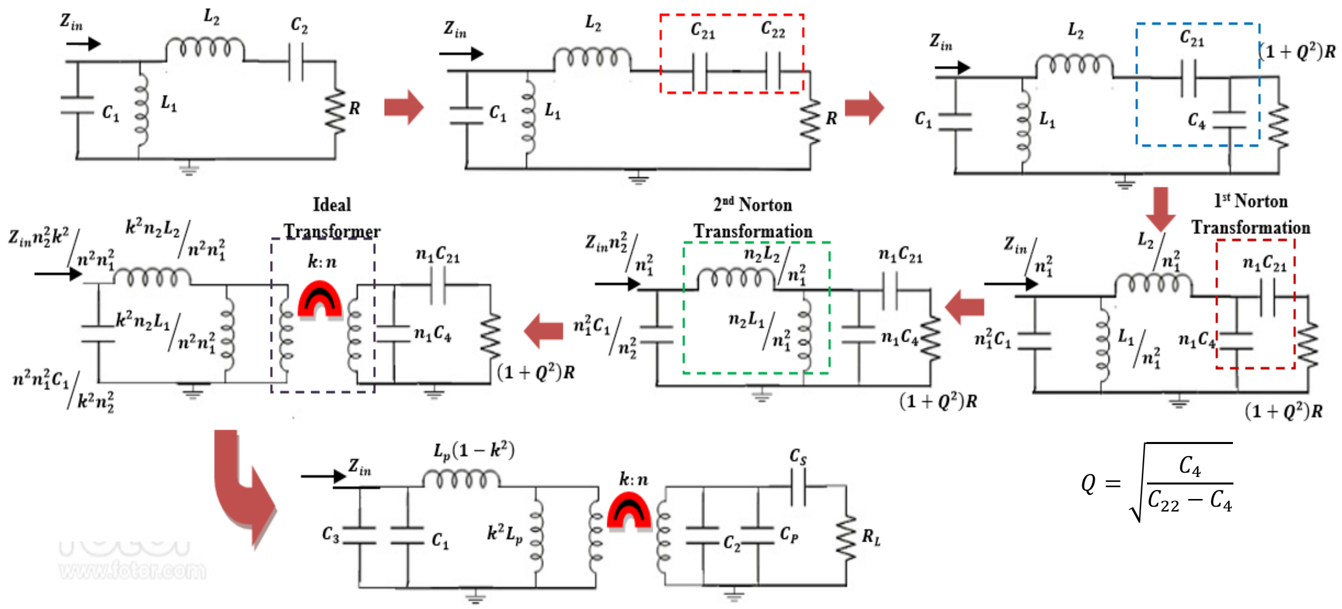

Fig. 2. Steps for converting the 2nd order band-pass filter into transformer

The proposed circuit is shown in Fig. 3 along with component dimensions depicted in Tab. 1. Transformer coupled active and passive g_m enhancement technique are used to improve the gain of circuit. Inductors L_3, L_4 and C_3 provide the separate DC current path for MOS M_2 and M_3 which is called as the folded cascode configuration. MOS M_3 is connected in CS configuration while MOS M_2 is connected in the CG configuration. L_3, L_4 and C_3 also help in providing inter-stage matching between M_2 and M_3.

The active g_m enhancement topology is introduced by the MOS M_1 while mutual coupling between L_1 and L_4 provide the passive g_m enhancement technique henceforth increasing the overall transconductance of proposed LNA. Magnetic coupling between L_1 and L_4 also provide the good impedance matching as well as require the less value of inductors and henceforth decreasing the circuit size. Figure 4 depicts the small signal model for the realized LNA.

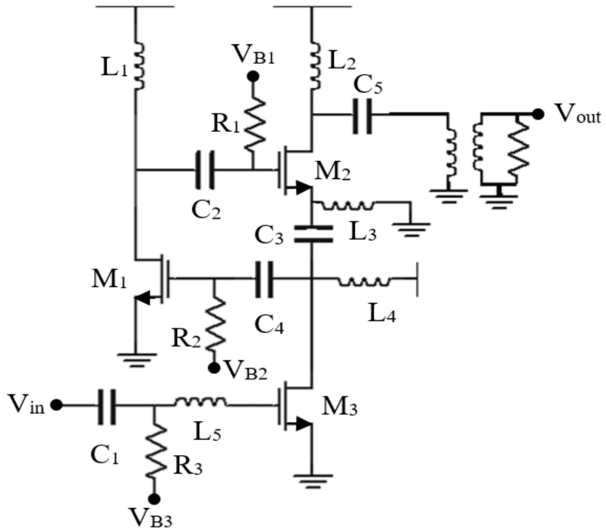

Fig. 3. Realized LNA circuit using active and passive g_m enhancement technique

Table 1. Component dimensions

M_1	18 µm/45 nm	L_1, L_4	1.8 nH
M_2	9 µm/45 nm	L_2	4.6 nH
M_3	9 µm/45 nm	L_3	2.5 nH
C_1-C_4	1 pF	L_5	4 nH
C_5	80 fF		

2.1 Input impedance

The impedance looking into the gate of the MOS M_3 considering the gate-source capacitance C_{gs3} is given by equation (1)

$$Z_{gs3} = \frac{1}{jwC_{gs3}} \quad (1)$$

where C_{gsi} is the gate to source capacitance for MOS M_i. The gate-drain capacitance C_{gd3} provides a feedback path [18]. To include its effect, we use Miller's theorem.

The Miller impedance due to C_{gd3} is:

$$Z_{gd3} = \frac{1}{jwC_{gd3}(1 - A_V)} \quad (2)$$

where A_V is the voltage gain from the gate to the drain of MOS M_3. For simplicity, let's assume the voltage gain $A_V \cong g_{m3}Z_{out3}$.

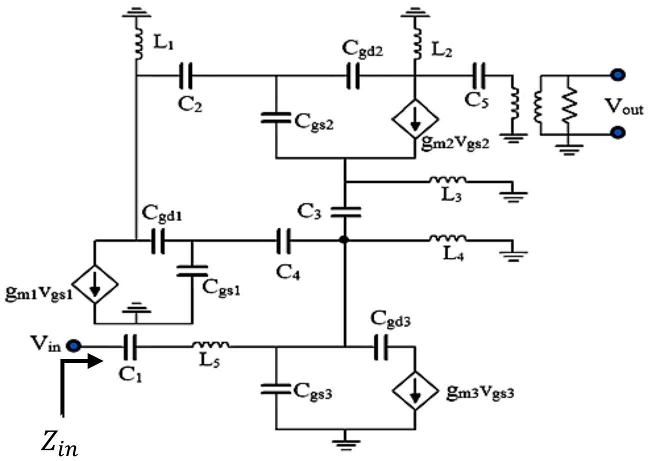

Fig. 4. Small signal model of realized LNA

The total impedance looking into the gate considering the Miller effect is:

$$Z_{in,GateM3} = \left(\frac{1}{jwC_{gs3}} \parallel \frac{1}{jwC_{gd3}(1 - A_V)}\right) \quad (3)$$

The input matching network consists of L_5 and C_1:

$$Z_{Match} = jwL_5 + \frac{1}{jwC_1} \quad (4)$$

The total input impedance looking into V_{in} is a parallel combination of the gate impedance and the matching network impedance:

$$Z_{in} = Z_{Match} \parallel Z_{in,GateM3} \quad (5)$$

$$Z_{in} = \left(jwL_5 + \frac{1}{jwC_1}\right) \parallel \left(\frac{1}{jwC_{gs3}} \parallel \frac{1}{jwC_{gd3}(1 - A_V)}\right) \quad (6)$$

$$Z_{in} = \left(jwL_5 + \frac{1}{jwC_1}\right) \parallel \left(\frac{1}{jw\left(C_{gs3} + C_{gd3}(1 - A_V)\right)}\right) \quad (7)$$

2.2. Gain calculation

The gain of input stage using MOS M_3 is given by

$$A_{V3} = -g_{m3}Z_{out3} \quad (8)$$

where

$$Z_{out3} = (jwL_3) \parallel \left(\frac{1}{jwC_{gd3}} \parallel \frac{1}{jwC_{gd2}}\right)$$

Now the gain provided by MOS M_1 can be calculated as

$$A_{V1} = -g_{m1}Z_{out1} \quad (9)$$

where

$$Z_{out1} = (jwL_4) \parallel \left(\frac{1}{jwC_{gd1}} \parallel \frac{1}{jwC_{gs2}}\right)$$

and the gain provided by MOS M_2 can be derived as

$$A_{V2} = -g_{m2}Z_{out2} \quad (10)$$

where

$$Z_{out2} = \left(\frac{1}{jwC_5} \parallel Z_{Load}\right)$$

Z_{Load} is the load connected at the output. Henceforth the overall gain is given by

$$A_V = A_{V1} \,.\, A_{V2} \,.\, A_{V3} \quad (11)$$

$$A_V = -g_{m1}Z_{out1} \cdot g_{m2}Z_{out2} \cdot g_{m3}Z_{out3} \quad (12)$$

3 Results and discussions

Figure 5 shows the simulation results for S_{11} with and without using L_1. L_1 inductor connected at the input showing the poor reflection. The inductor L_1 helps in achieving the impedance matching therefore minimum value of S_{11} is –19.26 dB at 6.68 GHz. The S_{11} value is less than –9 dB from frequency 6.2 GHz to 7.2 GHz, i.e., having the bandwidth of 1 GHz. The input impedance matching has been done for 50 Ω termination.

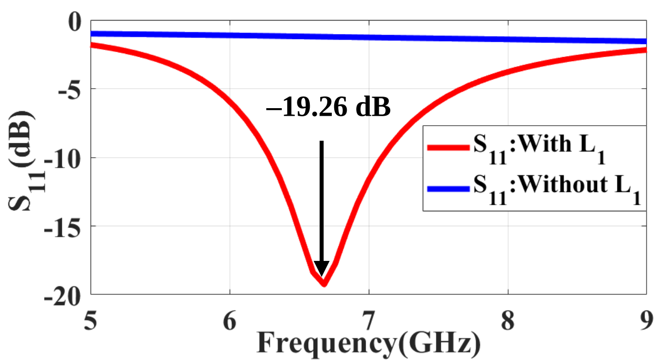

Fig. 5. Results for S_{11} with and without using L_1

Figure 6 shows the result for S_{21} including the effect of L_1. The maximum value of gain obtained is 14.35 dB at 6.44 GHz and it can be clearly shown that L_1 inductor helps in increasing the gain of realized circuit. Simulation results for NF are displayed in Fig. 7. The minimum value of NF is 4.34 dB with using the inductor L_1.

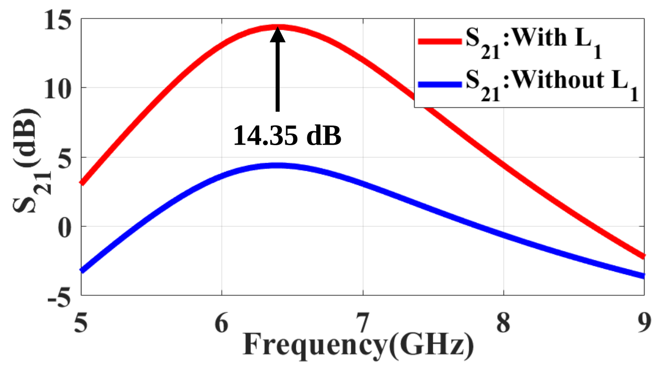

Fig. 6. Results for S_{21} with and without using L_1

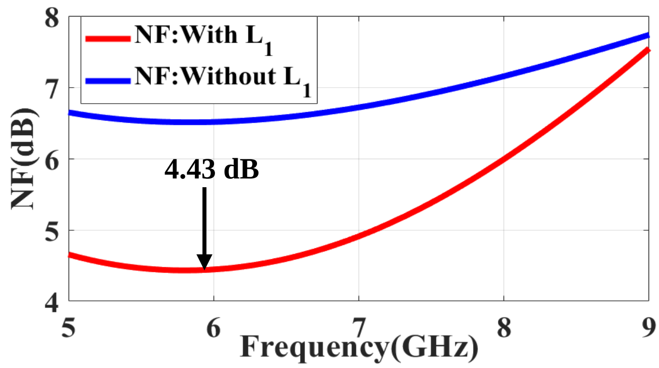

Fig. 7. Results for NF with and without using L_1

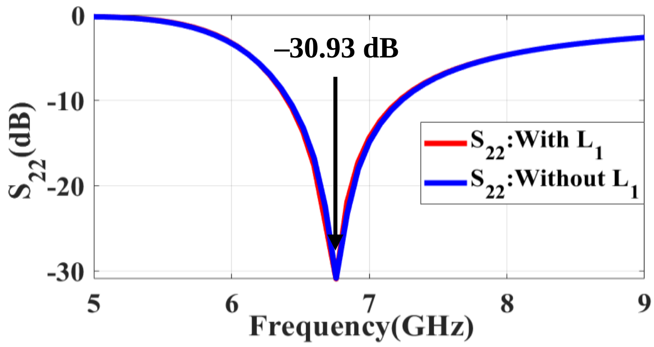

Fig. 8. Results for S_{22} with and without using L_1

One can clearly see that L_1 help in improving the parameters of realized LNA. Figure 8 is showing the value of output reflection coefficient i.e. S_{22} which is lesser than –10 dB for the frequency band of 6.4 GHz to 7.3 GHz. The layout of the realized LNA is shown in Figure 9 which is having the area of 439 µm × 373 µm, thus 0.164 mm^2.

Table 2. Comparison of realized LNA with other references

Ref.	NF (dB)	Frequency (GHz)	S_{11} (dB)	P_{DC} (mW)	Peak gain (dB)	Supply (V)	Technology (µm)
[13]	2.7-3.7	3.1-10.6	<–7.3	14.4	12.4	1.8	0.13
[14]	3.7	22-26	–16	2.78	9.2	1	0.13
[15]	3-7	2.6-10.2	–9	7.2	12.5	1.2	0.09
[16]	6.06	50-70	<–9.3	45	18.9	1.8	0.065
[17]	5.4-6.5	52-64	–19	4.4	12.5	1	0.090
This work	**4.34**	**6.2 - 7.2**	**–19.26**	**11.2**	**14.35**	**0.9**	**0.045**

Fig. 9. Layout of realized LNA

4 Conclusion

The realization of a LNA using transformer matching with active and passive g_m enhancement techniques were presented. The gain of the circuit improved by employing a cascode structure, while mutual coupling contributed in reducing the area of the realized LNA. The input and output ports were matched for 50 Ω termination. A maximum gain of 14.35 dB at 6.44 GHz and a minimum NF of 4.43 dB achieved by the realized LNA. The S_{11} value is observed to be less than –9 dB from 6.2 GHz to 7.2 GHz, providing a bandwidth of 1 GHz. The layout of the realized LNA drawn, occupied an area of 439 µm × 373 µm, which is 0.164 mm². Performance parameters were compared with those from other references, as depicted in Tab. 2.

References

[1] X. Meng and R. Zhou, "A K-Band Ultra-Compact Gm-Boost LNA Using One Multi-Coupled Transformer in 65-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 8, pp. 976-978, 2022, doi: 10.1109/LMWC.2022.3155669.

[2] Y. Zhang, Z. Wei, X. Tang, L. Zhang and F. Huang, "A 76.5–92.6 GHz CMOS LNA Using Two-Port kQ-Product Theory for Transformer Design," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 10, pp. 1187-1190, 2022, doi: 10.1109/LMWC.2022.3170929.

[3] M. Lee, X. Liu, Z. Yang, J. Jin and L. -S. Wu, "A Compact 0.2-1.6 GHz 20 MHz-Bandwidth Passive-LNA Exploiting an N-Path 1:3 Transformer," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 5, pp. 1699-1703, 2023, doi: 10.1109/TCSII.2023.3257880.

[4] J. Liu, S. Liu, Y. Gao, X. Liu and Z. Zhu, "A 28-/39-GHz Dual-Band CMOS LNA With Shunt-Series Transformer Feedback," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 1, pp. 51-54, 2023, doi: 10.1109/LMWC.2022.3201087.

[5] H. Shao, G. Qi, P. -I. Mak and R. P. Martins, "A 1.7–3.6 GHz 20 MHz-Bandwidth Channel-Selection N-Path Passive-LNA Using a Switched-Capacitor-Transformer Network Achieving 23.5 dBm OB-IIP$_3$ and 3.4–4.8 dB NF," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 413-422, 2022, doi: 10.1109/JSSC.2021.3129744.

[6] M. -H. Li, Y. Wang and H. Wang, "A 50–67-GHz Ultralow-Power LNA Using Double-Transformer-Coupling Technique and Self-Resonant Matching in 90-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 1, pp. 68-71, 2022. doi: 10.1109/LMWC.2021.3112465.

[7] J. Zhang, D. Zhao and X. You, "Analysis and Design of a CMOS LNA With Transformer-Based Integrated Notch Filter for Ku-Band Satellite Communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 1, pp. 790-800, 2022, doi: 10.1109/TMTT.2021.3126858.

[8] H. Chen, H. Zhu, L. Wu, W. Che and Q. Xue, "A Wideband CMOS LNA Using Transformer-Based Input Matching and Pole-Tuning Technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 7, pp. 3335-3347, 2021, doi: 10.1109/TMTT.2021.3074160.

[9] Y. Hu and T. Chi, "A 27–46-GHz Low-Noise Amplifier With Dual-Resonant Input Matching and a Transformer-Based Broadband Output Network," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 6, pp. 725-728, 2021, doi: 10.1109/LMWC.2021.3059592.

[10] B. Bae, E. Kim, S. Kim and J. Han, "Dual-Band CMOS Low-Noise Amplifier Employing Transformer-Based Band-Switchable Load for 5G NR FR2 Applications," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 3, pp. 319-322, 2023, doi: 10.1109/LMWC.2022.3218001.

[11] R. Wang, C. Li, J. Zhang, S. Yin, W. Zhu and Y. Wang, "A 18–44 GHz Low Noise Amplifier With Input Matching and Bandwidth Extension Techniques," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 9, pp. 1083-1086, 2022, doi:10.1109/LMWC.2022.3163462.

[12] F. Belmas, F. Hameau and J. -M. Fournier, "A Low Power Inductorless LNA With Double Gm Enhancement in 130 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1094-1103, 2012, doi: 10.1109/JSSC.2012.2185533

[13] Chang, Po-Yu, and Shawn SH Hsu. "A Compact 0.1–14 GHz Ultra-Wideband Low-Noise Amplifier in 0.13 µm CMOS." *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 10, pp. 2575-2581, 2010, doi: 10.1109/TMTT.2010.2063832

[14] Cho, Wei-Han, and Shawn SH Hsu. "An Ultra-Low-Power 24 GHz Low-Noise Amplifier Using 0.13µm CMOS Technology." *IEEE microwave and wireless components letters*, vol. 20, no. 12, pp. 681-683, 2010, doi: 10.1109/LMWC.2010.2085038.

[15] G. Sapone, G. Palmisano. "A 3–10-GHz low-power CMOS low-noise amplifier for ultra-wideband communication." *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 3, pp. 678-686, 2010, doi: 10.1109/TMTT.2010.2090357.

[16] Hsieh, Yi-Keng, et al. "A 60 GHz broadband low-noise amplifier with variable-gain control in 65 nm CMOS." *IEEE microwave and wireless components letters*, vol. 21, no.11, pp. 610-612, 2011, doi: 10.1109/LMWC.2011.2167134

[17] Chang, Po-Yu, et al. "An ultra-low-power transformer-feedback 60 GHz low-noise amplifier in 90 nm CMOS." *IEEE Microwave and Wireless Components Letters* vol. 22, no. 4, pp. 197-199, 2012, doi: 10.1109/LMWC.2012.2187883.

[18] D. He, N. Cui, J. Fan and Z. Yu, "Design of Multiple Feedback-Based Low-Noise Amplifier With Improved Broadband Simultaneous Noise and Impedance Matching Technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 2, pp. 582-586, 2024, doi: 10.1109/TCSII.2023.3309380.

[19] L. Wang and Y. J. Cheng, "A 2–20-GHz Ultrawideband High-Gain Low-Noise Amplifier with Enhanced Stability," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 4, pp. 415-418, 2024, doi: 10.1109/LMWT.2024.3351279.

[20] X. Zhang, K. Wang, Y. Yan and X. Liang, "A Compact 6–24-GHz Current-Reuse LNA With Bandwidth and Noise Enhancement," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 2, pp. 203-206, 2024, doi: 10.1109/LMWT.2023.3341145.

Received 7 January 2025