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New full-wave/half-wave rectifier with electronic control

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This research article introduces an innovative full-wave rectifier design centered around the Voltage Differencing Transconductance Amplifier (VDTA) as its foundational core, thereby eradicating the necessity for passive components. The proposed circuit demonstrates high linearity and good zero-crossing performances. The rectified output signal can be adjusted by controlling the bias currents. Its simple and compact design makes it well-suited for integration into IC circuits, especially for low-voltage, high-frequency applications. A detailed analysis of the proposed rectifier includes evaluating non-ideal effects and parasitic influences. By eliminating passive components, the circuit minimizes parasitic effects. Its robustness is evaluated through detailed simulations using 0.18 μm CMOS technology and a ±0.8 V power supply, showing strong agreement with theoretical predictions. Additional reliability insights are obtained via Monte Carlo simulations and corner analysis. To verify the rectifier's feasibility, practical experiments with off-the-shelf components confirm its functionality and efficiency. The circuit layout is implemented in Cadence Virtuoso, occupying a chip area of 2726 μm^2.

Keywords: full-wave rectifier, VDTA, transconductance mode, electronically tunable, non-ideality and parasitic effects analysis, simulation, layout, experiment

1 Introduction

Rectification is a key process for modifying voltage and current signals, widely used in instrumentation, measurement, communication circuits, and nonlinear analog signal processing. It is essential for designing devices such as peak detectors, ammeters, AC voltmeters, signal conditioners, wattmeters, RF demodulators, function generators, polarity detectors, and averaging circuits [1, 2]. Due to the diverse applications requiring high-performance rectifiers, there is a continuous need for precise and adaptable designs. Consequently, the exploration and advancement of such circuits have emerged as a pivotal and contemporary area of focus within the realm of analog signal processing implementation.

Over the past two decades, researchers in the domain of analog signal processing have proposed a multitude of rectifier designs utilizing various active components [3-35] and operating modes for both voltage and current. The primary objective of these studies is to overcome the limitations of traditional diode-based rectifiers, particularly the diode threshold voltage, as well as rectifiers based on operational amplifiers (OAs). OA-based full-wave rectifiers effectively rectify low-amplitude signals and avoid threshold issues but are limited in frequency range due to constraints in slew rate and bandwidth. These deficiencies engender distortion in the output signal arising from the constrained slew rate. Furthermore, rectifiers built on OAs do not adequately tackle the threshold voltage issue owing to the modest signal transients. To overcome these limitations, researchers have developed current-processing circuits that enable operation with small signal amplitudes over a wide frequency range while allowing electronic control of the transfer function.

In reference [3], a rectifier circuit is realized utilizing two current conveyors (CCII) and four diodes. However, this configuration lacks a low output impedance. Conversely, the rectifier proposed in reference [4] employs two second-generation current conveyors (CCII), a PMOS transistor, a voltage follower (VF), and two floating/grounded resistors. Nevertheless, it falls short in providing high input impedance. Similar impedance limitations in both input and output are observed in the circuits presented in reference [5], which involve a negative-type CCII, two diodes, and a floating/grounded resistor. To meet the requisite criteria for input and output impedances, the design put forth in reference [6] incorporates a CCII, an additional 28 MOS transistors, and a grounded resistor. However, it lacks the capacity to adjust the output signal's value. Similar attributes are evident in the rectifiers discussed in references [7], employing two differential voltage current conveyors (DVCC), and in reference [8], relying on two current feedback operational amplifiers (CFOA). Despite several recent articles [9-11] addressing rectifier designs, they lack tunability features.

Reference [9] introduces a versatile full-wave rectifier circuit, utilizing voltage conveyors (VCs) as active components, enabling operation in voltage/current modes with adjustable input and output signals. A dual-output second-generation current conveyor (DO-CCII) is employed in the rectifier circuit presented in reference [10]. References [12, 13]

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introduce current-mode precision rectifier designs using EXCCII and additional n-MOS transistors. Similarly, a full-wave rectifier circuit is realized in reference [14] employing DDCC (differential difference current conveyor) alongside three passive resistors. Reference [15] describes a rectifier utilizing DVCC (differential voltage current conveyor), two OTA (operational transconductance amplifier) units, a diode, and multiple grounded resistors. A full-wave rectifier [16, 17] employing CCCII (second-generation current-controlled conveyor) offers a wide bandwidth, substantial dynamic range, high slew rate, and low power consumption. However, experimental validation of the circuit is not provided. The rectifier outlined in reference [18] consists of an OTRA (operational transresistance amplifier) block with multiple passive floating resistors. Another current-mode rectifier [19] is crafted using a PMOS and NMOS-based Low Voltage Cascode Current Mirror (LVCCM). Reference [20] introduces a new second-generation voltage conveyor (VCII) centered on a half-wave rectifier circuit architecture, capable of generating inverting and non-inverting outputs as voltage signals. This conveyor comprises a single VCII, two diodes, and a grounded resistor. A precision half/full-wave rectifier, based on a differential voltage current conveyor transconductance amplifier (DVCCTA) and five NMOS transistors, is described in reference [21]. The proposed design finds particular suitability for low voltage and high-frequency input signals. The design proposed in [22] features a single dual-X second-generation current conveyor (DXCCII), three MOS switches, and two resistors. An efficient full-wave rectifier with high precision, operating in current mode, is introduced in [23]. This structure is simple and compact, utilizing only a single current follower differential input transconductance amplifier (CFDITA) and two MOS transistors. A straightforward voltage-mode full-wave rectifier circuit is presented in [24]. The proposed circuit can be realized using a voltage follower (VF), a current follower (CF), two diodes, and two resistors. Alternatively, the circuit can also be implemented using one second-generation voltage conveyor (VCII), two diodes, and two resistors.

Upon reviewing solutions published over the last decade, it becomes evident that these proposed solutions possess certain shortcomings, such as increased voltage demand [6, 18, 26, 31], reliance on diodes [3, 5, 7-9, 15, 20, 24, 29, 35], reliance on numerous passive elements [3, 4, 14, 15, 18, 29], dependence on an external switch [11, 13, 22, 23, 33], and the absence of output adjustability [3-15, 20, 22-24, 29].

This paper presents a novel precision full-wave rectifier design utilizing two Voltage Differencing Transconductance Amplifiers (VDTAs). In contrast, for the half-wave rectifier, a solitary VDTA suffices, obviating the necessity for passive elements or diodes, while operating in the transconductance mode. Notably, the bias currents governing the VDTAs introduce the capability for electronic modulation of the output currents, providing an external control parameter without affecting other design variables. The use of VDTAs offers several advantages, including a reduced transistor count, a simple and symmetrical design, easy control, and excellent input-output impedance properties in transconductance mode. The circuit exhibits high input impedance, minimizing loading effects. It operates over a wide frequency range of up to 50 MHz, as confirmed by simulations and post-layout results. The design offers excellent DC transfer characteristics with accurate zero-crossing and minimal deviations across its operating range. Notably, it eliminates the need for specialized bias sources, avoiding body effects in all transistors. Additionally, due to the compact VDTA-based structure, component matching is unnecessary. Post-layout simulations and experimental results using standard off-the-shelf components validate consistency with theoretical and simulated predictions.

Compared to existing literature, the proposed rectifier circuit is a novel design based on the intrinsic architecture of VDTA. For instance, the rectifier outlined in [25] draws upon the Modified Voltage Differencing Transconductance Amplifier (MVDTA), constituted by two independent OTA stages and supplementary MOS transistors operating in a diode configuration. In contrast, the proposed circuit features a simpler, more compact design, enabling better pairing and electronic control of the rectifier's transfer functions. This results in lower distortion, similar output noise, and improved DC transfer.

2 Proposed configuration of rectifier circuits

The layout of the proposed full-wave rectifier is shown in Fig. 1. As evident in the diagram, the circuit yields two separate outputs: i_{out+} corresponds to the direct output from the transconductance mode full-wave rectifier, while i_{out-} signifies the inverting output.

The circuit utilizes the VDTA as its active component, initially introduced in 2008 [36]. The connections between current and voltage at the various ports of the VDTA are explained by Eqn. (1).

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} \beta_F g_{mF} & -\beta_F g_{mF} & 0 \\ 0 & 0 & \beta_S g_{mS} \\ 0 & 0 & -\beta_S g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \tag{1}$$

The transconductance gains are essential to its functionality, referred to as g_{mF} and g_{mS}, of the VDTA. The VDTA is structured with two interconnected

transconductance gain stages, as visually presented in Fig. 2. The parameters β_F and β_S signify the characterized tracking errors attributed to the first and second stages of the VDTA, respectively. These tracking errors, encompassing deviations from the ideal transconductance gains. They typically range from 0.9 to 1, with 1 being the ideal value. Notably, these tracking factors remain consistent and independent of frequency within the low to medium frequency ranges. The transconductance gains of the VDTA can be electronically adjusted by changing the applied biasing currents (or voltages). The integration of the VDTA is accomplished through CMOS transistors, as depicted in Fig. 2, employing the configuration delineated in [37]. By modulating the currents I_{BF} and I_{BS}, the transconductance gains g_{mF} and g_{mS} of the VDTA can be dynamically tailored.

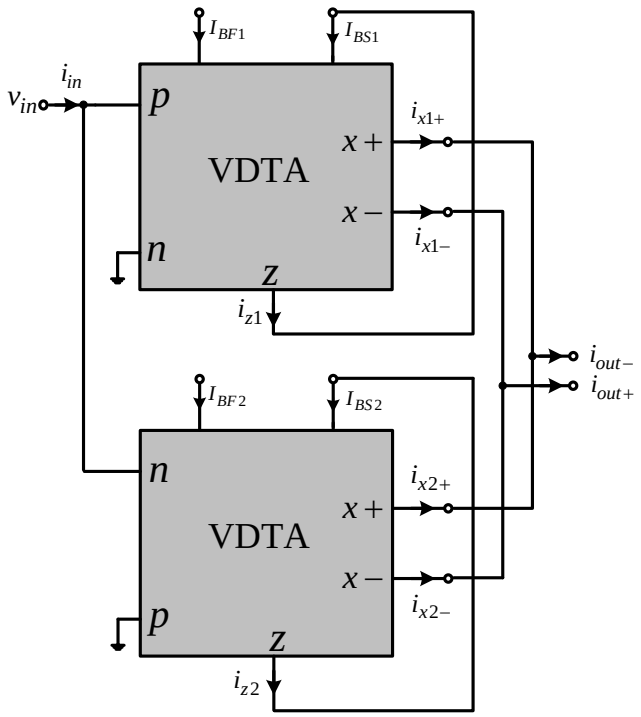


Fig. 1. Proposed full-wave (half-wave/inverting) rectifier

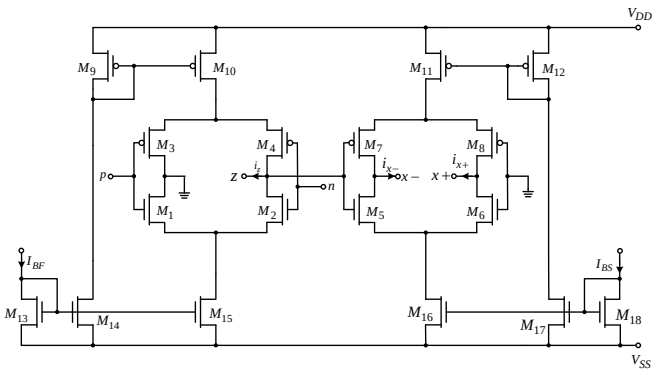


Fig. 2. CMOS transistor -implementation of VDTA

The arrangement of the VDTA is depicted in Fig. 2, featuring a composition of two Arbel-Goldminz transconductances [38]. The transconductance magnitudes, g_{mF} and g_{mS}, corresponding to the individual stages, are under the influence of the transconductance stemming from the output transistors. These can be dynamically fine-tuned through the currents I_{BF} and I_{BS}. The estimated formulations for these transconductance values are deduced in [38] as follows:

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1+g_2}\right)+\left(\frac{g_3 g_4}{g_3+g_4}\right); g_{mS} \cong \left(\frac{g_5 g_6}{g_5+g_6}\right)+\left(\frac{g_7 g_8}{g_7+g_8}\right) \quad (2)$$
$$g_i = \sqrt{\mu_i C_{ox} W_i I_{BF}\left(I_{BS}\right)/L_i}, i = 1,...8$$

where μ signifies the effective carrier mobility, C_{ox} denotes the gate-oxide capacitance per unit area, and W and L represent the effective channel width and length of the i-th MOS transistor, respectively.

In Fig. 1, the voltage at the z port depends on the voltage drop across the total resistance, which includes the output impedance of the z port and the output resistance of the I_{BS} (bias current) input. Precisely, the MOS transistor M_{18}, situated within the diode junction, effectively governs this potential. The output impedance of the z port is formed by the parallel combination of parasitic resistances R_z and capacitances C_z. In an ideal VDTA setting, the parasitic resistance is effectively infinite, while the parasitic capacitance approaches near-zero levels. Moreover, the output resistance of the bias input equals $1/g_{m18} \,||\, r_{ds18} \approx 1/g_{m18}$, seamlessly connected in parallel with the aforementioned impedances. This bias input port is fashioned through a current mirror employing transistors M_{17} and M_{18}, yielding a low impedance characteristic. Consequently, the potential at the z port finds expression as follows:

$$v_z = \beta_F g_{mF} v_{in} R_z \left\| \frac{1}{sC_z} \right\| \frac{1}{g_{m18}} \approx \beta_F \frac{g_{mF}}{g_{m18}} v_{in} \quad (3)$$

By interconnecting port z with the control port I_{BS}, as illustrated in Fig. 1, an adjustment in the quiescent operating point becomes apparent. This operating point corresponds to the voltage level that port z assumes. Consequently, it becomes imperative to modulate the VDTA's supply voltage, aiming for a symmetrical and distortion-free voltage signal that can aptly drive the second OTA stage of the VDTA. This adjustment must also guarantee the desired operational mode for all MOS transistors present in the circuit. The proposed circuit layout facilitates the shifting of the quiescent operating point of port z towards negative values. The magnitude of this shift is directly impacted by the supply voltage as well as the characteristics intrinsic to the MOS transistor itself, with special focus on the technology employed for circuit realization. Ensuring the proper functioning of transistor M_{18} necessitates its operation in the saturation

region. Achieving this requires careful considerations, including controlling the supply voltage, carefully choosing transistor parameters, and optimizing the circuit's practical implementation. Thus, the voltage at the z port for the rectifier in Fig. 1 can be defined as follows:

$$\begin{aligned} &v_{GS18} = v_{z1} - V_{SS} \geq v_{Tn} \\ &v_{z1} \geq V_{SS} + v_{Tn} \Rightarrow \beta_F \frac{g_{mF}}{g_{m18}} v_{in} \geq V_{SS} + v_{Tn} \end{aligned} \tag{4}$$

By meeting the above criteria, transistor M_{18} is activated only during the positive half-cycle of the input voltage signal. This particular biasing arrangement stands as a pivotal factor in achieving the intended operation of the second OTA stage within the VDTA. Its role is crucial in minimizing distortions in the output rectified signal, thereby reducing the overall total harmonic distortion (THD) of the rectifier circuit. This specific arrangement guarantees precise rectification of the input voltage signal at the points of zero-crossing, thereby enabling the proposed circuit to operate effectively across an extensive frequency span. Moreover, the absence of a diode within the rectifier's design permits accurate manipulation of low-amplitude sine wave voltage signals, even when they fall below the threshold voltage characteristic of traditional diodes. In contrast, diode-based rectifiers often suffer from zero-crossing distortion in the output signal due to the inherent properties of the diodes.

Drawing upon the functional relationships delineated in Eqn. (1), it becomes evident that:

$$i_{x1-} = -i_{x1+} = \begin{cases} \beta_{F1}\beta_{S1} \dfrac{g_{mF1} g_{mS1}}{g_{m18}} v_{in}; v_{in} \geq 0 \\ 0; v_{in} < 0 \end{cases} \tag{5}$$

and that it is analogous to:

$$i_{x2-} = -i_{x2+} = \begin{cases} 0; v_{in} \geq 0 \\ \beta_{F2}\beta_{S2} \dfrac{g_{mF2} g_{mS2}}{g_{m18}} v_{in}; v_{in} < 0 \end{cases} \tag{6}$$

Consequently, the current at the output of the presented full-wave rectifier can be expressed as:

$$\begin{aligned} i_{out+} &= -i_{out-} = \frac{1}{g_{m18}} \left(\beta_{F1}\beta_{S1} g_{mF1} g_{mS1} + \beta_{F2}\beta_{S2} g_{mF2} g_{mS2} \right) |v_{in}| \\ &= \beta_F \beta_S \frac{g_{mF} g_{mS}}{g_{m18}} |v_{in}| \end{aligned} \tag{7}$$

The ultimate derived relationship is established assuming matched characteristics between the two employed VDTAs in the arrangement. According to this equation, the current i_{out+} represents a rectified version of the input voltage, amplified by the transconductance of both VDTA stages (g_{mF} and g_{mS}) and the output resistance from the second bias port. Conversely, the output current i_{out-} corresponds to the outcome of the inverting full-wave rectifier, sourced from the *x*- port that functions as an inverting full-wave rectification mechanism. Furthermore, it can be inferred that either the output of the first or second VDTA can serve as a half-wave rectifier. In this scenario, the proposed rectification setup necessitates only one active block for its implementation – namely, the VDTA.

Upon connecting a resistive load to the configuration's output, a voltage-mode rectifier configuration is achieved. It is worth noting, however, that due to the high-impedance characteristics of the VDTA's output ports, the load should not exceed 10 kΩ to prevent substantial distortion in the output current signal. When incorporating a resistance at the input, it is advisable to employ a value no lower than 1 kΩ to ensure effective processing of input current signals. Additionally, the amplitude of the output current or voltage signal can be manipulated by adjusting the magnitudes of the currents I_{BF}, thereby allowing the input signal to directly influence the transconductance gain of the second OTA stage within the active VDTA circuit.

2.1 Non-ideal and parasitic analysis

As discussed earlier, the VDTA exhibits deviations from ideal gains due to inherent tracking errors in real-world scenarios. With reference to the above-mentioned Eqn. (7), it can be inferred that the proposed full-wave rectifier illustrates sensitivity values that are either equivalent to or lower than unity in magnitude. This indicates low passive and active sensitivities in the circuit.

Furthermore, it is crucial to acknowledge that the transconductance of the OTA cell within the VDTA is a parameter subject to frequency dependence. This particular attribute assumes a significant role in establishing the circuit's bandwidth limitations, which can be effectively characterized through a single pole model. The transconductance gains of the VDTA can be expressed as follows:

$$g_{mF} = g_{mF0} \frac{\omega_F}{(s + \omega_F)}; \quad g_{mS} = g_{mS0} \frac{\omega_S}{(s + \omega_S)} \tag{8}$$

The transconductance gain factors of the OTA cells at zero frequency are denoted as g_{mF0} and g_{mS0}, while $\omega_F = 1/\tau_F$ and $\omega_S = 1/\tau_S$ r represent their respective pole

frequencies, where τ_F and τ_S denote the associated time delays. Substituting these parameter values into Eqn. (7) provides a deeper comprehension of the frequency characteristics of the implemented rectifier and their susceptibility to non-ideal effects. It becomes evident that the effective operational frequency range of the full-wave rectifier proposed in Fig. 1 is defined as $\omega << \min(\omega_F, \omega_S)$. The exact values of these pole frequencies in Eqn. (8) depend on the specific implementation of the VDTA. To increase the bandwidth of the VDTA, a compensation resistor R, a voltage buffer, and an additional set of MOS transistors can be introduced, as recommended in [39]. This adaptation influences the transconductance gain, denoted as $g_{mF}=g_{m0}/(1+g_{mF0}R)$, which consequently impacts the bandwidth of the OTA cells due to its dependency on g_{mF}. In the proposed design, this particular modification was not adopted, as the intention was to employ the simplest feasible VDTA configuration involving a minimal number of transistors.

Parallel to their respective terminals (p, n, z, $x+$ and $x-$), parasitic resistances R_p, R_n, R_z, R_{x+} and R_{x-} and parasitic capacitances C_p, C_n, C_z, C_{x+} and C_x [25] exist. In an ideal VDTA setup, these parasitic resistances would practically approach infinity, while the parasitic capacitances would virtually reach zero [25]. Given the specific layout of the proposed circuit, the influence of parasitic impedances is reduced to a minimum. Consequently, only the impedance at the z port necessitates consideration when assessing the transfer function of the full-wave rectifier. This leads us to an examination of the operation of the proposed rectifier within a high-frequency environment. In summary, it can be concluded that:

$$\begin{aligned} i_{out+} &= -i_{out-} = \beta_F \beta_S g_{mF} g_{mS} \frac{1}{g_{m18}} \left\| R_z \right\| \frac{1}{sC_z} |v_{in}| \\ i_{out+} &= -i_{out-} = \beta_F \beta_S g_{mF} g_{mS} \frac{R_z}{1+g_{m18}R_z + sR_zC_z} |v_{in}| \end{aligned} \tag{9}$$

Ensuring the accurate functioning of the presented full-wave rectifier [8] necessitates the fulfillment of the subsequent conditions, as inferred from the established Eqn. (9):

$$\omega \frac{R_zC_z}{1+g_{m18}R_z} << 1 \tag{10}$$

The practical frequency range can be ascertained by assessing the maximum operating frequency f, which is considered as one-tenth of the angular frequency ω, where ω is calculated as $\omega=2\pi f$.

$$f \le \frac{0.1}{2\pi}\left(\frac{R_zC_z}{1+g_{m18}R_z}\right) \tag{11}$$

The impact of parasitic elements in the proposed full-wave rectifier circuit affects the output current, particularly at elevated frequencies, as highlighted in Eqn. (9). However, by carefully selecting the parameters of the MOS transistors, it is possible to reduce these effects and minimize their impact on the overall circuit performance.

2.2 Temperature sensitivity

The temperature sensitivity of the proposed rectifier (VDTA) is primarily determined by the temperature-dependent characteristics of its transconductance parameters g_{mF}, g_{mS}, and g_{18}.

The mobility of charge carriers in semiconductors (electrons and holes) decreases as temperature increases. This phenomenon can be described by the following relationship:

$$\mu(T) = \mu_0 \left(\frac{T_0}{T}\right)^{\alpha} \tag{12}$$

where μ_0 is the mobility at a reference temperature T_0, and α is a temperature exponent (typically 2.4 for electrons and 2.2 for holes). The carrier mobility in MOSFETs decreases with increasing temperature. This decrease in mobility directly reduces the transconductance, Eqn. (2). The threshold voltage V_T of MOSFETs generally decreases with increasing temperature. This decrease can partially counteract the effect of reduced mobility by increasing the drain current and on this way increasing the Arbel-Goldminz transconductances. The threshold voltage changes approximately linearly with temperature:

$$V_T(T) = V_{T0} - k(T - T_0) \tag{13}$$

where V_{T0} is the threshold voltage at the reference temperature and k is a temperature coefficient. In 180nm CMOS technology, the typical temperature coefficients k for the threshold voltage are approximately –2 to –3 mV/°C for NMOS and –1 to –2 mV/°C for PMOS.

The transconductance g_{m18} can be expressed incorporating its temperature dependency as follows:

$$g_{m18} = \sqrt{2\mu_{0n}\left(\frac{T_0}{T}\right)^{\alpha_n} C_{ox} W_{18}/L_{18}\, i_{D18}}\,; i_{D18} = i_z = g_{mF} v_{in} \tag{14}$$

where i_{D18} is the drain current of transistor M_{18} operating in saturation region. Since transistors M_1, M_2, M_5, and M_6 (similarly to M_3, M_4, M_7, and M_8) are matched in terms of their parameters (having identical effective channel width and length W and L), the transconductance values, according to Eqn. (2), simplify to:

$$g_{mF} \cong \left(\frac{g_1+g_3}{2}\right); g_{mS} \cong \left(\frac{g_5+g_7}{2}\right) \tag{15}$$

The bias current setting the parameter g_{mF} is I_{BF}, and g_{mS} is determined by the current at the z port. Considering the previously mentioned facts and relationships (14) and (15), Eqn. (7) simplifies to (incorporating temperature-dependent parameters):

$$\begin{aligned} i_{out+} &= -i_{out-} = \beta_F \beta_S \frac{g_{mF} g_{mS}}{g_{m18}} |v_{in}| \\ &= \beta_F \beta_S \frac{\frac{1}{4}\left(\sqrt{\mu_{0n}\left(\frac{T_0}{T}\right)^{\alpha_n} C_{ox} W_1/L_1} + \sqrt{\mu_{0p}\left(\frac{T_0}{T}\right)^{\alpha_p} C_{ox} W_3/L_3}\right)^2 \sqrt{I_{BF} i_z}}{\sqrt{2\mu_{0n}\left(\frac{T_0}{T}\right)^{\alpha_n} C_{ox} W_{18}/L_{18}\, i_z}} |v_{in}| \\ &= \beta_F \beta_S \frac{\frac{1}{4}\left(\sqrt{\mu_{0n}\left(\frac{T_0}{T}\right)^{\alpha_n} C_{ox} W_1/L_1} + \sqrt{\mu_{0p}\left(\frac{T_0}{T}\right)^{\alpha_p} C_{ox} W_3/L_3}\right)^2 \sqrt{I_{BF}}}{\sqrt{2\mu_{0n}\left(\frac{T_0}{T}\right)^{\alpha_n} C_{ox} W_{18}/L_{18}}} |v_{in}| \end{aligned} \tag{16}$$

The above equation illustrates that the temperature-induced changes in the numerator are partially offset by those in the denominator, assuming a stable current source I_{BS}. During simulation, such a bias current is typically employed, while practical implementations may adopt the VDTA design proposed in [40], which incorporates Proportional to Absolute Temperature (PTAT) current sources to counteract mobility degradation effects. It can be concluded that the transconductance of the Arbel-Goldminz cell decreases with rising temperature primarily due to reduced carrier mobility, despite the compensatory effect of decreasing threshold voltage. Designing for temperature stability involves employing techniques such as temperature-compensated biasing and circuit adjustments to mitigate temperature-related variations in transconductances g_{mF} and g_{mS}. A true evaluation of the temperature sensitivity of the designed full-wave rectifier will emerge after simulation validation. Furthermore, relation (16) reaffirms the rectification function of the designed circuit.

3 Simulation and experimental results

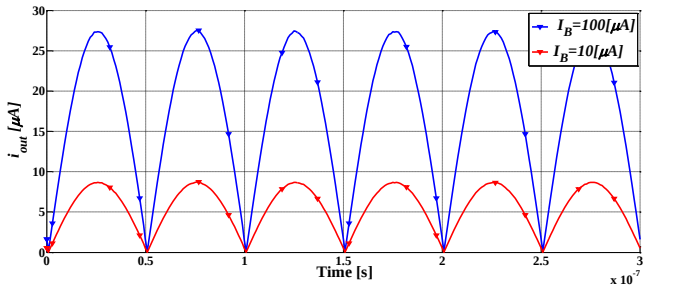
To evaluate the performance of the full-wave rectifier circuits shown in Fig. 1, validation was conducted through simulation in the HSPICE environment, utilizing the TSMC 0.18 μm CMOS process parameters at level 49. The aspect ratios of the MOS transistors shown in Fig. 2 were chosen in alignment with the recommendations provided in [25]. The power supply was set to ±0.8 V to extend the operational frequency range and reduce distortion in the output rectified signal, as previously discussed. The simulated circuits exhibited a maximum power consumption of 0.63 mW.

Table 1 presents the values for g_{mF}, g_{mS}, and g_{18} corresponding to different bias currents I_{BF}. In the proposed rectifier design, I_{BS} represents the current at the z port from the first stage of the VDTA, which varies over time based on the dynamics of the input voltage signal. Consequently, these parameter values are established under the condition of a constant input voltage signal v_i=V_I=const=100 mV.

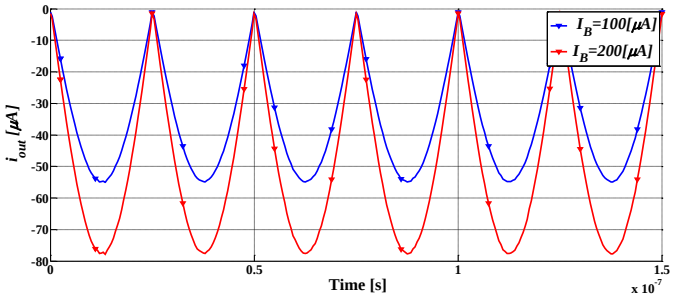
Table 1. Values of the transconductance parameters g_{mF}, g_{mS}, and g_{18} for different bias currents I_{BF}

I_{BF} (μA)	10	40	100	160	200
g_{mF} (μA/V)	210	422	664.5	838	939.74
g_{mS} (μA/V)	304.51	431.67	541.68	608.3	644.17
g_{18} (μA/V)	729.98	1040.94	1299.91	1455.2	1545.84

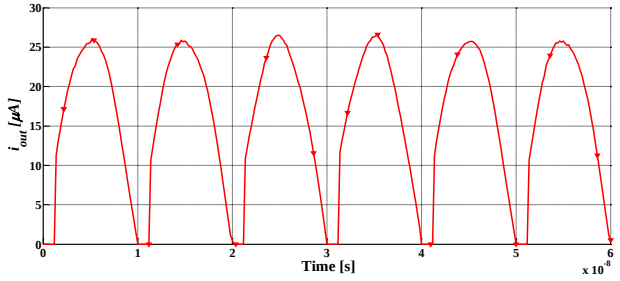
The transient response of the proposed full-wave rectifier circuit is outlined in Fig. 3, incorporating various magnitudes and frequencies of the input voltage signal. In Fig. 3(b), the operational behavior of the proposed arrangement in the inverting mode is depicted, with the output current originating from the i_{x+} ports of the VDTA. Demonstrating the circuit's adjustability, the manipulation of the biasing current I_{BF} showcased the circuit's tunable nature. Simulation results show a slight delay at 20 MHz due to internal parasitic components in the VDTA. Figure 3(c) displays the output rectified current waveform at 50 MHz, where noticeable distortion is present. The distortion at the zero-crossing points, caused by the maximum slew rate of the VDTA's output current, defines the upper frequency limit of the proposed rectifiers.



(a)



(b)



(c)

Fig. 3. (a) Transient response at frequency f=10 MHz and input amplitude of 100 mV, (b) Transient response in inverting mode at frequency f=20 MHz and input amplitude of 200 mV, (c) Transient response in direct mode of operation at maximum operating frequency of 50 MHz (V_m=100 mV, I_{BF1}=I_{BF2}=100 μA).

Moving on to Fig. 4, it provides insight into the DC transfer characteristics of the proposed full-wave rectifier circuit at an operating frequency of 10 MHz, considering I_{BF1}=I_{BF2}=40 μA. The attained peak value of the input voltage signal approximates 300 mV, with marginal distortion evident at an input voltage signal amplitude of 280 mV. In the least favorable scenario, an offset of 0.38 μA is observed at the zero-crossing point. These findings indicate that the proposed rectifier exhibits remarkable linearity, coupled with minimal distortion occurring at the zero-crossing point [25, 26]. The most significant relative discrepancy relative to the ideal characteristics is noted as 1.5% within the corner regions of the transfer characteristics.

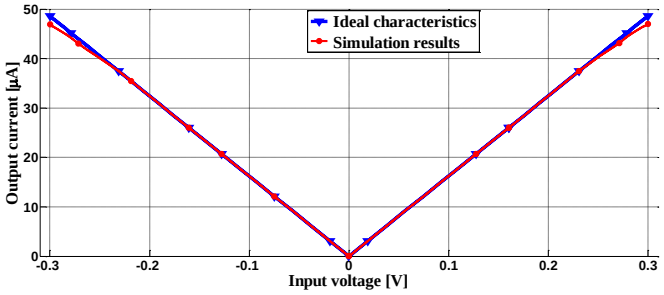
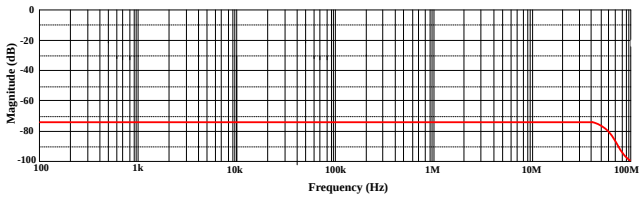
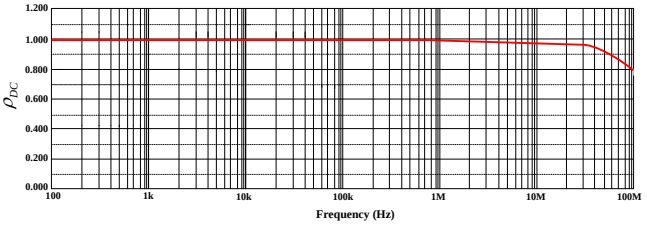


Fig. 4. DC transconductance transfer characteristics

In Fig. 5(a), the AC transfer characteristics of the full-wave rectifier illustrated in Fig. 1 are showcased, maintaining the same input voltage signal and bias current values as employed in the DC analysis illustrated in Fig. 4. The delineated characteristics distinctly exhibit the rectifier's commendable operation, extending proficiently up to a frequency of 50 MHz, and displaying a favorable degree of linearity [9, 25]. A pivotal metric for evaluating rectifier efficacy is the DC Value transfer ρ_{DC} [9, 28], which evaluates the purity of the rectified output signal by contrasting simulated DC values against ideal DC values in relation to magnitude and frequency, see Fig. 5(b). An ideal outcome for this ratio is unity.



(a)



(b)

Fig. 5. (a) AC transfer characteristics, (b) DC transfer ratio versus frequency with various magnitudes for I_{DCsim}/I_{DCth} (V_m=200 mV, I_{BF1}=I_{BF2}=40 μA).

As evidenced in Fig. 5(b), the simulation outcomes of ρ_{DC} across frequencies ranging from 1 to 100 MHz indicate that as the frequency escalates and the input voltage signal's magnitude diminishes, the divergence from the ideal attributes intensifies, leading to a reduction in ρ_{DC} below unity. However, the ρ_{DC} values continue to closely align with the ideal unity, affirming the precision of the rectifier's performance [25]. The total harmonic distortion (THD) of the proposed circuit measures at –11.8 dB at 50 Hz, and –20.2 dB at 50 MHz, while considering an input signal magnitude of 300 mV.

Figure 6 illustrates the transient temperature analysis, portraying the behavior of the proposed configuration (with I_{BF}=I_{BS}=100 μA) while the temperature ranges from 25 °C to 75 °C in increments of 25 °C. This analysis serves to exemplify the design's resilience. The observation reveals that the response manifests only a marginal departure, featuring a slight alteration in the amplitude of the rectified signal, as it encounters varying temperatures. The simulations conducted under these conditions employed an input voltage signal at a frequency of 10 MHz.

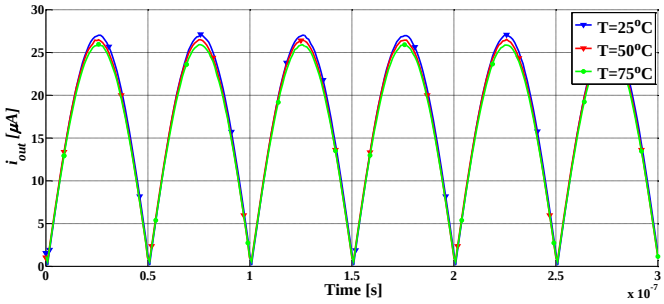
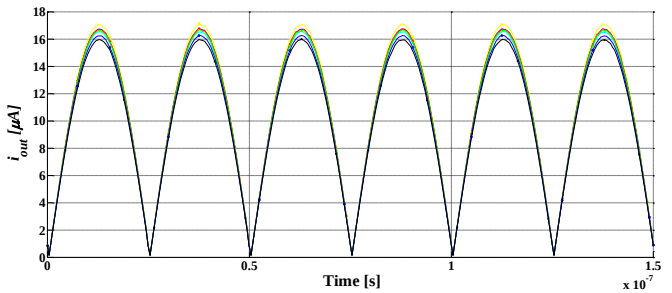
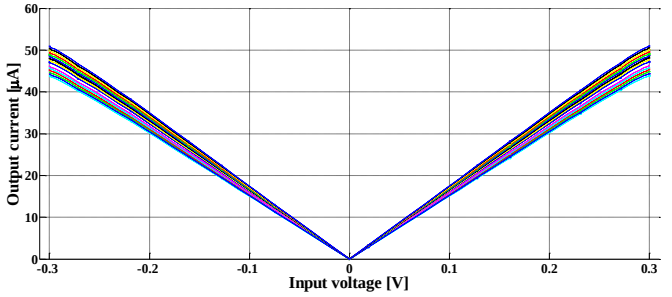


Fig. 6. Temperature analysis of the proposed rectifier circuit-response in different temperature conditions for the 100 mV input voltage signal amplitude.

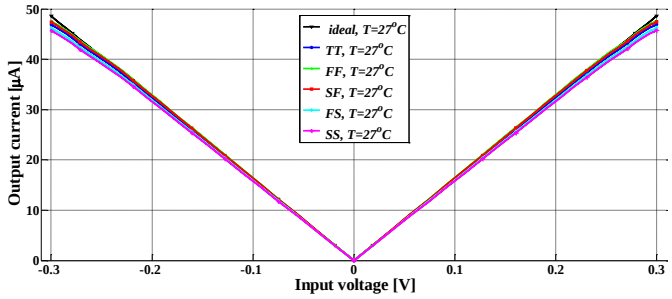
The Monte Carlo (MCS) analysis emerges as a valuable instrument for investigating and evaluating the robustness and uncertainty intrinsic to the proposed full-wave rectifier circuit, factoring in the mismatch in transistors within the designed circuit [21]. This analysis involves subjecting an input voltage signal with an amplitude of 100 mV and a frequency of 20 MHz (alongside I_{BF1}=I_{BF2}=40 μA) to a Monte Carlo simulation performed 200 times. This simulation accounts for a Gaussian deviation of 5% in gate oxide thickness t_{ox}, width, and length parameters across all MOS transistors, as well as a 10% Gaussian deviation in V_{TH0} (threshold voltage). The outcomes of the simulation are visualized in Fig. 7(a), while the DC Monte Carlo analysis is depicted in Fig. 7(b). The results obtained indicate that the rectifier circuit preserves its functionality within acceptable bounds, even in the presence of a minor deviation observed in the output response [25]. Figure 7(c) presents the corners analysis encompassing variations such as Typical NMOS Typical PMOS (TT), Fast NMOS Fast PMOS (FF), Slow NMOS Slow PMOS (SS), Fast NMOS Slow PMOS (FS), and Slow NMOS Fast PMOS (SF). Across this spectrum of process corner variations, the proposed rectifier circuit demonstrates commendable operational performance, spanning a diverse design space. This showcases its ability to excel across a broad range of temperature conditions and diverse environmental scenarios.



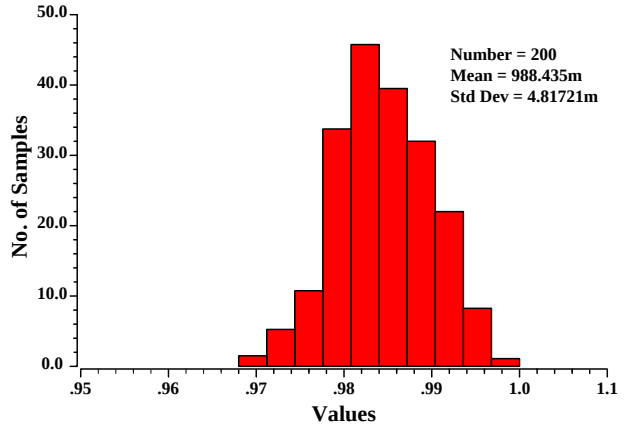
(a)



(b)



(c)



(d)

Fig. 7. Monte Carlo analysis of the presented rectifier circuit: (a) Time response, (b) Input-output DC characteristics, (c) Process corner analysis, (d) Histogram of the ρ_{DC} based on Monte Carlo analysis for 200 runs.

In Fig. 7(d), the histogram showcases the distribution of ρ_{DC} obtained through the Monte Carlo process/mismatch analysis involving 200 runs, with an input voltage set at 200 mV/20 MHz. The mean value of ρ_{DC} stands at 984.435 m, accompanied by a standard deviation of approximately 4.81721 m, underscoring the circuit's tolerable sensitivity to disparities among

transistors. It is worth noting that, based on simulation findings [27], the proposed rectifiers exhibit favorable noise characteristics, yielding an equivalent output noise of 11.2 nA/√Hz at the operational frequency of 50 MHz.

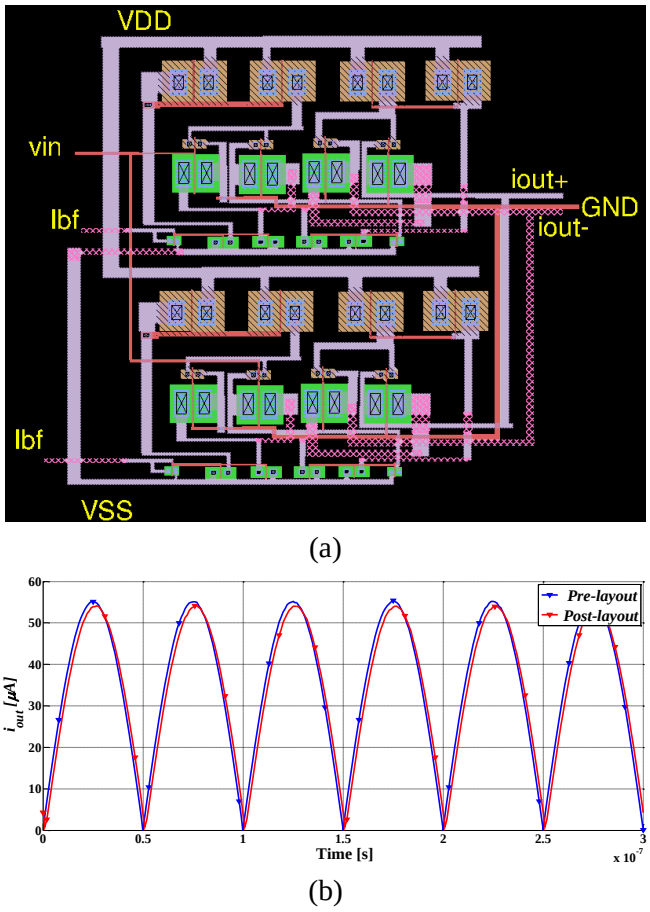


Fig. 8 (a) Layout of the full-wave rectifier proposed in Fig. 1(b). Transient response of pre- and post-layout simulation at 10 MHz, V_m=200 mV, I_{BF1} = I_{BF2} = 100 μA.

Transitioning to the layout dimension, Fig. 8(a) presents the layout depiction of the proposed full-wave rectifier circuit, spanning an aggregate area of 2726 μm² (58 μm × 47 μm). In order to gauge the impact of parasitic elements on the overall performance, a post-layout simulation was conducted, as depicted in Fig. 8(b). An observable marginal variation in the transient response emerges between the pre-layout and post-layout simulations, underscoring the influence of parasitics within the design. Notable delays arise in the obtained outcomes due to the presence of parasitic impedances and consequential interconnection resistances, further accentuating the distinction between pre-layout and post-layout results.

3.1 Experimental results

To verify the functionality of the proposed circuit, an experimental validation was conducted using readily available components, as shown in Fig. 9(a). Due to the lack of a commercially available monolithic VDTA IC, MAX435 ICs from Maxim Integrated [25] were used. The DC power supply was set to ±5 V. Measurements were taken using a TDS20114 oscilloscope, capturing 3000 samples, which were then imported into MATLAB for plotting without modifications [25]. Figure 9(b) presents the experimental results using an input voltage of 500 mV amplitude and 500 kHz frequency. The output waveform shows a slight offset due to tracking errors, parasitic effects, and transistor mismatches. The prototype has a frequency limitation, with a bandwidth of about 1 MHz. This constraint is due to the commercial ICs used, which have inherent frequency limitations and parasitic effects from interconnections [21].

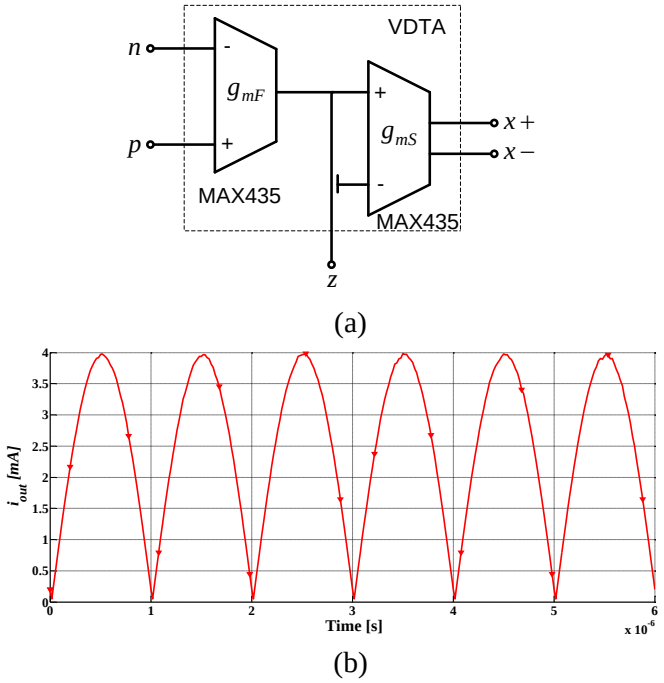


Fig. 9. (a) Practical implementation of VDTA, (b) Experimental result obtained using commercial ICs

3.2 Comparison

A thorough evaluation of the performance of the introduced full-wave rectifier circuit in comparison to prior works is detailed in Tab. 2. This comparison encompasses diverse aspects, including the count of active and passive elements, highest attainable frequency and amplitude, power consumption, and the degree of adjustability.

Table 2. Comparison with previously published rectifiers

Ref.	Type of active building blocks used	Number of diodes	Number of resistors	Maximum frequency	Maximum amplitude	Electronic tunability	Power consumption
[3]	2 CCII	2	3	10 MHz	±1 V	No	-
[4]	1 CCII, 1 DVCC, 1 MOS	-	4	1 MHz	±20 mV	No	-
[5]	1 CCII	2	2	600 kHz	±350 mV	No	-
[6]	1 CCII, 28 MOS	-	1	100 MHz	±300 mV	No	5.2 mW
[7]	2 DVCC	2	2	1 MHz	±150 mV	No	0.93 mW
[8]	2 CFOA 3 or 2 NMOS	2	0 or 1	10 MHz	±350 mV	No	1.33 mW
[9]	2 VC	2	1	9 MHz	±20 μA	No	1.38 mW
[10]	1 DO-CCII, MOS Transistors-34	-	1	1 MHz	±100 μA	No	188 μW
[11]	1 DXCCII, 2 MOS	-	2	50 MHz	±400 mV	No	≈1.4 mW
[12]	1 EXCCII-36 MOS	-	-	125 MHz	±0.5 mA	No	0.62 mW
[13]	1 EX-CCII-27 MOS	-	-	10 MHz	±200 μA	No	0.3 mW
[14]	DDCC, 2 MOS	-	3	200 MHz	±300 μA	No	2.94 mW
[15]	1 OTA (1 DVCC)	2	3	1 MHz	±300 μA	No	-
[16]	1 CCCII-21 (CM) or 23 (VM) MOS	-	-	30 MHz	±500 mV ±1 mA	Yes	1.18 mW 1.07 mW
[17]	2 CCII	-	3	200 kHz	±100 mV ±200 μA	No	-
[18]	3 OTRA 6 MOS	-	8	1 kHz	±2 V	No	-
[19]	12 MOS	-	3	85 MHz to 153.2 MHz	±100 μA	Yes	0.16 mW
[20]	1 VCII (half-wave)	2	1	1 MHz	±10 μA	No	0.6 mW
[21]	2 DVCCTA, 5 NMOS	-	-	1 MHz	200 mV	Yes	-
[22]	1 DXCCII,3 MOS	-	2	5 MHz	±0.1 mA	No	0.73 mW
[23]	CFDTIA, 2 MOS	-	-	30 MHz	±1.6 mA	No	0.76 mW
[24]	VCII	2	2	1 MHz	±0.6 V	No	0.24 mW
[25]	1 MVDTA, 4 NMOS	-	-	50 MHz	±350 mV ±10 mA	Yes	0.84 mW
[26]	1 MOCCCII, CC, 2(4) MOS	-	-	100 MHz 200 MHz	±150 mV ±300 μA	No	4.62 mW
[27]	1 CDTA, 2 CMOS	-	1	100 MHz	±200 mV ±500 μA	Yes	1.12 mW
[28]	FDDTA	-	-	50 kHz	±450 mV	No	8 μW
[29]	OTRA (6 MOS)	1	4	5 MHz	±100 μA	No	2.31 mW
[30]	1 EX-CCII-24 MOS	-	1	5 MHz	±150 mV	No	1.7 mW

[31]	1 MZC-CDTA, MOS transistors	-	-	10 kHz	±300 µA	Yes	14 mW
[32]	EXCCII, 2 MOS	-	-	30 MHz	±300 µA	No	0.2 mW
[33]	5 MOSFET	4	-	20 MHz	2 V	No	-
[34]	1 CCII, 1 DXCCII	2	2	10 MHz	±350 mV	No	-
[35]	2 OTA	4	2	1 MHz	±300 mV	Yes	1.21 mW
This work	2VDTA	-	-	50 MHz	±300 mV	Yes	0.63 mW

As shown in Tab. 2, the proposed design stands out by eliminating passive elements and using only a single active component, the VDTA. Unlike the designs in [9], this rectifier does not require additional current or voltage buffers while achieving a wide frequency range of up to 50 MHz. The extensive validation and verification of the proposed design through HSPICE and post-layout simulations further underscore its reliability. Consequently, this presented full-wave rectifier exhibits substantial potential for diverse applications across an array of fields, including signal processing, current mode filters, amplifiers, radio frequency oscillators, low-level signal conditioning and instrumentation, DC converters, oscillators, low noise amplifiers, and ASK/FSK modulators [25].

4 Conclusion

This paper presents a novel full-wave rectifier design using the VDTA as the primary active component. The design is highly efficient, requiring only one VDTA for half-wave rectification and two for full-wave rectification, without the need for passive components or diodes. This eliminates zero-crossing distortion and enables precise control of the output rectified current by adjusting the VDTAs' bias currents. The circuit's performance is thoroughly evaluated through HSPICE simulations and post-layout analysis using 0.18 µm CMOS technology parameters. Additionally, experimental validation is conducted with commercially available components. Simulation results, from both pre- and post-layout analyses, confirm excellent performance across a wide frequency range, up to 50 MHz. The study also examines the effects of non-idealities such as parasitic impedances and tracking errors on circuit operation. The proposed rectifier demonstrates strong DC and AC characteristics, excellent zero-crossing behavior, and temperature stability, achieved through effective compensation of the VDTA's transconductance temperature dependence. To assess robustness, corner analysis and Monte Carlo simulations are performed, providing insights into process variations and transistor mismatches. With a compact footprint of just 2726 µm², the proposed full-wave rectifier is well-suited for integration into ICs, making it a practical and scalable solution.

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