

SIMULATION ANALYSIS AND PERFORMANCE EVALUATION OF DC-DC CONVERTERS AND H-BRIDGE INVERTERS IN PROTEUS ENVIRONMENT

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Abstract: This paper presents a hardware-in-the-loop simulation analysis of fundamental DC-DC converters (Buck, Boost and Four-Switch Non-Inverting Buck-Boost) and DC-AC inverters (Half-Bridge and Full H-Bridge) in Proteus Professional. The switching logic and PWM pulse sequences are generated directly via an Arduino Mega 2560 microcontroller, utilizing low-level hardware timer register configurations to ensure precise dead-time insertion and duty-cycle control. Non-ideal semiconductor behavior, MOSFET channel on-resistance, diode forward drops and inductor equivalent series resistance are integrated into the power stages. The obtained results demonstrate that incorporating non-ideal component parameters provides a more realistic assessment of converter performance than ideal analytical models alone. The simulations also confirm the importance of appropriate gate-driver design and dead-time insertion for preventing destructive cross-conduction in H-Bridge configurations. The main contribution of this study is the integration of microcontroller-based control, gate-driver behavior, non-ideal power-stage modelling and multiple DC-DC and DC-AC converter topologies within a single simulation framework. This approach provides a safe and repeatable pre-prototype validation stage, reducing design uncertainty before subsequent implementation and testing on physical hardware.

Keywords: Proteus Professional, Buck, Boost, Buck-Boost, Arduino Mega 2560, H-Bridge Inverters

INTRODUCTION

The increasing integration of photovoltaic generation and other distributed energy sources has made power-electronic converters essential interfaces between DC sources, storage systems and AC loads. DC-DC converters regulate and adapt voltage levels, while DC-AC inverters provide the required alternating output. Although the fundamental behavior of these topologies is well established analytically, classical equations commonly assume ideal switches and lossless passive components. In practical systems, MOSFET on-state resistance, diode forward-voltage drop, inductor and capacitor parasitic resistances, finite switching times and gate-driver limitations cause measurable deviations from ideal converter behavior.

The transition from analog to microcontroller-based control provides greater flexibility for duty-cycle adjustment, synchronization and protection functions, but it also introduces digital timing constraints. In the ATmega2560 platform, high-frequency switching and microsecond-level dead-time require deterministic use of hardware timers rather than software delays, which may introduce timing jitter [1]. This interaction between discrete-time control and the continuous-time power stage becomes particularly important in H-Bridge inverters, where inadequate

switching synchronization may produce shoot-through and potentially destructive DC-bus currents.

A further design challenge is the gap between ideal analytical calculations and physical prototyping. Analytical models are useful for initial design but cannot fully represent practical electrical losses and switching behavior, whereas early hardware testing requires components, instrumentation and protection against potentially destructive control errors. Simulation-based virtual prototyping provides an intermediate step in which converter parameters, internal voltages and currents, gate-drive signals and abnormal switching conditions can be examined safely and repeatedly before physical assembly. Proteus Professional is therefore used in this study to combine microcontroller execution with the simulated power stage and selected non-ideal component characteristics.

The primary objective of this study is to develop and evaluate a common microcontroller-power-stage co-simulation framework for fundamental DC-DC and DC-AC converter structures. The analysis includes Buck, Boost and Four-Switch Non-Inverting Buck-Boost converters together with Half-Bridge and Full H-Bridge inverter stages. The study specifically aims to compare simulated converter behavior with ideal analytical expectations, quantify the influence of selected non-ideal parameters

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such as MOSFET channel resistance, semiconductor voltage drops and passive-component parasitic resistances, evaluate isolated HCPL-3120 and floating-bootstrap IR2110 gate-driver arrangements, examine low-level ATmega2560 hardware-timer control and verify the importance of dead-time in preventing bridge cross-conduction.

The novelty and main contribution of the work lie in the integrated evaluation of these elements within a single Proteus-based framework rather than in proposing new converter topologies. A paper links register-level ATmega2560 switching control, practical gate-driver behavior, selected non-ideal power-stage parameters and dead-time protection so that software-level timing decisions can be observed directly through converter voltage and current waveforms. Particular attention is given to the divergence between ideal and simulated converter gains and to the safe reproduction of H-Bridge cross-conduction conditions. This provides a practical bridge between ideal converter theory and subsequent physical prototype validation.

The remainder of the manuscript is organized as follows. Section II is reserved for a Literature Review, Section III presents the research methodology and the implemented simulation architecture, including the DC-DC topologies, inverter stages, microcontroller control and gate-driver circuits. Section IV presents and discusses the simulation results, with emphasis on converter performance, non-ideal effects and bridge switching behavior. The final section summarizes the main findings, limitations of the simulation approach and directions for future physical prototype validation.

1. LITERATURE REVIEW

1.1. Power Converter Modelling: From Ideal Theory to Non-Ideal Behaviour

DC-DC and DC-AC power converters represent essential elements of modern renewable-energy and power-electronic systems. The fundamental operating principles of these converters are well established, however, their practical behavior can differ significantly from the predictions obtained using ideal analytical models.

Classical power-electronics analysis provides the fundamental voltage-conversion relationships for Buck, Boost and Buck-Boost converters. Rashid [2], for example, describes these converter topologies using steady-state relationships based on volt-second balance and idealized switching assumptions. Such models are essential for understanding converter operation and determining initial component values. In practical implementations, however, semiconductor devices and passive components cannot be considered lossless - various power elements cause

deviations from ideal voltage-conversion relationships. At higher switching frequencies, switching losses and electromagnetic interference may also become significant and require careful design and filtering. Consequently, the simulation can be used not only to confirm basic converter operation but also to examine the extent to which practical component characteristics alter the expected converter response. For an ideal Buck converter operating in continuous conduction mode, the output voltage is proportional to the input voltage and the duty cycle. In contrast, the ideal Boost converter increases the input voltage, while the Buck-Boost family provides both step-down and step-up conversion, depending on the topology and control strategy. Erickson and Maksimović [3] provide a systematic treatment of converter operating principles, steady-state analysis, and dynamic modeling, establishing a theoretical foundation for evaluating switching-converter performance. These analytical relationships are useful for initial design, but their predictions depend on assumptions concerning semiconductor switches and passive components.

Practical converter performance is influenced by MOSFET on-state resistance, diode forward-voltage drop, inductor winding resistance, capacitor equivalent series resistance and switching-related losses. These non-ideal characteristics affect the achievable voltage gain, conduction losses, output-voltage ripple, and transient response. Consequently, a converter operating under realistic component parameters may exhibit a substantial deviation from its ideal voltage-conversion ratio. Rashid [2] provides a broad reference on power-conversion topologies, semiconductor devices, and practical power-electronic circuits, while Erickson and Maksimović [3] establish the analytical methods required to interpret the differences between ideal and non-ideal behavior.

Syed et al. [4] investigated the performance of a non-isolated DC-DC converter with a wide input voltage range for photovoltaic applications. Their study involved mathematical modeling and PSIM-based simulation of a 3-kW converter, focusing on voltage gain, conversion efficiency, and continuous conduction mode (CCM) operation. The proposed topology employed a reduced redundant power processing approach to improve energy conversion under varying input conditions. Their analysis highlighted the importance of considering practical operating conditions when evaluating converter efficiency rather than relying exclusively on ideal voltage-conversion relationships. A similar distinction between theoretical and simulated behavior is observed in the present study, where the Boost converter produces an output voltage of 29.16 V compared with the ideal prediction of 43.75 V. Although the investigated converter topologies and operating conditions differ, both studies demonstrate the importance of evaluating practical electrical characteristics when assessing DC-DC converter performance.

Madhappan and Selvaraju [5] conducted a comparative analysis of four non-isolated DC-DC converter topologies for photovoltaic applications, including conventional Boost, interleaved Boost, quasi-Z-source, and switched-capacitor converters. The models were developed in MATLAB/Simulink and experimentally validated using a programmable photovoltaic source and an STM32F103 microcontroller. At an output power of 200W, the interleaved Boost converter achieved the highest measured efficiency of 91.1%, followed by the quasi-Z-source converter at 88.7%, the conventional Boost converter at 84.0%, and the switched-capacitor converter at 80.4%. These results demonstrate that converter topology significantly influences achievable efficiency and overall operating performance. In comparison, the present research focuses on the voltage-conversion characteristics of fundamental DC-DC topologies rather than experimentally measured efficiency. The simulated Buck converter achieved an output voltage of 24.04 V at a duty cycle of 0.24, while the non-inverting Buck-Boost converter maintained a positive output polarity and produced 34.12 V from a 35 V input at the investigated unity-gain operating point. Together, these studies emphasize the importance of evaluating converter performance beyond ideal theoretical assumptions, although they address different performance metrics and validation methods.

Recent research has extended the analysis of conventional converters toward performance comparison and renewable-energy applications. Mumtaz et al. [6] review non-isolated DC-DC converter topologies and associated control techniques, discussing the relevance of topology selection and controller design to the performance of renewable-energy systems. Sutikno et al. [7] compare high-gain converter structures for photovoltaic applications, emphasizing design trade-offs involving voltage gain, component count, switch voltage stress, complexity, and efficiency. More recently, Mohammad et al. [8] evaluated multiple non-isolated converter topologies through MATLAB/Simulink modeling, considering output voltage, current, efficiency, and ripple-related performance parameters.

These studies demonstrate that converter evaluation should extend beyond the verification of an ideal conversion ratio. However, much of the reviewed literature focuses on photovoltaic applications, specialized high-gain structures, or comparisons among different converter topologies. The present study instead investigates conventional Buck and Boost converters together with a four-switch non-inverting Buck-Boost converter under a common microcontroller-controlled simulation framework. Particular attention is given to the relationship between ideal analytical predictions and simulated behavior when selected semiconductor and passive-component non-idealities are included.

Pulse-width modulation (PWM) is a widely used switching-

control method in power electronics. By adjusting the switching duty cycle, PWM regulates the average voltage applied to a converter's energy-transfer elements. In DC-DC converters, the switching sequence and duty cycle influence the steady-state conversion ratio, inductor-current waveform, output-voltage ripple, and dynamic response. In inverter applications, the modulation strategy additionally determines the switching sequence used to synthesize an alternating output voltage.

Holmes and Lipo [9] provide a comprehensive treatment of PWM principles and their application to power converters, including inverter modulation techniques and the relationship between switching patterns and output-waveform quality. Their work provides a standard theoretical reference for discussing PWM-based power conversion. For microcontroller-controlled implementations, the theoretical modulation strategy must also be translated into accurate digital switching events. Timer resolution, switching frequency, duty-cycle resolution, output synchronization, and timing delays can affect the generated switching signals.

Previous studies have investigated individual DC-DC converter topologies from both theoretical and simulation perspectives. Gowri et al. [10] examined Arduino Nano-controlled Buck, Boost and Buck-Boost converters, demonstrating that inexpensive microcontroller platforms can provide a practical alternative to more complex control circuitry. Similarly, Nallusamy and Rukmani [11] investigated the design and simulation of Arduino Nano-controlled DC-DC converters for low- and medium-power applications. Their study further demonstrates the suitability of combining microcontroller control with simulation-based converter development.

Lyu and Zhang [12] also analyzed a MOSFET-based Buck switching circuit using digital control, with emphasis on simplifying circuit architecture for educational and basic DC power-supply applications. Together, these studies demonstrate the usefulness of low-cost digital controllers for fundamental switching-converter applications.

However, these studies are primarily concerned with individual DC-DC converter implementations and basic digital control. They do not provide a unified evaluation of DC-DC and DC-AC conversion stages that simultaneously considers low-level microcontroller timing, non-ideal component behavior, gate-driver operation and bridge cross-conduction protection.

Buck-Boost conversion has also been investigated independently. Uddin et al. [13] presented a performance analysis of a DC-DC Buck-Boost converter, providing a useful basis for understanding combined step-up and step-down operation. The present research extends this direction by considering a Four-Switch Non-Inverting Buck-Boost configuration and observing its transition

between Buck and Boost operating regions. In the investigated model, the converter is tested at a 50% duty cycle and during transient changes between the two operating regions.

The relevance of including non-ideal parameters becomes evident when simulated results are compared with theoretical expectations. For example, the Boost-converter model developed in the present research incorporates MOSFET on-state resistance and inductor parasitic resistance. The resulting output therefore differs considerably from the value predicted by an ideal lossless model. This illustrates an important distinction between using simulation simply to reproduce ideal equations and using simulation as a virtual prototype in which selected physical component characteristics are deliberately introduced.

1.2. Half-Bridge and Full H-Bridge Inverter Topologies

The Half-Bridge represents one of the fundamental inverter structures. It typically consists of two complementary semiconductor switches connected across a split DC link, with the output taken from the midpoint of the switching leg. The structure is comparatively simple but limits the available output-voltage amplitude and requires a split DC-link arrangement.

The Full H-Bridge extends this principle by employing two switching legs and four semiconductor devices. This enables both polarities of the DC-link voltage to be applied across the load and therefore provides greater utilization of the available DC-bus voltage.

Previous literature has investigated both structures. Chaudhary and Sharma [14] discuss the operation and application of Half-Bridge inverters, providing the theoretical basis for this converter structure. Chen et al. [15] evaluated H-Bridge and Half-Bridge converter configurations, demonstrating the importance of topology selection in converter performance. Although their application was capacitive-coupled wireless charging, their comparison provides relevant background regarding the structural differences between Half-Bridge and Full H-Bridge arrangements.

In the present research, the Half-Bridge and Full H-Bridge are instead investigated as DC-AC conversion stages under a common microcontroller-based control framework. With a 50 V DC source, the Half-Bridge model provides an output swing corresponding to approximately half of the DC-link voltage, whereas the Full H-Bridge allows the load voltage to alternate across the full DC-link range. This allows the two inverter structures to be compared within the same simulation environment while maintaining a common control and measurement framework.

Another recent study has examined inverter performance under different modulation and implementation conditions. Akaaboune et al. [16] presented the design and implementation of a three-level single-phase H-Bridge inverter using selective harmonic elimination PWM, comparing its performance with sinusoidal PWM and investigating total harmonic distortion. Their work illustrates the importance of modulation strategy and output-waveform analysis when evaluating inverter performance. In a related experimental study, the performance of different carrier-based PWM techniques for a single-phase H-Bridge inverter was investigated by comparing unipolar and bipolar SPWM and third-harmonic-injection PWM at different switching frequencies [17]. The results emphasize the relationship between modulation choice, switching frequency, and harmonic performance.

Although these studies provide useful evidence concerning inverter modulation and output quality, their primary emphasis is on waveform synthesis, harmonic reduction, or experimental inverter performance. The present research has a different scope: Half-Bridge and Full H-Bridge structures are evaluated within the same Proteus simulation environment used for the DC-DC converters. This enables a consistent examination of output-voltage behavior, switching signals, and gate-driver operation without claiming that the investigation constitutes a comprehensive THD or efficiency study.

Abdul Hamid et al. [18] presented the design and simulation of a single-phase inverter using unipolar sinusoidal pulse-width modulation. Their MATLAB/Simulink model incorporated a MOSFET-based Full H-Bridge, a microcontroller-based switching control circuit, and an LC output filter. The simulation results demonstrated a significant reduction in total harmonic distortion, from 53.97% without the output filter to 2.95% with filtering. However, the experimental prototype, controlled by an Arduino Uno, produced a higher THD of 25.6%, highlighting the differences between idealized simulation conditions and practical hardware behavior. In comparison, the present research investigates the switching behavior of Half-Bridge and Full H-Bridge configurations in Proteus, where the Half-Bridge produces approximately ± 24.8 V and the Full H-Bridge achieves an output swing of ± 50 V from a 50 V DC supply. While Abdul Hamid et al. focused on sinusoidal waveform synthesis and harmonic reduction, the present study emphasizes DC-bus voltage utilization, gate-driver operation, and dead-time protection. Both studies demonstrate the importance of evaluating the interaction between digital control signals and the inverter power stage, although they address different aspects of inverter performance.

Aihsan et al. [19] investigated the performance of a single-phase Full H-Bridge inverter employing unipolar SPWM under resistive and inductive load conditions. Their research combined PSIM simulation with experimental testing to

evaluate output-voltage waveforms and total harmonic distortion. The inverter was operated at a modulation index of 0.8 and a switching frequency of 5 kHz, with an LC filter used to improve output waveform quality. Under the investigated inductive load conditions, the measured voltage THD decreased from 12.8% before the transformer to 5.57% after the transformer, while the output waveform exhibited a more sinusoidal shape than under the tested resistive load. These findings demonstrate that load characteristics and output-stage components significantly influence inverter waveform quality. In comparison, the present study evaluates the Half-Bridge and Full H-Bridge topologies primarily through their voltage waveforms and switching behavior, rather than through harmonic analysis under different load conditions. Furthermore, the present Full H-Bridge simulation examines the influence of dead-time insertion, where the introduction of a 300 μ s blanking interval eliminates the simulated shoot-through current spikes exceeding 45 A under the investigated conditions. Thus, while Aihsan et al. emphasized output waveform quality and load-dependent harmonic performance, the present research focuses on gate-driver behavior and the prevention of unsafe switching overlap.

1.3. Gate-Driver Requirements and Dead-Time Protection

The switching commands produced by a microcontroller cannot generally be applied directly to the gates of power MOSFETs, particularly in bridge configurations. High-side N-channel MOSFETs present an additional challenge because their source potential changes with the switching node. Dedicated gate-driver circuits are therefore required to provide the appropriate gate-to-source voltage and sufficient gate-charging current.

Darjat et al. [20] investigated a single-phase Full-Bridge inverter using a bootstrap circuit for a photovoltaic application. Their work demonstrates the practical importance of bootstrap-based high-side switching and provides relevant background for the gate-driver configuration used in Full H-Bridge systems.

The present research considers two gate-driving approaches: an isolated HCPL-3120-based driver and an IR2110 driver using a bootstrap network. In the IR2110 arrangement, the bootstrap diode and capacitor provide the floating supply required by the high-side driver during appropriate switching intervals.

Another H-Bridge research has continued to investigate the integration of dedicated gate drivers and controlled switching sequences. Akaaboune et al. [16], for example, describe an inverter implementation using dedicated high- and low-side drivers and complementary MOSFET switching. Nevertheless, output-waveform and harmonic analyses do not necessarily provide a direct evaluation of the current consequences of unsafe switching overlap. In this study, an isolated HCPL-3120-based driver

arrangement and an IR2110 bootstrap configuration are considered within the simulation framework. The complementary switching behavior is examined with and without an inserted blanking interval. This approach enables the simulated electrical consequences of unsafe switching to be compared with protected operation. The analysis is intended as a simulation-based examination of switching behavior rather than experimental proof of hardware reliability.

In addition to high-side gate driving, safe bridge operation requires careful coordination of complementary switching signals. Jati and Haspari [21] emphasize that the two MOSFETs belonging to the same Full H-Bridge leg must not conduct simultaneously. Such simultaneous conduction creates a direct path across the DC supply and produces the condition known as shoot-through. Appropriate dead-time must therefore be introduced between complementary switching transitions.

This represents an area where simulation provides a particularly important contribution. Previous literature establishes the requirement for avoiding simultaneous switch conduction, while the present research uses the virtual model to observe the electrical consequence of this condition directly. The bridge can be simulated both with and without an appropriate blanking interval, allowing the resulting DC-bus current behavior to be compared without exposing physical MOSFETs to potentially destructive current.

Therefore, dead-time is not treated only as a theoretical protection requirement. Its effect can be observed directly through the simulated switching and current waveforms.

1.4. Importance of Simulation-Based Development

Mathematical models provide an essential understanding of converter operation but necessarily rely on simplifying assumptions. Physical prototypes, on the other hand, provide the most realistic representation of system behavior but require components, instrumentation, fabrication time and appropriate protection against electrical faults.

A detailed simulation model provides an intermediate development stage in which converter topology, embedded control, gate-driver behavior and selected non-ideal component characteristics can be evaluated before physical assembly. One of the most significant advantages of this approach is rapid design modification. Component values, switching frequencies, duty cycles and load conditions can be changed without rebuilding a circuit. Different operating conditions can therefore be evaluated quickly.

A second advantage is observability. Simulation provides direct access to internal circuit variables that may be difficult to measure in a physical prototype. Inductor

currents, MOSFET gate signals, switching-node voltages and DC-bus currents can be observed simultaneously without adding physical probes to the circuit. This is particularly useful when studying switching converters because measurement instrumentation can itself influence high-frequency circuits.

A third advantage is repeatability. A physical circuit may be affected by temperature, component tolerances, supply variation and measurement noise. In simulation, identical initial conditions and component parameters can be reproduced, allowing the influence of a single parameter to be investigated independently.

A fourth and particularly important advantage is safety. Converter control errors can result in excessive current, overvoltage or semiconductor destruction. This is especially relevant for Full H-Bridge circuits, where an incorrect complementary switching sequence can short the DC bus through two simultaneously conducting MOSFETs. Simulation enables such conditions to be deliberately reproduced and investigated without risking physical equipment.

Finally, simulation reduces the cost and time associated with early-stage prototyping. Multiple circuit configurations can be evaluated before selecting the most appropriate design for fabrication. This does not eliminate the need for hardware implementation, but it can significantly reduce the number of physical iterations required.

1.5. Simulation versus Physical Equipment

Although simulation provides considerable advantages, it is important to distinguish between a simulated converter and a physical power-electronic system. The resulting waveform can be compared with the ideal analytical result under otherwise identical conditions. This makes it easier to determine why a particular deviation occurs.

In physical hardware, all non-ideal effects occur simultaneously. Although this produces the most realistic result, it can make causal analysis more difficult. A measured reduction in output voltage may result from conduction losses, temperature, wiring resistance, component tolerance or several interacting effects. Simulation permits these effects to be introduced individually and systematically.

Simulation also allows potentially destructive conditions to be tested safely. For example, an intentionally incorrect H-Bridge switching sequence can be examined to determine whether cross-conduction occurs. Performing the same experiment on physical equipment could destroy the semiconductor switches or damage the DC supply.

However, physical hardware provides information that simulation cannot completely reproduce. Real PCB

layouts contain stray inductances and capacitances. Switching nodes generate electromagnetic interference and high-frequency coupling. Semiconductor junction temperatures change dynamically, modifying electrical parameters such as $R_{DS(on)}$. Gate-driver propagation delays may differ between individual devices, while sensors and ADCs introduce measurement noise and tolerances.

Consequently, even a detailed simulation cannot reproduce every aspect of a manufactured converter. This limitation is particularly important in the thermal domain. The simulation environment used in the thesis includes electrical non-idealities but does not fully reproduce dynamic semiconductor self-heating, temperature-dependent parameter drift, PCB stray loop inductances or high-frequency EMI coupling. Physical prototype measurements would therefore still be required to obtain thermal characteristics, experimental efficiency curves and electromagnetic-performance data. For this reason, simulation should not be presented as a replacement for physical testing. Theoretical equations establish expected converter behavior. Simulation then introduces selected practical characteristics and enables control and protection strategies to be verified safely. Finally, physical testing determines whether the design remains valid when exposed to real thermal, electromagnetic, manufacturing and measurement effects. The contribution of simulation is therefore that it reduces uncertainty before physical construction.

1.6. Research Gap and Positioning of the Present Work

The reviewed literature demonstrates that the individual elements required for digitally controlled power conversion are well established. However, based on the reviewed sources, these elements are generally investigated separately.

First, Arduino-based DC-DC studies demonstrate the feasibility of low-cost digital converter control but do not combine Buck, Boost and Four-Switch Non-Inverting Buck-Boost converters with Half-Bridge and Full H-Bridge inverter stages within the same simulation framework.

Second, existing converter studies provide important analytical and simulation results, but simplified analyses often rely on ideal or near-ideal switching assumptions. The present research deliberately introduces selected non-ideal electrical parameters so that the difference between theoretical voltage conversion and more realistic simulated behavior can be examined.

Third, existing microcontroller-controlled converter studies do not generally combine converter analysis with detailed low-level ATmega2560 timer configuration. The present work directly configures the microcontroller hardware timers rather than treating the controller merely as a generic PWM source. This allows the digital timing

architecture and the electrical switching behavior to be analyzed as parts of the same system.

Fourth, existing inverter studies establish the importance of appropriate gate driving and avoidance of shoot-through. The present work combines this knowledge with explicit simulation of the gate-driver circuits and dead-time protection. The unsafe cross-conduction condition can therefore be compared directly with protected operation.

Finally, there remains a methodological gap between ideal analytical studies and direct physical implementation. Purely analytical models cannot reproduce many non-ideal electrical effects, while physical prototyping introduces cost, measurement complexity and the possibility of component damage during early controller development. The present research positions microcontroller-power-stage co-simulation as an intermediate engineering stage between these two approaches.

Its contribution is therefore not based on introducing a new Buck, Boost or H-Bridge topology. These converter structures are already well established in the literature. Instead, the contribution lies in integrating multiple converter structures, low-level ATmega2560-based switching control, non-ideal component parameters, gate-driver dynamics and dead-time verification within a common simulation environment. This integration enables a systematic transition from ideal theoretical equations toward behavior that more closely approximates the conditions expected in physical hardware.

1.7. Literature Review Synthesis

The reviewed literature establishes a strong theoretical and practical foundation for microcontroller-controlled power conversion. Fundamental converter theory provides the analytical relationships required for Buck, Boost and Buck-Boost design, while previous Arduino-based studies demonstrate that low-cost digital controllers can successfully generate the switching signals required by these converters.

Research concerning Half-Bridge and Full H-Bridge structures further establishes the requirements for DC-AC conversion, including high-side gate driving, complementary switching and prevention of shoot-through.

Nevertheless, the literature also demonstrates why theoretical analysis alone is insufficient for evaluating practical converter behavior. Real semiconductor and passive-component characteristics cause voltage drops, losses and transient effects that are absent from ideal equations. Similarly, gate-driver dynamics and switching overlap can significantly influence inverter reliability. Simulation provides a practical method for examining these effects before hardware construction. Its primary value is not that it perfectly reproduces physical equipment, but that it provides a safe, repeatable and highly observable

virtual prototype in which embedded control and power-stage behavior can be evaluated together.

At the same time, simulation has clear limitations. Thermal self-heating, electromagnetic interference, PCB-dependent parasitic effects, component tolerances and measurement noise ultimately require physical verification. The literature therefore supports a development methodology in which theoretical analysis, simulation and physical testing are complementary rather than competing approaches. The resulting simulation environment provides a bridge between ideal converter theory and future physical implementation, allowing critical design decisions, switching behavior and protection mechanisms to be evaluated before the cost and risk associated with hardware fabrication are introduced.

2. METHODOLOGY

The research methodology is based on simulation modeling and performance analysis of power converters within the Proteus Professional environment. The Proteus models include selected non-ideal electrical parameters, so the control layer, gate-driver layer and power stage can be observed within the same simulation. However, the model does not fully reproduce PCB stray inductance, electromagnetic interference, component tolerances or dynamic semiconductor self-heating. The results should therefore be interpreted as pre-prototype validation rather than a replacement for final experimental hardware measurements.

The simulation architecture was organized into three interconnected functional layers: the digital control layer, the gate-driver layer, and the power-conversion layer. The digital control layer was implemented using an Arduino Mega 2560, which generated the required PWM and complementary switching signals through direct configuration of the ATmega2560 Timer1 registers. The gate-driver layer interfaced the low-voltage microcontroller outputs with the MOSFET gates and included the HCPL-3120 isolated driver and the IR2110 floating high-side driver, depending on the converter topology. The third layer consisted of the corresponding DC-DC or DC-AC power stage, including the switching devices, diodes, inductors, capacitors, and resistive loads. This structure allowed the switching commands generated by the actual microcontroller firmware to be directly applied to the simulated power circuit.

The Arduino Mega 2560 was configured at its standard 16 MHz clock frequency. Timer1 was used as the main PWM generation peripheral because it provides a 16-bit counter and allows the switching frequency and duty-cycle resolution to be configured through the TCCR1A, TCCR1B, ICR1, and OCR1A/OCR1B registers. The COM bits were used to define the output behavior, the WGM

bits to select the waveform-generation mode, and the CS bits to select the timer prescaler. For high-frequency switching applications, a prescaler of $N = 1$ was used. Depending on the converter under investigation, fixed-TOP and variable-TOP PWM modes were evaluated. In particular, Fast PWM Mode 7 provides 10-bit resolution with $TOP = 1023$ and a theoretical switching frequency of approximately 15.625 kHz at a 16 MHz clock, while Mode 14 allows the TOP value to be defined through ICR1 and therefore provides direct control of the switching frequency.

2.1. Topological Specifications of DC-DC Converters

Figure 1 presents the complete Proteus implementation of the Buck converter used in this study. The Arduino Mega 2560 generates the PWM switching command, while the driver stage interfaces the low-voltage control domain with the MOSFET power stage. The converter is supplied from 100 VDC and uses a 330 μ H inductor and a 220 μ F output capacitor. The component values were selected according to the continuous-conduction-mode design calculations, while the operating point was selected to obtain an output voltage of approximately 24 V. The Arduino-generated PWM signal was applied through the gate-driver stage to the MOSFET switching device. A resistive load was connected at the converter output, and virtual oscilloscope channels were used to observe the PWM signal, output voltage, and inductor-current response. The simulation was therefore used not only to verify the expected voltage-conversion ratio but also to evaluate the transient response, output-voltage ripple, and continuity of the inductor current.

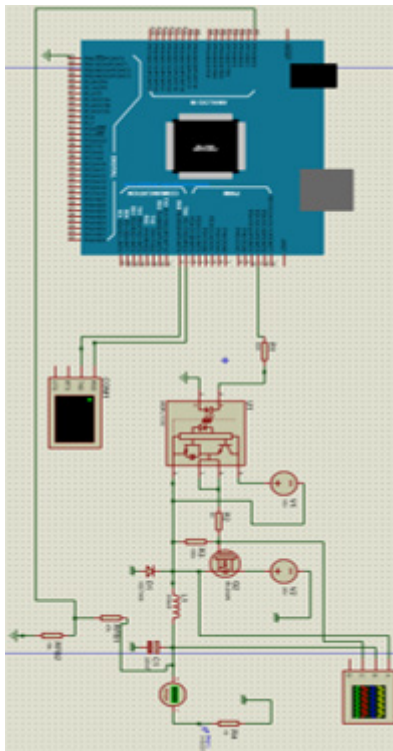


Figure 1: Buck Converter Circuit in Proteus Professional

Figure 2 shows the Proteus model of the Boost converter supplied from a 35 V DC source. The converter was operated at a switching frequency of 20 kHz, obtained using Timer1 with ICR1 = 799 as the TOP value. The influence of the inductor series resistance and MOSFET channel resistance is included so that their effect on the obtainable voltage gain can be observed. The configuration therefore enables a controlled comparison between the theoretical lossless prediction and the simulated converter response. The significance of these parameters becomes evident in Figure 7, where the simulated output reaches 29.16 V instead of the ideal calculated value of 43.75 V. This comparison demonstrates why simulation with non-ideal parameters is useful before hardware construction: the ideal equation alone does not reveal the magnitude of voltage-gain degradation caused by combined conduction losses.

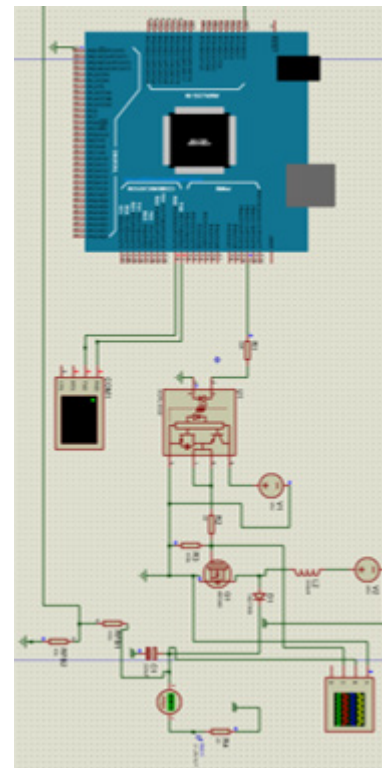


Figure 2: Boost Converter Circuit in Proteus Professional

Figure 3 illustrates the implemented non-inverting Buck-Boost configuration. The topology permits both step-down and step-up operation while maintaining the same output-voltage polarity as the input. The simulation is evaluated around the unity-gain operating point at $D = 0.5$ and through duty-cycle transitions between Buck and Boost operation. This test is particularly suitable for simulation because the duty ratio can be swept under repeatable conditions while internal switching behavior and output response are observed simultaneously. The corresponding results in Figure 8 are used to determine whether the transition occurs without voltage discontinuities or excessive transient behavior [2].

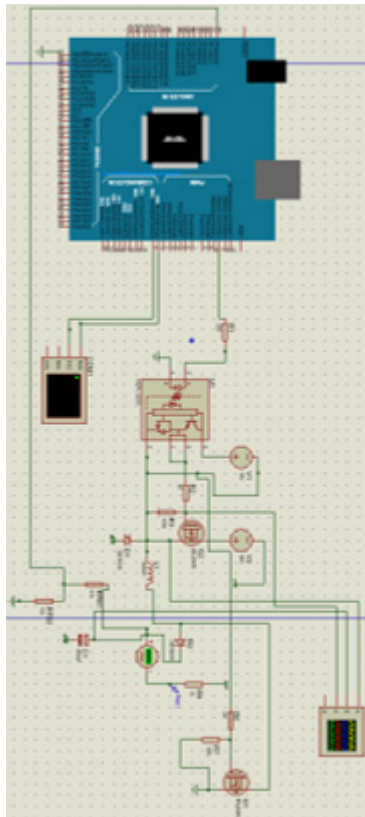


Figure 3: Noninverted Buck-Boost Converter Circuit in Proteus Professional

2.2. Inverter Bridge Topologies and Gate Driver Circuits

Figure 4 presents the Half H-Bridge simulation model supplied from a 50 VDC bus. A capacitive voltage divider

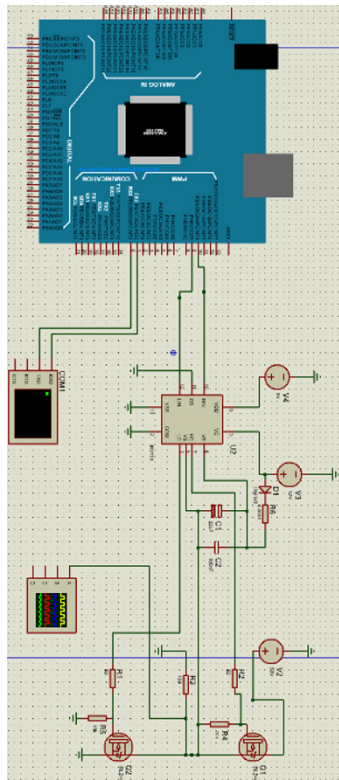


Figure 4: Half H-Bridge Circuit in Proteus Professional

creates an artificial neutral point, allowing the switching node to alternate ideally between approximately +25 V and -25 V. The simulation therefore evaluates not only the expected voltage conversion but also the stability of the capacitive midpoint under load. This is relevant because neutral-point drift can be observed directly in the virtual environment without additional physical differential-measurement hardware. The effect is subsequently quantified in Figure 9, where the output reaches approximately ± 24.8 V and increasing load current produces visible midpoint ripple.

Figure 5 shows the complete Full H-Bridge configuration consisting of four MOSFETs arranged in two complementary switching legs. In contrast to the Half-Bridge, this topology utilizes the full DC bus and therefore allows the load voltage to alternate across the complete supply range. A 50 V DC link was applied to the bridge, while the switching signals were generated by the Arduino Mega 2560. High-side gate driving was implemented using the IR2110 bootstrap driver and, for isolated gate-drive operation, the HCPL-3120 configuration was also evaluated. In the IR2110 implementation, the bootstrap network included a 22 μ F capacitor, while 22 Ω series gate resistors and 100 k Ω pull-down resistors were included in the gate-drive circuitry. These component values were used to reproduce the required gate-drive behavior and provide controlled switching of the MOSFETs.

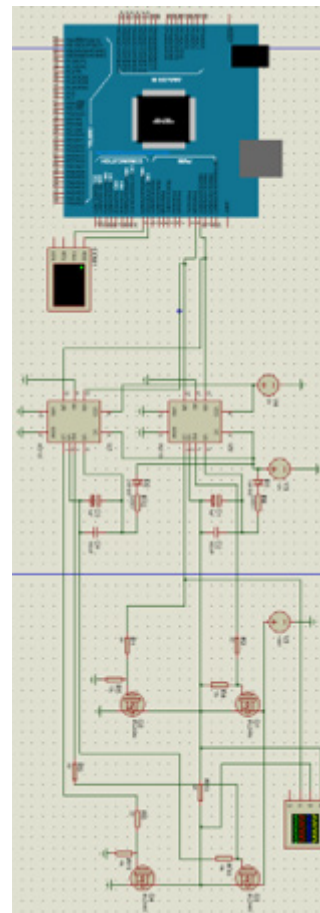


Figure 5: Full H-Bridge Circuit in Proteus Professional

This is particularly important for evaluating dead-time because unsafe overlap between complementary switches can be deliberately reproduced in simulation and its current consequence observed without risking destruction of physical MOSFETs or the DC source. The corresponding electrical behavior is evaluated in Figure 10 and in the subsequent shoot-through analysis. It enables a full output voltage swing from -50 V to +50 V, generating an AC output profile with an effective frequency of 1.67 kHz.

- 1) **Gate Drivers (HCPL-3120 and IR2110 Bootstrap)**
Driving high-side MOSFET switches requires specialized driver configurations. Two approaches are tested in simulation. First one is HCPL-3120 optocoupler driver that provides galvanic optical isolation between control circuitry and power stages while delivering high gate-charging current capability. Next one is IR2110 with bootstrap network. It employs an external bootstrap diode and capacitor to supply the floating high-side driver during low-side MOSFET conduction intervals.
- 2) **Dead-Time Protection Implementation**
DC bus shoot-through occurs when upper and lower MOSFETs in the same leg conduct simultaneously due to turn-off propagation delays. To prevent this phenomenon, a dedicated hardware/signal dead-time delay is introduced. Total switching period is 600 μ s (switching frequency of 1.67 kHz). Dead-time interval is a safety blanking delay of 300 μ s inserted between turn-off and turn-on commands of complementary MOSFETs within a leg [9].

3. RESULTS

This section presents a detailed qualitative and quantitative evaluation of the simulation outputs obtained via the Proteus Professional virtual oscilloscope and logic analyzer instruments. The analysis bridges the gap between idealized steady-state equations and the physical realities of power electronic converters, capturing transient behavior, semiconductor conduction losses, parasitic damping and gate-drive dynamics under load.

3.1. Buck (Step-Down) Converter: Continuous Conduction Dynamics & Ripple Profile

Figure 6 presents the simulated Buck converter response and allows the switching waveform, transient output behavior and steady-state operation to be evaluated together. At $D = 0.24$, the output initially reaches approximately 27.2 V and then settles at about 24.04 V. Upon enabling the PWM drive signal at $D = 0.24$, the output voltage exhibits a smooth, second-order critically damped envelope. The initial inrush current through the 330 μ H inductor produces a brief, controlled voltage overshoot peaking at 27.2 V within 0.35 ms, after which

the output settles cleanly into its nominal 24.04 V steady state.

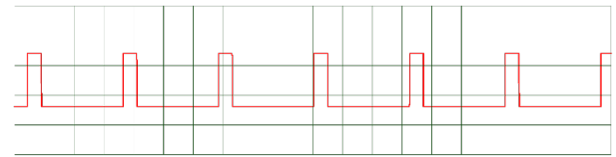


Figure 6: Buck Converter Simulation Results in Proteus Professional

The virtual oscilloscope trace of the inductor current displays a classic symmetric sawtooth profile. The current ramps upward during the MOSFET conduction interval (ton) with a slope dictated by $(V_{in} - V_{out})/L$ and decays linearly during the freewheeling interval (toff) through the diode. Crucially, the minimum trough of the inductor current remains strictly above zero ($I_{L,min} \approx 1.85$ A at 10 Ω load), providing visual and numerical confirmation of Continuous Conduction Mode.

Across the 220 μ F filter capacitor, the steady-state output voltage trace exhibits an exceptionally tight peak-to-peak ripple ($\Delta V_{out} \approx 0.32$ V), representing less than 1.35 % of the nominal DC output voltage. The absence of high-frequency ringing or parasitic spikes confirms that the output filtering network effectively absorbs switching harmonics at 20 kHz. The relevance of this result is that CCM operation, transient overshoot and output ripple can be checked simultaneously before final component selection and physical construction.

3.2. Boost (Step-Up) Converter: Parasitic Damping & Realized Voltage Transfer Limitation

Figure 7 provides the clearest comparison between ideal analytical behavior and the non-ideal simulated model - a compelling demonstration of how parasitic elements reshape the energy transfer process.

Under lossless theoretical assumptions at a constant duty ratio, the Boost converter is expected to step up 35 V to an ideal output of 43.75 V. However, the captured steady-state waveform in Proteus reveals a plateauing output voltage at exactly 29.16 VDC under a 10 Ω load.

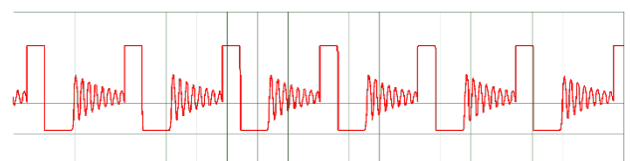


Figure 7: Boost Converter Simulation Results in Proteus Professional

A close examination of the internal branch currents reveals the mechanism of this attenuation. During ton, high peak charging currents flowing through the inductor encounter the internal series equivalent resistance ($R_L \approx 0.45$ Ω)

and the MOSFET channel resistance ($R_{DS(on)} \approx 0.18 \Omega$). This produces a significant I^2R Ohmic voltage drop that subtracts directly from the energy stored in the magnetic field. Consequently, during toff, the collapsing magnetic field collapses across the load with reduced energy density, bounded further by the forward conduction voltage drop ($V_F \approx 0.7 \text{ V}$) of the freewheeling diode.

When subjecting the Boost converter to step-up load variations, the output trace displays a pronounced sag before recovery, highlighting the right-half-plane (RHP) zero characteristic inherent to Boost topologies in continuous conduction. The observed reduction in output demonstrates that conduction losses can substantially alter the expected voltage gain. This is an important benefit of simulation over relying only on ideal calculations, since individual non-ideal parameters can be introduced and their influence studied before a physical prototype is assembled.

3.3. Non-Inverting Buck-Boost Converter: Smooth Mode Transitions & Polarity Integrity

Figure 8 shows the response of the non-inverting Buck-Boost converter while preserving positive output polarity. Unity gain operating point with $D = 0.5$ and at 50 % duty cycle with a 35 VDC input, the dual-switch topology produces a clean 34.12 VDC output trace. The minor 0.88 V drop from ideal unity gain is attributed to the combined forward drops of the two series-connected semiconductor switches conducting simultaneously in this topology.

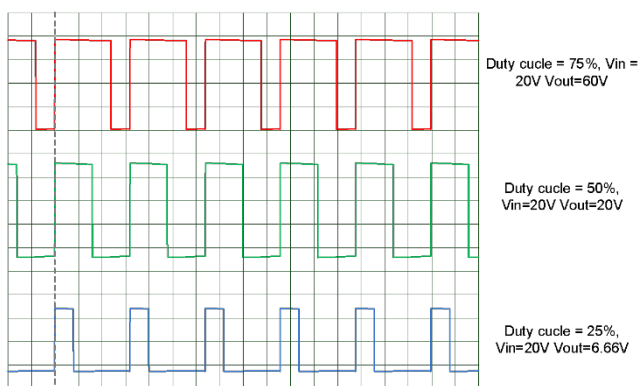


Figure 8: Noninverted Buck-Boost Converter Simulation Results in Proteus Professional

Interesting behavior, seamless Buck-to-Boost mode crossover, is obtained by sweeping the duty ratio continuously from $D = 0.3$ (Buck mode) to $D = 0.7$ (Boost mode), the output trace smoothly transitions without experiencing discontinuous voltage jumps, severe ringing, or magnetic saturation in the inductor. The output voltage tracks proportionally, proving the superior dynamic flexibility of the four-switch non-inverting architecture over single-switch inverting configurations.

3.4. Half-Bridge Inverter: Split-Capacitor Neutral Drift & Voltage Balance

Figure 9 presents the Half H-Bridge output and the behavior of the split-capacitor neutral point with a 50 VDC rail, simulated to assess the stability of the artificial midpoint generated by twin series capacitors ($C_1=C_2=100 \mu\text{F}$).

The steady-state AC output waveform exhibits a symmetric square profile stepping cleanly between +24.8 V and -24.8 V. This confirms the expected $\pm \text{VDC}/2$ peak amplitude reduction inherent to half-bridge conversion. Under increased load current, the simulated midpoint develops a low-frequency ripple because the two capacitors charge and discharge during alternate half-cycles. The result identifies neutral-point stability as a practical limitation of the Half-Bridge structure and demonstrates how simulation can reveal this design weakness before hardware implementation.

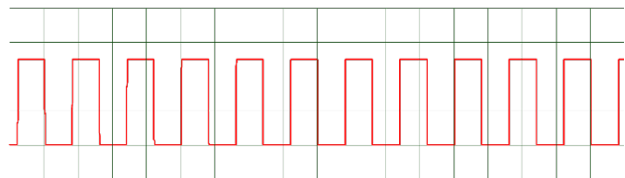


Figure 9: Half H-Bridge Simulation Results in Proteus Professional

When the AC output load current increases beyond 1 A, the oscilloscope trace reveals a low-frequency triangular voltage ripple superimposed on the artificial neutral node. Because each capacitor charges and discharges during alternate half-cycles, insufficient capacitance leads to mid-point potential drift, resulting in slight amplitude asymmetry between the positive and negative half-cycles of the AC output [7].

3.5. Full H-Bridge Inverter: High-Side Driver Dynamics & Full Rail Swing

Figure 10 presents the Full H-Bridge output waveform and confirms full DC-bus utilization.

The differential voltage measured across the AC load demonstrates a full $\pm 50 \text{ V}$ peak-to-peak square wave envelope. The waveform period is captured precisely at $T = 600 \mu\text{s}$, confirming an effective fundamental AC output frequency of $f_{out} = 1.67 \text{ kHz}$.

The gate-driver analysis also verifies floating high-side operation: the bootstrap arrangement maintains the required gate-to-source drive while the source potential moves with the switching node. Capturing the gate-to-source voltage (VGS) on the high-side MOSFETs via the IR2110 bootstrap driver and HCPL-3120 optocouplers proves the efficacy of the drive scheme. When the low-side MOSFET turns on, the bootstrap capacitor charges

rapidly to 15 VDC. When the high-side MOSFET is commanded to conduct, the driver successfully elevates the gate voltage to $V_{DC} + 15\text{ V} = +65\text{ V}$ relative to ground, maintaining a crisp 15 V differential across the gate-source junction. The observed switching transitions exhibit rise times (t_r) under 85 ns, minimizing switching power dissipation.

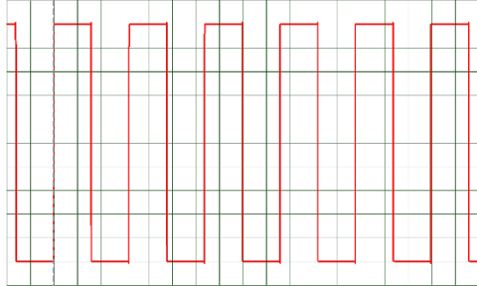


Figure 10: Full H-Bridge Simulation Results in Proteus Professional

3.6. Shoot-Through Prevention via Blanking Dead-Time Insertion

To eliminate the destructive risk of cross-conduction (where top and bottom MOSFETs in the same bridge leg conduct simultaneously due to turn-off propagation delays), a 300 μs blanking interval was evaluated.

During the 300 μs window where both gate drive signals are clamped to 0 V, the captured DC bus current trace drops down strictly to zero amperes. Without this blanking time, the simulation exhibits massive current spikes exceeding 45 A at every switching edge as the collapsing gate charge of the turning-off switch overlaps with the turn-on threshold of the incoming switch.

The inclusion of this 300 μs safety pause completely suppresses short-circuit current pulses, proving that hardware/signal dead-time insertion is an absolute prerequisite for ensuring long-term thermal stability and device survival in high-frequency inverter bridges.

4. CONCLUSION

This study presented a Proteus Professional co-simulation framework for the analysis and performance evaluation of fundamental DC-DC and DC-AC power-conversion topologies controlled by an Arduino Mega 2560. The implemented framework integrated the microcontroller control layer, gate-driver circuits, and non-ideal power stages within a common simulation environment. Buck, Boost, Four-Switch Non-Inverting Buck-Boost, Half-Bridge, and Full H-Bridge configurations were investigated under selected operating conditions, with particular attention given to PWM-based switching, component non-idealities, gate-driver operation, and dead-time protection.

The simulation results demonstrated clear differences between ideal analytical predictions and converter behavior when practical electrical parameters were introduced. The Buck converter achieved a steady-state output of approximately 24.04 V with a peak-to-peak output ripple of about 0.32 V, while maintaining continuous inductor current. The Boost converter showed a substantially reduced voltage gain compared with the ideal prediction, producing 29.16 V instead of the theoretically calculated 43.75 V. This difference demonstrated the influence of MOSFET on-state resistance, inductor series resistance, and diode forward-voltage drop on the achievable converter output. The Four-Switch Non-Inverting Buck-Boost converter maintained positive output polarity and demonstrated a continuous transition between Buck and Boost operating regions as the duty cycle was varied.

For the DC-AC conversion stages, the Half-Bridge produced an output of approximately $\pm 24.8\text{ V}$ from the 50 V DC bus, while the Full H-Bridge utilized the complete DC-link voltage and achieved a $\pm 50\text{ V}$ output swing. The Half-Bridge simulation also revealed low-frequency ripple at the capacitive midpoint under increased load current, demonstrating the influence of neutral-point stability on the converter output. In the Full H-Bridge, the implemented gate-driver configurations enabled high-side MOSFET switching, while the dead-time investigation showed that an appropriate blanking interval is essential for preventing simultaneous conduction of complementary switches. In the simulated test conditions, the introduction of a 300 μs dead-time eliminated the observed shoot-through current pulses that exceeded 45 A without the blanking interval.

Overall, the results demonstrate that microcontroller-based co-simulation can provide a useful pre-prototype stage for evaluating both control and power-stage behavior. The approach enables switching sequences, converter waveforms, selected non-ideal effects, and protection mechanisms to be examined under repeatable conditions before physical implementation. However, the results remain simulation-based and should not be interpreted as a complete substitute for experimental validation. The implemented models do not fully reproduce thermal self-heating, temperature-dependent semiconductor behavior, PCB parasitics, electromagnetic interference, measurement noise, or manufacturing tolerances. Therefore, physical prototype testing remains necessary to validate thermal performance, efficiency, electromagnetic behavior, and long-term switching reliability.

Future work will focus on transferring the developed simulation framework toward physical prototype implementation and on extending the digital control strategy beyond fixed or predefined switching conditions. In particular, closed-loop controller implementation using

PID or sliding-mode control, together with total harmonic distortion analysis under reactive and nonlinear loads, can provide a further basis for improving converter regulation and evaluating performance under more demanding operating conditions.

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