

DESIGN AND EXPERIMENTAL VALIDATION OF COMPACT NFC ANTENNA AND EMBEDDED SiP RFID MODULE BASED ON LTCC AND PCB TECHNOLOGIES

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ABSTRACT

This paper presents the design, fabrication, and experimental validation of compact NFC antenna structures and a miniaturized RFID module based on System-in-Package (SiP) integration. Planar spiral antennas operating at 13.56 MHz are implemented on LTCC and PCB substrates using two-layer and three-layer configurations. The influence of substrate material, geometry, and tuning strategy on inductance, resonance frequency, reflection coefficient, and Q -factor is experimentally evaluated using vector network analysis. A compact RFID module is subsequently realized using a cavity-based SiP architecture with face-down chip integration and anisotropic conductive film (ACF) interconnection. The results demonstrate that substrate selection and integration strategy significantly affect electrical performance, coupling efficiency, and miniaturization limits, providing a practical basis for the development of embedded SiP RFID/NFC modules.

Keywords: NFC antenna, RFID, LTCC, PCB, System-in-Package (SiP), miniaturization

1. INTRODUCTION

The ongoing digitalization of the economy and the transition toward Industry 4.0 and Industry 5.0 paradigms impose increasing demands on compact, energy-efficient, and reliable wireless identification systems. RFID (Radio Frequency Identification) and NFC (Near Field Communication) technologies represent key enabling solutions, as they provide contactless communication without requiring an internal power source on the tag side [1]–[3], [10]. Their application domains span logistics, smart cities, advanced manufacturing, healthcare, authentication, and IoT-based monitoring systems, as demonstrated in recent antenna and system-level studies [4], [6], [12]–[16].

High-frequency RFID systems operate in the globally standardized 13.56 MHz band defined by ISO/IEC 14443 and ISO/IEC 15693 standards [1]. Communication in this band relies on near-field inductive coupling between the reader and the transponder, providing stable and energy-efficient short-range operation. NFC technology, derived from HF RFID, is widely implemented in mobile, payment, and secure access devices, forming a mature and globally deployed ecosystem [2]. From a physical perspective, the overall system performance is strongly determined by antenna parameters, resonance tuning accuracy, and the efficiency of magnetic energy transfer between the reader and the tag [3], [10].

Passive NFC antennas are typically realized as planar spiral coils whose inductance, series resistance, parasitic capacitances, and quality factor Q directly influence resonance behavior, energy harvesting capability, and communication range [3], [8], [12], [13]. As antenna dimensions decrease, inductance is reduced while resistive and dielectric losses become more dominant. In addition, substrate-related parasitic effects and manufacturing tolerances increasingly affect resonance stability, making compact antenna design a coupled electromagnetic and technological optimization problem.

In parallel, modern microelectronic systems are increasingly implemented using System-in-Package (SiP) approaches, where active and passive components are integrated within multilayer substrates [5], [14], [16]. Such approaches enable significant miniaturization and improved functional density but introduce new challenges related to interconnection reliability, material compatibility, and process optimization [7]. LTCC (Low Temperature Co-fired Ceramics) technology provides a promising multilayer RF platform due to its stable relative permittivity, low dielectric losses, and compatibility with embedded passive structures [5], [9]. Alternatively, double-sided PCB substrates offer a technologically accessible and cost-efficient solution, albeit with higher dielectric losses and lower parametric stability.

This paper presents the design, fabrication, and experimental validation of NFC antenna structures and a miniaturized RFID module based on SiP integration. The work is structured into two complementary parts. The first part focuses on the development and characterization of NFC antennas implemented on LTCC and PCB substrates, enabling systematic comparison of geometry, substrate influence, and resonance tuning. The second part demonstrates the realization of a compact RFID module using a cavity-based SiP architecture with face-down chip integration and anisotropic conductive film (ACF) interconnection technology.

The main novelty of this work lies in the combined experimental investigation and system-level integration of compact NFC antennas within a System-in-Package (SiP) architecture using both LTCC and PCB technologies.

Unlike conventional studies that focus either on antenna design or packaging separately, this work provides a direct comparison of substrate materials (LTCC vs. PCB) under identical antenna geometries and operating conditions at 13.56 MHz. Furthermore, the paper demonstrates the practical implementation of a cavity-based SiP module with face-down chip integration using anisotropic conductive film (ACF), which enables a high level of miniaturization without conventional soldering.

The contribution is therefore not limited to antenna design, but extends to the experimentally validated integration strategy, including the interaction between antenna performance, substrate properties, and embedded packaging technology. This combined approach provides new insight into the trade-offs between miniaturization, electrical performance, and manufacturability in compact RFID/NFC modules.

To the best of the authors' knowledge, such a combined experimental comparison and integration approach for NFC antennas and embedded SiP RFID modules has not been comprehensively reported in recent literature.

2. DESIGN AND FABRICATION OF NFC ANTENNA STRUCTURES

The NFC antenna is designed as a planar spiral coil operating at the standardized frequency of 13.56 MHz. A square geometry is selected due to its efficient utilization of substrate area and its compatibility with rectangular chip placement and multilayer integration in compact SiP structures. Although circular geometries may provide slightly more uniform current distribution, square spirals offer better layout flexibility and integration potential within constrained module dimensions.

To mitigate current crowding and local electric field concentration associated with sharp 90° corners, the spiral layout incorporates locally rounded transitions. This design refinement improves current distribution uniformity and reduces additional AC resistance and parasitic capacitance effects, which are particularly important for miniaturized antenna configurations.

The antenna geometry is defined by a six-turn planar spiral structure with an outer dimension of 15 × 15 mm. For scaling analysis, a reduced variant with dimensions of 8 × 8 mm is also considered. The conductor width and spacing between adjacent turns are set to 200 μm and 300 μm, respectively, representing a compromise between manufacturability and electromagnetic performance. For the larger antenna variant, the estimated inductance is approximately 800 nH.

In the case of the smaller antenna (8 × 8 mm), the inductance decreases to approximately 300–350 nH due to the reduced loop area. Consequently, a higher tuning capacitance is required to achieve resonance at 13.56 MHz. This increase in capacitance leads to higher sensitivity to parasitic effects and component tolerances, which must be carefully considered during the design process.

Overall, the selected geometry represents a compromise between inductance, footprint, and integration capability within multilayer SiP architectures.

2.1. Analytical considerations and equivalent model

The designed planar spiral antenna can be approximated by an equivalent series RLC circuit, where the inductance is represented by the spiral coil, the resistance accounts for conductor and dielectric losses, and the capacitance includes both the tuning capacitor and parasitic contributions. The equivalent model enables estimation of the resonance frequency and quality factor of the antenna.

The inductance of the square planar spiral was estimated using standard analytical approximation models for spiral inductors, taking into account the number of turns, average diameter, and conductor geometry. For the proposed geometry, the inductance is approximately 800 nH for the 15 × 15 mm variant.

The resonance frequency is determined by the well-known relationship,

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

where L represents the antenna inductance and C is the total capacitance including both the tuning capacitor and parasitic components.

In LTCC technology, it is possible to implement an embedded planar capacitor within the multilayer structure. Although this approach was not experimentally realized in this work, it represents a potential method for achieving fully integrated antenna-resonator structures in future SiP implementations.

The electrical behavior of the NFC antenna can be described using the equivalent circuit shown in Fig. 1.

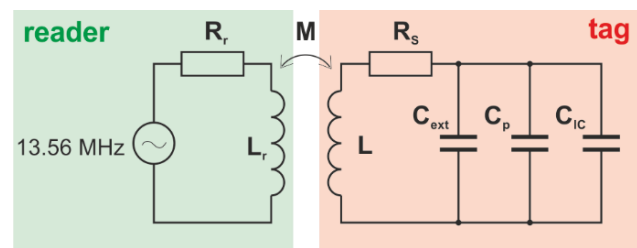
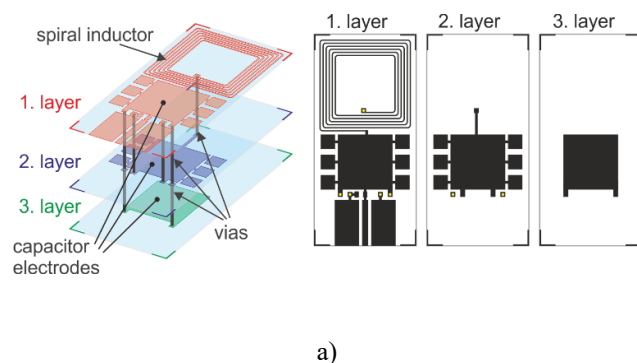


Fig. 1 Equivalent magnetically coupled circuit model of the NFC system including reader inductance L_r , tag inductance L , mutual inductance M , series resistances R_r , R_s and capacitive loading (C_{ext} , C_{IC} , C_p)

2.2. Fabrication on LTCC substrate

The first proposed NFC antenna concept is implemented as a three-layer multilayer ceramic structure based on LTCC technology, as illustrated in Fig. 2(a). The corresponding two-layer alternative with an external tuning capacitor is shown in Fig. 2(b). These architectures form the basis for experimental verification of multilayer NFC antenna configurations.



a)

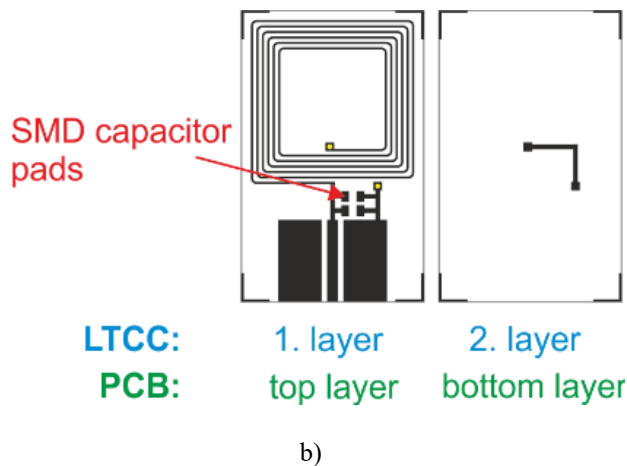


Fig. 2 Proposed NFC antenna architectures: (a) three-layer LTCC structure with embedded planar capacitor and via interconnections; (b) two-layer implementation with external SMD tuning capacitor

The LTCC antennas were fabricated using DuPont Green Tape 951PT ceramic material with a relative permittivity of $\epsilon_r \approx 8.7$. Conductive patterns were realized using silver-based paste, while interlayer electrical connections were formed by metallized vias filled with conductive paste.

The fabrication process followed a standard LTCC processing sequence, including via formation and filling, screen printing of conductive patterns, stacking of individual layers, isostatic lamination, and co-firing. During the co-firing process, the LTCC material exhibits shrinkage of approximately 12–13% in the X–Y plane, which was taken into account during the design stage by appropriate geometrical compensation.

For selected antenna variants, an embedded multilayer planar capacitor was integrated directly into the LTCC stack. This approach enables internal tuning of the resonance frequency and reduces the dependence on external SMD components, thereby improving integration capability and making the structure more suitable for future SiP implementations.

The fabricated antenna samples used for experimental evaluation are shown in Fig. 3. In addition to antenna test structures, selected samples also incorporate cavity features intended for subsequent integration of electronic components within a SiP architecture.

The fabricated antenna samples were categorized into four main types (A–D), as summarized in Table 1. Fig. 3 presents representative fabricated samples and technological realizations corresponding to these antenna categories, although not all variants are shown individually. The classification is based on antenna geometry, size, and integration approach, including variants with and without integrated capacitive structures.

The fabricated antenna samples are identified using a combined designation system consisting of the antenna type, variant number, and substrate technology. The first letter (A–D) denotes the antenna geometry and integration concept described in Table 1. The numerical index distinguishes different implementations or layout modifications within the same antenna category, while the suffix indicates the substrate material (LTCC or PCB). For example, sample A/LTCC represents the first

implementation of the standard antenna geometry fabricated on LTCC substrate.

The geometrical and material parameters of the fabricated NFC antenna structures are summarized in Table 2.

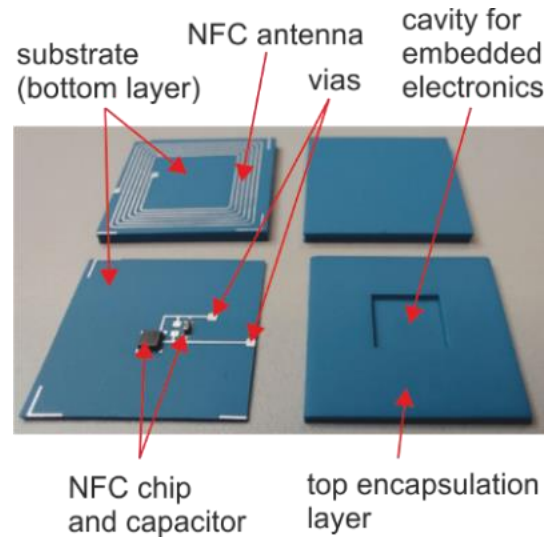


Fig. 3 Fabricated LTCC-based NFC antenna samples and cavity structures prepared for experimental evaluation and subsequent SiP integration. The presented samples illustrate different antenna dimensions and technological realizations described in Table 1

Table 1 Classification of fabricated antenna samples

Type	Size	Description	Substrate
A	15 × 15 mm	Standard spiral antenna	LTCC, PCB
B	15 × 15 mm	Antenna with embedded capacitor	LTCC only
C	8 × 8 mm	Miniaturized antenna	LTCC, PCB
D	8 × 8 mm	Miniaturized antenna with central integration area	LTCC, PCB

Table 2 Geometrical and substrate parameters of fabricated NFC antennas

Sample	Substrate	Size [mm]	Layers	ϵ_r	L [nH]
A/LTCC	LTCC	15 × 15	3	8.7	~800
B/LTCC	LTCC	15 × 15	3	8.7	~800
A/PCB	PCB	15 × 15	2	4.2–4.6	~800
C/PCB	PCB	8 × 8	2	4.2–4.6	300–350
D/LTCC	LTCC	8 × 8	3	8.7	300–350

Although several antenna variants (A–D) were fabricated and experimentally evaluated, only selected representative samples are discussed in detail in this paper. The selection was based on their relevance to the proposed SiP integration concept and their suitability for reliable experimental comparison. In particular, antennas with

dimensions of 15×15 mm were chosen for further analysis, as smaller variants (8×8 mm) exhibited significantly weaker inductive coupling and reduced energy transfer under standard measurement conditions. Other variants, including antennas with integrated capacitive structures or modified geometries, are considered supplementary and are not analyzed in detail to maintain clarity and focus of the presented results.

Samples of type A represent standard antenna structures with dimensions of 15×15 mm, while type B corresponds to LTCC-based antennas with an embedded planar capacitor. Types C and D represent miniaturized variants (8×8 mm), where type D additionally enables placement of the electronic components within the antenna area.

For clarity, individual samples are denoted using a combined notation indicating geometry and substrate, for example A/LTCC or C/PCB.

2.3. Fabrication on PCB substrate

For comparison purposes, NFC antenna structures were also implemented on double-sided PCB substrates. The fabrication was carried out using FR4-based material PCL370HR with a substrate thickness in the range of approximately 150–300 μm and copper thickness of 18 μm .

The antenna geometry was kept identical to the LTCC implementation in order to enable a direct comparison of electrical and technological properties. The planar spiral coil was realized on the top copper layer, while the bottom layer was used for routing and interconnection of the tuning capacitor and measurement pads.

The PCB fabrication process involved several standard steps, including pattern definition by photolithographic etching or CNC milling, drilling of via holes with typical diameters of 300–400 μm , via filling using conductive polymer paste, and subsequent curing of the conductive material. The final assembly of the antenna structure was completed by mounting SMD capacitors using solder paste followed by a reflow process.

Compared to LTCC technology, PCB fabrication offers a simpler and more cost-effective approach with higher flexibility in rapid prototyping. However, the lower dielectric permittivity and higher dielectric loss tangent of FR4 materials influence the electromagnetic performance of the antenna, particularly in terms of Q-factor and resonance stability.

The PCB-based antennas therefore serve as a reference solution for evaluating the influence of substrate material and fabrication technology on antenna performance and miniaturization capability.

2.4. Measurement and characterization of NFC antenna structures

The fabricated NFC antennas, whose layouts are shown in Fig. 4, were experimentally characterized using a vector network analyzer (Keysight PNA-L N5231A, 300 kHz–13.5 GHz). The evaluation focused on determining the inductance, resonance frequency, reflection coefficient S_{11} , and quality factor Q.

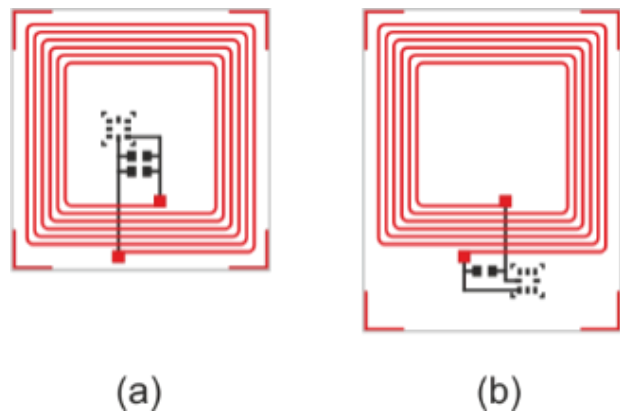


Fig. 4 Layout of the designed NFC antenna structures: (a) antenna with integrated central component area; (b) antenna without central integration

The inductance of the antenna coil was first determined from impedance measurements at the target frequency of 13.56 MHz. The corresponding Smith chart representation is shown in Fig. 5. The measured inductance for the LTCC antenna sample A.1 was approximately 829.6 nH, which is in good agreement with the design values.

Based on the measured inductance, the required tuning capacitance was calculated to achieve resonance at 13.56 MHz. Suitable capacitor values were selected from standard E-series components and implemented using SMD technology.

The resonance condition was verified experimentally using Smith chart analysis, where resonance corresponds to a purely real impedance ($\text{Im}\{Z\} = 0$). The measured result is shown in Fig. 6. After tuning, the resonance frequency for the LTCC antenna sample A.1 was approximately 13.536 MHz.

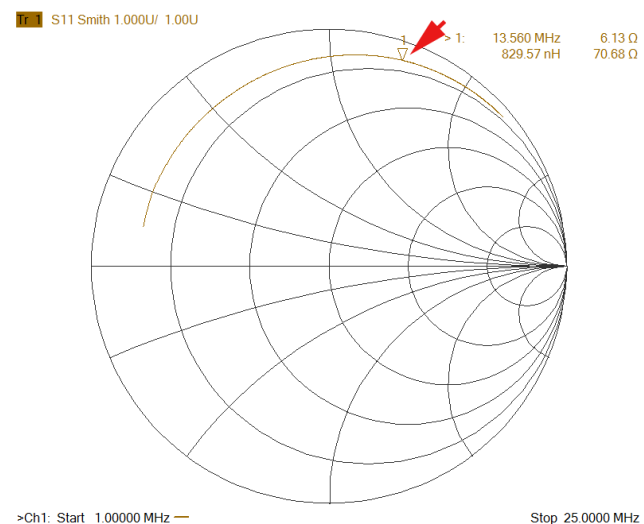


Fig. 5 Smith chart representation of measured impedance showing inductive behavior of the LTCC antenna at 13.56 MHz (LTCC sample A.1, $L \approx 829$ nH)

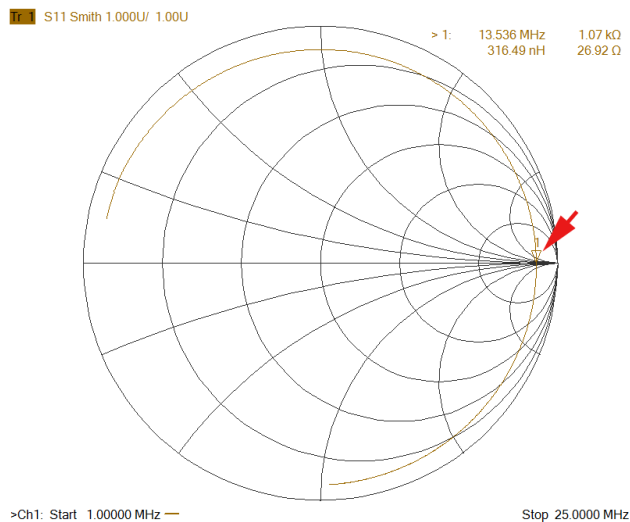


Fig. 6 Smith chart verification of resonance condition ($\text{Im}\{Z\} = 0$) for the LTCC antenna after tuning (LTCC sample A.1, $f_0 \approx 13.536$ MHz)

In addition to impedance analysis, the antennas were evaluated in reflection mode using the reflection coefficient S_{11} . A single-port measurement setup with a coupling loop was used to provide non-contact excitation of the antenna. The antenna under test was gradually positioned relative to the coupling loop, and the resonance behavior was observed through variations in the reflection coefficient.

The influence of antenna geometry on coupling efficiency is illustrated in Fig. 7. For clarity, only selected representative antenna variants are shown in Fig. 7. These were chosen based on their relevance to the comparative analysis and their stable and repeatable measurement behavior. Other fabricated variants exhibited weaker coupling or less consistent results and are therefore not included in this figure to maintain readability of the presented data. The results show that antennas with smaller dimensions (8×8 mm) exhibit a shallower minimum of the reflection coefficient S_{11} compared to larger antennas (15×15 mm). This indicates reduced inductive coupling due to lower mutual inductance, resulting in weaker energy transfer. In contrast, larger antennas demonstrate stronger coupling and a more pronounced resonance dip.

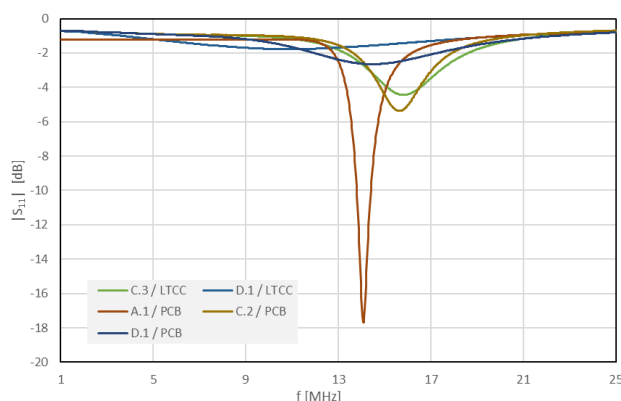


Fig. 7 Comparison of measured reflection coefficient S_{11} for selected NFC antennas geometries (15×15 mm and 8×8 mm) according to the sample designation system described in the text

The measured results further indicate that PCB-based antennas exhibit higher Q-factor values compared to LTCC implementations. This behavior is primarily attributed to lower conductor losses in copper layers compared to silver-based conductive pastes used in LTCC technology. On the other hand, LTCC structures offer improved integration capability and mechanical stability, which are essential for future SiP-based module development.

Overall, the experimental characterization confirms the expected trade-offs between antenna geometry, substrate material, and electromagnetic performance. The obtained results provide a reliable basis for the subsequent development of compact RFID modules based on SiP integration.

3. DEVELOPMENT OF SiP RFID MODULE

The following discussion combines antenna-level measurements and system-level SiP validation.

3.1. SiP concept and architecture

The SiP module concept is directly based on the cavity structures introduced in the fabricated antenna samples (Fig. 2), which were further developed to enable embedded component integration.

The second part of this work focuses on the development of a compact RFID/NFC module based on System-in-Package (SiP) integration. The objective is to demonstrate the feasibility of integrating the NFC antenna, chip, and passive components into a single multilayer structure while achieving a high level of miniaturization and functional integration.

The proposed module operates at 13.56 MHz and implements a passive RFID/NFC tag. The design is based on a cavity-type architecture, in which the electronic components are embedded inside the substrate. This approach enables reduction of the module thickness, improved mechanical protection, and shorter electrical interconnections.

Two layout configurations were investigated. In the first configuration, the NFC chip is positioned within the central area of the antenna coil, enabling a compact layout with minimal footprint. In the second configuration, the chip is placed outside the coil region in order to reduce potential electromagnetic interference and mutual coupling effects.

The concept of the proposed SiP module is illustrated in Fig. 8.

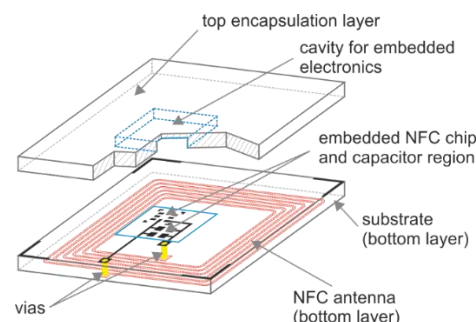


Fig. 8 Concept of the embedded SiP RFID module based on cavity structures introduced in Fig. 3, showing face-down chip integration and multilayer encapsulation

3.2. Materials and substrate technologies

Two substrate technologies were considered for the realization of the SiP module, namely LTCC ceramic (DuPont Green Tape 951PT) and PCB-based materials (PCL370HR prepregs). These materials were selected to enable a direct comparison between ceramic and polymer-based multilayer structures.

The LTCC technology provides stable dielectric properties, low loss tangent, and the possibility of embedding passive components directly into the multilayer structure. In contrast, PCB-based substrates offer a simpler and more cost-effective fabrication process, as well as higher flexibility in rapid prototyping. However, they exhibit higher dielectric losses and lower long-term stability compared to LTCC materials.

3.3. Face-Down integration using ACF technology

To achieve a high level of miniaturization and eliminate conventional solder-based interconnections, a face-down integration approach was employed. The NFC chip (NT3H2111W0, XQFN8 package) was placed inside a cavity with its contact pads facing the substrate.

Electrical interconnection was realized using anisotropic conductive film (ACF), specifically Anisolm AC-7206U-18. This technology enables vertical electrical conduction while maintaining lateral insulation, which is essential for fine-pitch interconnections in compact SiP structures.

Compared to traditional soldering, the ACF-based approach significantly reduces thermal stress during assembly and allows integration within multilayer structures without exposing the components to high temperatures.

3.4. Cavity structure and SiP module design

The SiP module is based on a multilayer architecture incorporating a cavity for embedding the electronic components. The antenna is implemented on the outer layer of the substrate, while the NFC chip and passive components are located within the cavity region.

The cavity is formed either during LTCC layer stacking or by mechanical processing (e.g., CNC milling) in PCB substrates. After placement, the chip is fixed and electrically connected using ACF technology, and the structure is subsequently encapsulated or laminated.

This approach results in a compact and mechanically robust module with reduced interconnection length and improved integration density. The proposed architecture also provides a scalable platform for further integration of additional functional elements, such as sensors.

3.5. Fabrication process of the SiP RFID module

The fabrication of the proposed SiP RFID module is based on a sequence of processes combining antenna realization, cavity preparation, component integration, and final encapsulation. The overall technological workflow is illustrated in Fig. 9.

Initially, the multilayer substrate with predefined conductive interconnections is fabricated using either LTCC or PCB technology. In the case of PCB substrates,

standard subtractive processes such as photolithographic etching or CNC milling are employed to define the antenna geometry and interconnection structures. For LTCC-based implementations, the process involves screen printing of conductive patterns, via formation, multilayer stacking, and co-firing.

Subsequently, a cavity is created within the substrate to accommodate the NFC chip and passive components. In PCB-based structures, the cavity is formed by mechanical milling, while in LTCC technology it is defined during the layer structuring process. The cavity dimensions are designed to ensure precise placement of the components and to minimize mechanical stress during subsequent processing steps.

The NFC chip is then positioned in a face-down configuration inside the cavity, with its contact pads oriented toward the substrate. Electrical interconnection is realized using anisotropic conductive film (ACF), which enables vertical electrical conduction while maintaining lateral insulation. The bonding process is carried out under controlled thermo-compression conditions, ensuring reliable electrical contact without the need for high-temperature soldering.

After establishing the electrical interconnection, an adhesive layer is applied to improve mechanical stability and to fix the components within the cavity. This step is followed by encapsulation or lamination of the structure, resulting in a compact and mechanically robust SiP module.

The described process flow represents a low-temperature integration approach that is particularly suitable for multilayer SiP structures combining different materials, such as ceramics and polymer-based substrates. Compared to conventional assembly techniques, the proposed method reduces thermal stress, shortens interconnection paths, and enables a higher level of integration within a limited footprint.

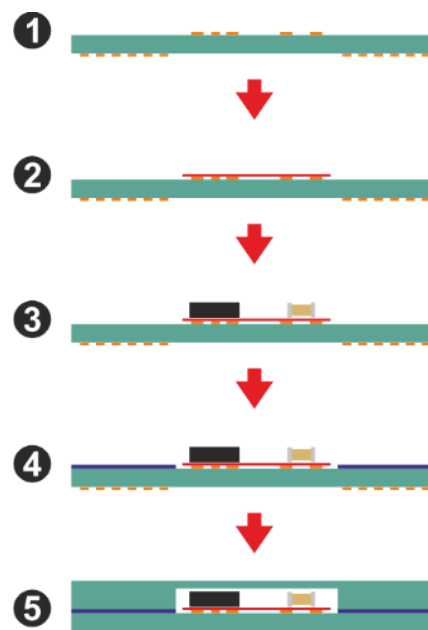


Fig. 9 Technological process flow of the SiP RFID module fabrication: (1) substrate preparation with conductive interconnections, (2) ACF application, (3) face-down chip and component integration, (4) adhesive application, and (5) encapsulation

The proposed fabrication approach is compatible with scalable manufacturing processes and provides a practical pathway toward industrial implementation of embedded RFID/NFC modules.

3.6. Functional verification and discussion

The fabricated SiP modules were evaluated in terms of resonance behavior, coupling efficiency, and integration feasibility. The results indicate that the proposed architecture enables successful operation at 13.56 MHz even with embedded components.

The use of ACF technology provided reliable electrical interconnection without the need for high-temperature soldering. The placement of the chip inside the cavity did not prevent proper antenna operation, although it introduced additional parasitic effects that must be considered in the design phase.

PCB-based modules exhibited higher Q-factor values due to lower conductor resistance, while LTCC structures demonstrated superior integration capability and mechanical stability. The comparison confirms that the selection of substrate and integration methods significantly affects both electrical performance and manufacturability.

Overall, the proposed SiP module demonstrates the feasibility of compact RFID/NFC integration and provides a foundation for further development of embedded electronic systems for digitalization applications.

4. RESULTS AND DISCUSSION

PCB antennas achieved Q-factor values of approximately 5.9–6.3, compared to 3.5–5.1 for LTCC structures (Table 3).

Table 3 Summary of measured electrical parameters of selected NFC antennas

Sample	Substrate	L [nH]	f_0 [MHz]	Q
A.1/LTCC	LTCC	829.6	13.536	3.5–5.1
A.1/PCB	PCB	~800	~13.56	5.9–6.3
C/PCB	PCB	300–350	~13.56	< 3
D/LTCC	LTCC	300–350	~13.56	< 3

The geometrical and substrate-related parameters of the corresponding antenna structures are summarized in Table 2. For qualitative comparison of coupling behavior and reflection coefficient characteristics, see Fig. 7. Table 3 clearly demonstrates the trade-off between antenna miniaturization and electromagnetic performance. Larger 15×15 mm antennas provide stronger coupling and higher inductance, whereas miniaturized 8×8 mm structures exhibit reduced mutual coupling and lower Q-factor. The comparison also confirms that PCB-based antennas achieve higher Q-factor values, while LTCC structures provide superior integration capability for SiP implementation.

The experimental results obtained from the fabricated NFC antenna structures and SiP RFID modules enable a comprehensive evaluation of the influence of substrate materials, antenna geometry, and integration approach on the overall system performance.

Although multiple antenna variants (A–D) were fabricated and experimentally evaluated, only selected representative samples are discussed in detail. The selection was based on their relevance to the proposed SiP integration concept and their suitability for reliable comparison.

A comparison between LTCC and PCB-based antennas reveals distinct differences in electrical performance and integration capability. PCB antennas fabricated on FR4 (PCL370HR) exhibit higher Q-factor values compared to LTCC implementations, primarily due to the lower conductor resistance of copper traces. In contrast, LTCC structures utilize silver-based conductive pastes with higher sheet resistance, which leads to increased losses. However, LTCC antennas offer superior integration potential, enabling the realization of embedded passive components and compact multilayer architectures. In addition, LTCC technology provides improved mechanical stability and is better suited for SiP integration, making it advantageous for highly integrated systems despite its lower Q-factor.

The influence of antenna geometry is clearly reflected in the measured results. Larger antennas with dimensions of 15×15 mm exhibit higher inductance values, typically in the range of 800–830 nH, and stronger inductive coupling. This results in deeper minimum in the reflection coefficient S_{11} and more efficient energy transfer. In contrast, smaller antennas with dimensions of 8×8 mm show significantly reduced inductance, approximately 300–350 nH, due to the reduced loop area. Consequently, these antennas exhibit weaker coupling and a shallower S_{11} response, indicating reduced energy transfer capability. These findings confirm that antenna miniaturization introduces a fundamental trade-off between compact size and electromagnetic efficiency.

The measured Q-factor values further highlight the dependence on substrate material and fabrication technology. PCB-based antennas achieve Q-factor values in the range of approximately 5.9–6.3, while LTCC antennas exhibit lower values between 3.5 and 5.1. This difference can be attributed to higher conductor losses in LTCC structures, thinner conductive layers, and additional dielectric and process-related losses. Despite this, LTCC remains a strong candidate for integrated applications where compactness and structural stability are more critical than maximizing Q-factor.

The reflection coefficient measurements provide additional insight into the effect of antenna size on coupling behavior. Larger antennas demonstrate stronger coupling with the excitation loop, resulting in a more pronounced S_{11} dip at resonance. Conversely, smaller antennas exhibit weaker coupling due to reduced mutual inductance, leading to a less pronounced resonance response. This behavior is consistent with theoretical expectations and confirms the importance of loop area in determining coupling efficiency.

The integration of the NFC chip into the SiP module demonstrates the feasibility of embedding active components within the substrate while maintaining functional antenna performance. The proposed cavity-based architecture with face-down chip integration and ACF interconnection enables significant miniaturization and reduction of interconnection length. Compared to conventional surface-mounted solutions, the SiP approach provides improved mechanical protection of the chip,

reduced module height, and increased integration density. However, the embedded configuration introduces additional parasitic effects, which may influence resonance tuning and coupling behavior. It was observed that placing the chip outside the antenna coil region can reduce potential electromagnetic interference and improve system stability.

Overall, the experimental results confirm that both substrate selection and integration strategy significantly influence the electrical and technological performance of NFC antenna systems. PCB-based antennas provide higher Q-factors and lower losses, making them suitable for performance-oriented designs, while LTCC-based structures offer superior integration capability and are more suitable for advanced SiP implementations. The presented results highlight the inherent trade-offs between miniaturization, efficiency, and integration complexity, and demonstrate a practical pathway toward compact RFID/NFC modules for digitalization applications.

In comparison with recent literature, the proposed approach combines antenna miniaturization with cavity-based SiP integration and experimental validation using both LTCC and PCB technologies. Recent studies mainly focus either on antenna optimization or on packaging technologies separately, whereas the presented work experimentally evaluates the interaction between antenna geometry, substrate material, and embedded integration strategy within a unified platform.

The achieved resonance stability at 13.56 MHz and successful operation of the embedded module confirm the feasibility of the proposed SiP concept for compact RFID/NFC applications. In comparison with conventional surface-mounted approaches, the proposed architecture reduces interconnection length and enables higher integration density. The use of ACF interconnection additionally provides a low-temperature assembly solution suitable for multilayer embedded systems.

Although the measured Q-factor values are moderate compared to larger standalone NFC antennas reported in literature, the obtained results demonstrate a practical trade-off between miniaturization, manufacturability, and integration capability. The presented approach therefore represents a practically applicable solution for future embedded RFID/NFC systems and smart integrated modules.

5. CONCLUSION

This paper presented the design, fabrication, and experimental validation of compact NFC antenna structures and a miniaturized RFID module based on System-in-Package (SiP) integration. The study combined antenna-level analysis with system-level integration, providing a comprehensive evaluation of both electromagnetic performance and technological feasibility.

The experimental results confirmed that antenna geometry and substrate material significantly influence key parameters such as inductance, resonance frequency, reflection coefficient, and quality factor. Larger antenna structures provide stronger inductive coupling and improved energy transfer, while miniaturized configurations introduce increased sensitivity to parasitic effects and component tolerances.

The comparison between LTCC and PCB technologies demonstrated that PCB-based antennas achieve higher Q-factor due to lower conductor losses, whereas LTCC structures offer superior integration capability and mechanical stability.

The proposed SiP module based on a cavity architecture with face-down chip integration and ACF interconnection demonstrated the feasibility of embedding active and passive components within a multilayer substrate. This approach enables significant reduction of module size, improved mechanical protection, and increased integration density. At the same time, the results indicate that careful consideration of parasitic effects and component placement is required to maintain stable resonance behavior in compact structures.

The proposed approach therefore demonstrates a viable pathway toward industrial implementation of compact SiP-based RFID modules.

Overall, the presented work provides a practical and experimentally validated pathway toward the development of miniaturized RFID/NFC modules based on SiP technology. The combination of LTCC and PCB approaches offers a flexible framework for optimizing the trade-off between electrical performance, manufacturability, and integration level. Future work will focus on further optimization of embedded interconnections, reliability analysis, and scaling of the proposed architecture toward fully integrated smart modules for advanced digitalization applications.

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