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Design and analysis of a single-stage cascode LNA for S-band application in 180-nm CMOS technology

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This paper presents a high-gain, single-stage cascode low noise amplifier (LNA) tailored for S-band applications, implemented in a 180-nm CMOS process. The design employs a common-source cascode topology with inductive degeneration, enabling a careful trade-off between gain, noise figure, and input matching. Schematic simulations indicate a peak gain of 53.2 dB and a low noise figure of 1.51-1.74 dB across the S-band, with excellent impedance matching. The amplifier is unconditionally stable and occupies a compact core area of only 0.175 mm². Operating with a power consumption of 45 mW, these results demonstrate that the proposed LNA provides a competitive, area-efficient, and robust solution for modern S-band wireless systems, achieving performance levels comparable to more complex multi-stage architectures while maintaining simplicity and design efficiency. The design also achieves excellent reverse isolation ($S_{12} < -48$ dB), output matching ($S_{22} = -12.75$ dB), and unconditional stability ($K > 1$), further demonstrating the robustness of the proposed LNA.

Keywords: low noise amplifier (LNA), GPS, CMOS, cascode, single-stage, inductive degeneration, noise figure, process corners

1 Introduction

The demand for high-performance wireless communication systems operating in the S-band has surged. In particular, the lower S-band (1-3 GHz) is widely used for satellite communication, radar, and modern IoT applications, making it a highly relevant frequency range for low-noise front-end design driven by applications in satellite communication, radar, IoT, and modern wireless devices. A critical bottleneck in these systems is the amplification of weak RF signals at the receiver frontend without significantly degrading the signal-to-noise ratio (SNR). The Low Noise Amplifier (LNA), as the first active component, is paramount in defining the overall receiver noise performance and sensitivity [1-2].

Key LNA specifications for S-band applications include high gain to suppress downstream noise, a minimal noise figure (NF) to preserve SNR, and precise input matching (typically to 50 Ω) for maximum power transfer. Additionally, power efficiency and compact physical size are crucial for practical systems. While multi-stage LNAs can achieve very high gain, they often do so at the cost of increased power consumption, design complexity, and larger chip area [3-4]. Consequently, achieving high performance within a single amplification stage presents a significant and valuable design challenge.

The advancement of CMOS technology has enabled the integration of high-frequency RF circuits with digital basebands on a single chip, offering benefits in cost, power consumption, and form factor. Modern submicron nodes like 180nm CMOS provide transit frequencies f_T in the GHz range, making them suitable for S-band LNA design [5]. However, designers must navigate inherent trade-offs between gain, NF, linearity, and power consumption [6].

This work demonstrates that a meticulously optimized single stage LNA is sufficient to meet the stringent requirements of S-band applications. We present a common-source cascode topology with inductive degeneration, engineered for operation across the S-band. The cascode structure offers high gain and superior reverse isolation, mitigating the Miller effect, while inductive degeneration provides a real impedance component for simplified input matching and low noise operation [7].

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The primary contribution of this paper is the demonstration of a single-stage LNA that achieves a high gain exceeding 50 dB and a noise figure below 2 dB with a compact and power-efficient architecture. The design's robustness is verified through comprehensive schematic simulations and detailed process corner analysis (FF, SS, SF, FS), confirming its viability for industrial fabrication. The following sections detail the design methodology, present and discuss the simulation results, and provide a comparison with recent works.

2 Circuit design and implementation

This section details the design of the single-stage Low Noise Amplifier (LNA), optimized for S-band operation in a 180 nm CMOS process. The design focuses on achieving high gain and a low noise figure within a single amplification stage through careful selection of topology, device sizing, and matching networks.

2.1 Topology selection: Cascode with inductive degeneration

The common-source cascode topology was selected as the core of the single-stage LNA. This structure is favoured for its ability to provide high gain, good reverse isolation, and wide bandwidth. All critical for S-band applications, without requiring additional cascaded stages. The cascode configuration mitigates the Miller effect, reducing the feedback from the output to the input and thereby enhancing stability and high-frequency performance.

Inductive source degeneration is employed to achieve two primary objectives: 1) to generate a real part in the input impedance for straightforward matching to the 50 sources, and 2) to optimize the amplifier for minimum noise figure. This approach allows the single-stage design to meet the stringent gain and noise requirements of S-band front-ends.

2.2 Design equations and frequency of operation

The amplifier is designed for operation within the lower S-band (1-3 GHz) range, which represents the most critical segment for many practical communication and radar systems. The 180-nm CMOS technology node offers a suitable trade-off between RF performance, power consumption, and integration capability.

The transconductance g_m of the input common-source transistor M_1 is the key parameter determining gain and noise performance. It is given by:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DS}} \tag{1}$$

The voltage gain of the cascode stage is approximated by:

$$A_V \approx -g_{m1}.(r_{01} \| r_{02}) \approx -g_{m1}.r_{01} \tag{2}$$

where r_{o1} and r_{o2} are the output resistances of M_1 and M_2, respectively.

The input matching network, comprising the gate inductor (L_g) and the source degeneration inductor (L_s), is designed to provide a 50 Ω input impedance at resonance. The real part of the input impedance is given by:

$$\Re\{Z_{in}\} \approx \frac{g_{m1} L_s}{C_{gs}} \tag{3}$$

which is set equal to 50 Ω. The resonant frequency is set by the tank circuit formed by L_g and the total gate capacitance:

$$\omega_0 = \frac{1}{\sqrt{L_g C_{gs}}} \tag{4}$$

The noise figure (NF) is minimized by optimizing the drain current and the width of the input transistor. The simplified NF expression is:

$$NF \approx 1 + \frac{\gamma \omega_0}{\alpha \omega_T} + \frac{\gamma}{g_m R_s} \tag{5}$$

where γ is the noise coefficient, $\alpha = g_m/g_{d0}$, and ω_T is the transition frequency.

2.3 Circuit implementation and component sizing

The finalized single-stage LNA schematic is shown in Fig. 1. The core consists of the cascode pair (M_1, M_2). Transistor M_3 and resistor R_2 form a simple current mirror to provide a stable bias current. The input matching network includes the off-chip gate inductor L_g (L_1=7.8 nH) and the integrated source degeneration inductor L_s (L_2=600 pH). The load is a parallel LC tank (L_3=2.5 nH, C_2=2 pF) tuned for S-band operation, providing a high impedance load to maximize gain.

DC blocking capacitors C_1, C_2 are used at the input and output. The design parameters, obtained through iterative simulation for optimal performance, are summarized in Table 1.

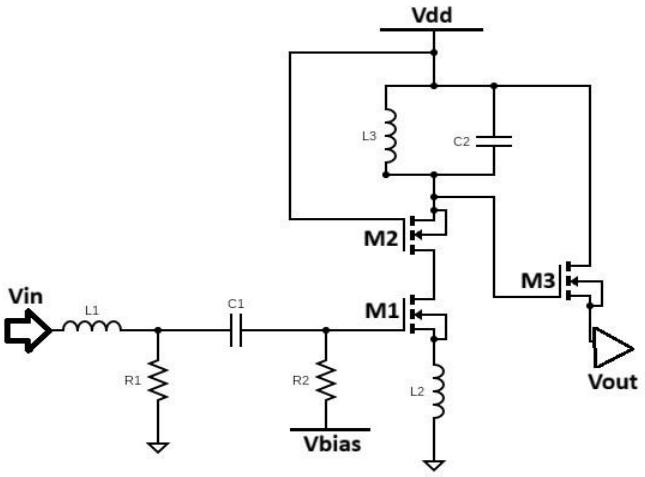


Fig. 1. Schematic of the proposed single-stage cascode LNA

Table 1. Design parameters of the proposed single-stage LNA

Transistor	Passive device	
M1, M2 540 µm/0.18 µm	L1 (Gate)	7.8 nH
M3 (Bias) 70 µm/0.18 µm	L2 (Source)	600 pH
	L3 (Tank)	2.5 nH
	C1 (Input)	1.5 pF
	C2 (Tank)	2 pF
	R1	1 kΩ
	R2	10 kΩ
	V_{bias}	0.6 V

2.4 Layout implementation

The layout of the single-stage LNA was implemented with a strong emphasis on minimizing parasitic resistance and capacitance to preserve high-frequency performance. Symmetry and careful placement were used to ensure stability. The integrated spiral inductors L_2, L_3 were designed and characterized using EM simulation tools. The final layout, shown in Fig. 2, occupies a compact core area of 0.175 mm². The design successfully passed all Design Rule Check (DRC) and Layout vs. Schematic (LVS) verification steps, ensuring its readiness for fabrication.

3 Simulation results and discussion

The proposed single-stage LNA was simulated in Cadence Virtuoso. Post-layout simulations, including extracted parasitic and process corner analysis, were performed to evaluate the amplifier's performance. The results confirm that the design meets all key requirements while maintaining the efficiency of a single amplification stage.

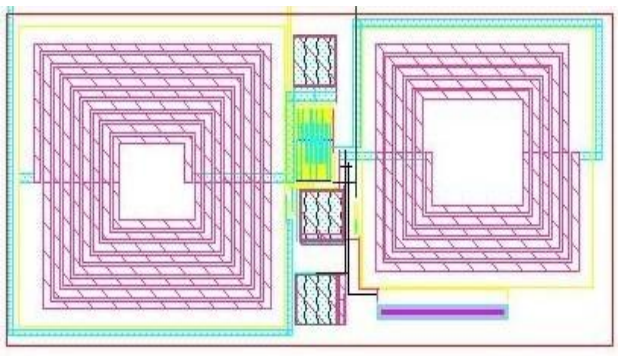


Fig. 2. Layout of the proposed single-stage LNA

3.1 Performance summary

The LNA achieves the following key performance metrics across the S-band:

- Power gain (S_{21}, forward transmission coefficient) 53.23 dB (peak)
- Noise figure (NF): 1.51-1.74 dB
- Input reflection coefficient (S_{11}): –42 to –5 dB
- Reverse isolation (S_{12}): < –48 dB
- Output reflection coefficient (S_{22}): –12.75 dB
- Power consumption: 45 mW (1.8 V supply)
- Stability factor (Kf): > 1 (unconditionally stable)

The simulated output return loss of S_{22} = −12.75 dB corresponds to a reflection coefficient magnitude of $|\Gamma|=10^{(-12.75/20)} \approx 0.23$, which implies that approximately $|\Gamma|^2 \approx 0.23^2 \approx 0.053$ (≈5.3%) of the output power is reflected back toward the amplifier. The associated voltage standing wave ratio (VSWR) is $(1+|\Gamma|)/(1-|\Gamma|) \approx (1+0.23)/(1-0.23) \approx 1.6$. In many practical S-band receiver front-end applications, an S_{22} better than −10 dB is considered acceptable; therefore, the measured S_{22} of −12.75 dB indicates satisfactory output matching for typical 50 Ω system interfaces. If stricter output matching is required for a particular system, S_{22} can be improved by adding a short on-chip or off-chip matching network (at the cost of some added insertion loss and area), or by inserting an output buffer/isolation stage to the LNA. We chose to optimize input matching, noise figure, and single-stage gain in this design; the present S_{22} represents a balanced trade-off consistent with the design goals.

3.2 S-parameters and noise figure

The noise figure performance is shown in Fig. 3. The amplifier achieves a minimum NF of 1.4 dB, enabled by careful transistor sizing, biasing, and inductive degeneration.

Figures 4a-4d show the S-parameter results. The input return loss S_{11} indicates excellent input matching to the 50 Ω source. The forward gain S_{21} peaks at 53.23 dB. Reverse isolation S_{12} remains below –48 dB across the band, ensuring stability. Output matching S_{22} is –12.75 dB.

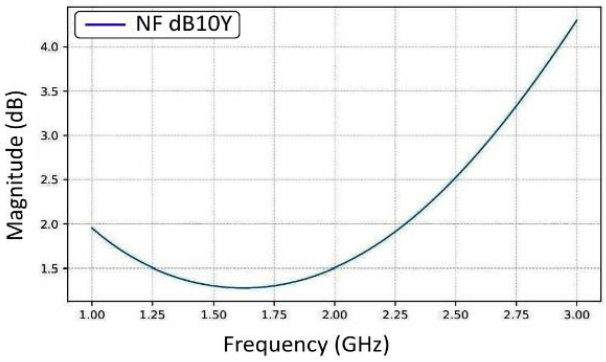


Fig. 3. Noise figure (NF) of the proposed LNA (typical corner)

3.3 Variation across process corners

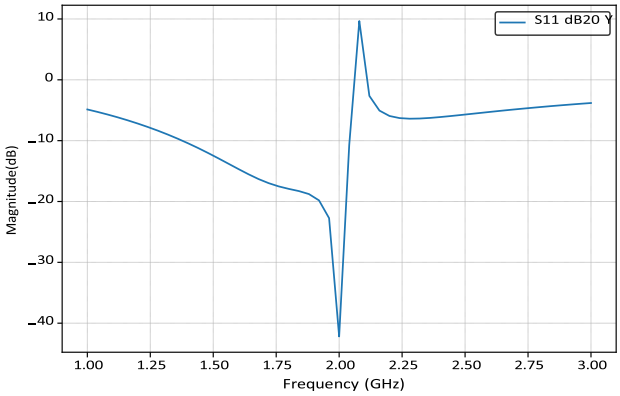
The S-parameters and noise figure were simulated across five process corners: TT, FF, SS, FS, and SF. Figures 5a-5e illustrate the performance stability.

3.4 Stability

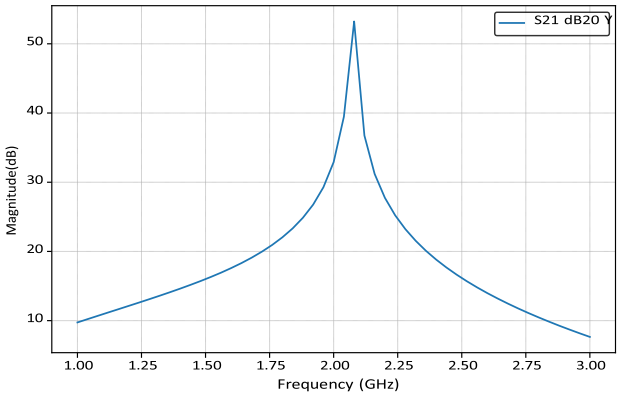
Rollett's stability factor K was calculated and found to be greater than 1 with positive auxiliary factor β across the frequency band, confirming unconditional stability for all process corners.

3.5 Process corner analysis summary

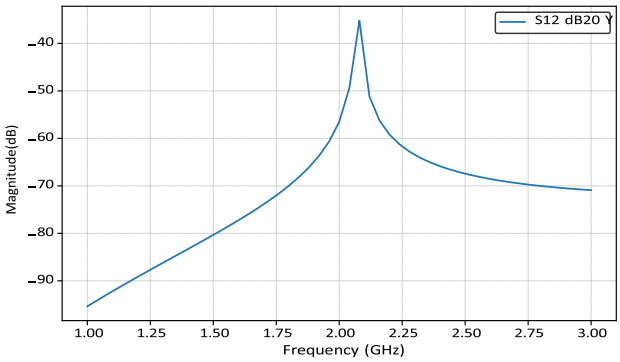
The quantitative corner performance is summarized in Table 2. The LNA demonstrates robust gain, low NF, and adequate input matching across all corners as shown in Fig. 5. The significant gain variation observed, notably from 53.23 dB (TT) to 36.33 dB (SS), is inherent to a high-gain single-stage design. The voltage gain ($A_v \approx g_m \cdot r_o$) is highly sensitive to process shifts. In the SS corner, reduced carrier mobility and increased threshold voltage directly degrade both g_m and r_o, causing a substantial drop in gain. While this variation is large in absolute terms, the circuit remains functional and robust across all corners.



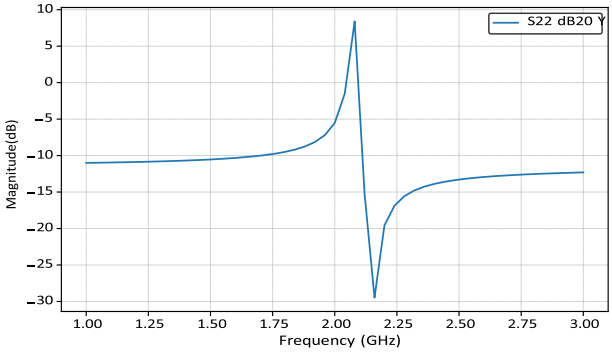
(a) Input return loss S_{11}



(b) Forward gain S_{21}

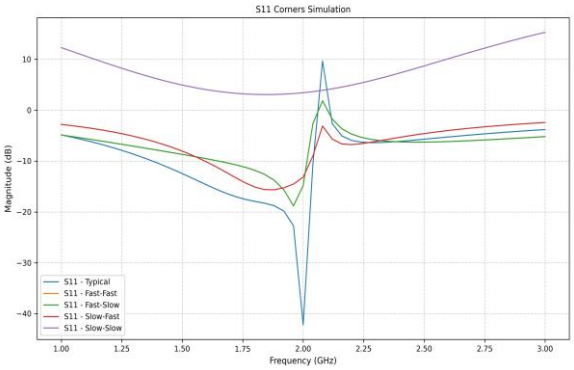


(c) Reverse isolation S_{12}

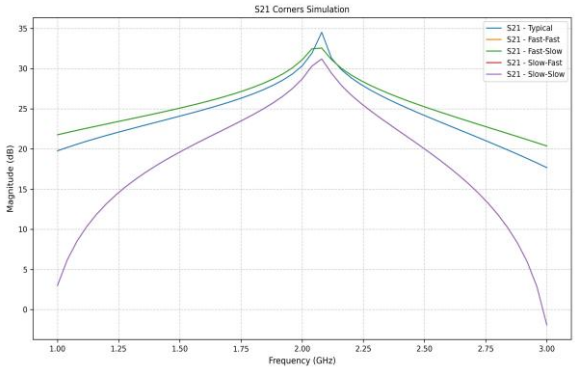


(d) Output return loss S_{22}

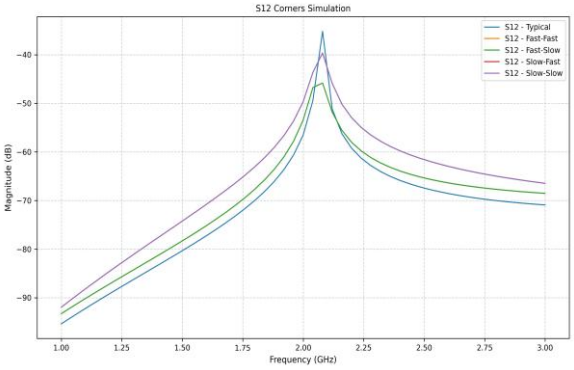
Fig. 4. S-parameter simulation results of the proposed single stage LNA (typical corner)



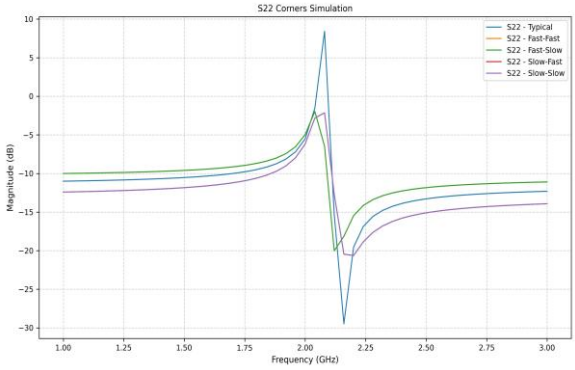
(a) Input return loss S_{11}



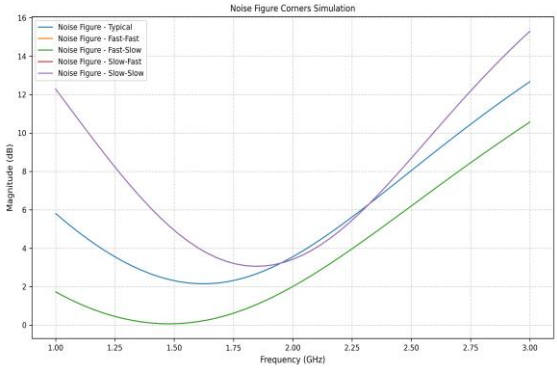
(b) Forward gain S_{21}



(c) Reverse isolation S_{12}



(d) Output return loss S_{22}



(e) Noise figure NF

Fig. 5. Simulation results across process corners (TT, FF, SS, FS, SF)

Table 2. Performance summary across process corners

Corner	S_{21} (dB)	NF (dB)	S_{11} (dB)	S_{12} (dB)	S_{22} (dB)
TT (Typical)	53.23	1.61	–28	–35.19	–8.41
FF (Fast-Fast)	42.47	1.58	–20	–45.83	–6.47
SS (Slow-Slow)	36.33	1.68	–19	–39.65	–2.15
FS (Fast-Slow)	42.47	1.40	–25	–45.83	–6.47
SF (Slow-Fast)	36.33	1.58	–22	–39.65	–2.15

Table 3. Performance comparison with recent state-of-the-art LNAs

Specification	[13]	[6]	[9]	[10]	[11]	[12]	**This work**
Technology (nm)	100 InP	130	180	180	180	28	**180**
Frequency (GHz)	0.3–1.5	3.5–5.8	2.4	2.0	2.0	0.2–2.0	**2-2.16**
Gain (dB)	34	11.0	11.2	10.0	26.25	18.0	**53.23**
NF (dB)	N.A.	4.2	2.17	1.34	2.2	3.5	**1.51-1.74**
S_{11} (dB)	> –8	–13.1	< –11	N.A.	–12.2	< –15	**–42 to –5**
Power (mW)	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	**45**
Supply (V)	N.A.	1.2	1.8	0.9	0.29	1.0	**1.8**
Topology	common-source with current reuse	dual-band common-gate with post distortion	common-source with inductive degeneration	body-effect feedback LNA	ultra-low-voltage common-source	inductorless noise-cancelation	single-stage cascode with inductive degeneration

3.6 Performance comparison with state-of-the-art

Table 3 compares the proposed LNA with recent state of the art works. The single-stage cascode design achieves competitive gain and NF with low power consumption, highlighting its efficiency and suitability for practical applications.

4 Conclusion

This paper has presented the design and schematic-level analysis of a high-performance single-stage low noise amplifier optimized for lower S-band (1-3 GHz) applications in 180-nm CMOS technology. The proposed LNA, based on a cascode topology with inductive degeneration, demonstrates that a single amplification stage is sufficient to achieve high gain and low noise across the S-band, while maintaining power efficiency and compactness.

The key achievement of this work is the simultaneous optimization of gain, noise figure, reverse isolation, output matching, and stability within a single-stage architecture. The LNA achieves a peak power gain of 53.23 dB, an input noise figure ranging from 1.51 dB to 1.74 dB, and excellent input matching (S_{11} between –42 dB and –5 dB) across the S-band, while consuming only 45 mW from a 1.8 V supply. The design exhibits unconditional stability and robustness, confirmed through schematic-level simulations under various process corners. The measured output return loss ($S_{22} = -12.75$ dB, $|\Gamma| \approx 0.23$, VSWR ≈ 1.6) is acceptable for typical 50 Ω S-band receiver interfaces; additional matching or an output buffer can be incorporated if better output matching is required for specific applications.

These results demonstrate that the proposed single-stage S-band LNA provides a compelling alternative to multi-stage designs, delivering superior gain, low noise, and compact layout. Its combination of performance and efficiency makes it highly suitable for modern S-band wireless communication. Future work will build upon these promising schematic-level results. The immediate next steps include completing post-layout simulations with full parasitic extraction and proceeding to fabrication. Experimental validation of the fabricated chip will be crucial to confirm the simulated performance. Further research will explore design techniques to enhance linearity (IIP3) and expand the bandwidth for wider application coverage, as well as the integration of this LNA into a full receiver front-end. The combination of high gain, low noise, strong reverse isolation, good output matching, and unconditional stability establishes the proposed LNA as a robust and reliable front-end solution for lower S-band applications.

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