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Compact and efficient realization of fractional-order filter using admittance equalization-based fractional device

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This paper proposes a novel fractance device (FD) based on simple R-C pairs for realizing fractional-order analog filters. Unlike conventional R-C ladder network-based FDs, which are complex and bulky, the proposed design employs only two passive components. This simplification results in lower cost, compact hardware, and improved power efficiency. The proposed FD is implemented in a VDTA-based fractional-order universal filter to evaluate its performance. The accuracy and validity of the proposed design are verified through SPICE and MATLAB simulations. Further, Monte Carlo analysis confirms the robustness and stability of the proposed circuit under parameter variations. The novelty of this work lies in its minimal-component realization of fractance behavior without compromising performance. The proposed approach supports SDG 7 (Affordable and Clean Energy) and SDG 9 (Industry, Innovation, and Infrastructure), advancing energy-efficient and innovative solutions for modern communication and signal processing systems.

Keywords: fractance device, universal filter, admittance equalization, sustainable electronics, SDG 7, SDG 9

1 Introduction

An electronic filter is a circuit that allows certain frequencies of electrical signals to pass while blocking others. They are used in various applications to manipulate the frequency components of signals in communication systems, audio electronics, and other electronic devices. Based on the frequencies they allow and reject, they are categorized as low-pass, high-pass, band-pass, band-stop, and all-pass filters. Filters are being used in a variety of applications, including transmitters, receivers, signal processing circuits, etc. Filters are defined by three main characteristics: passband ripple, stopband attenuation, and the rate of passband roll-off. For optimal performance, a filter should exhibit minimal ripple in the passband and a steep roll-off. It is often seen that the higher-order filters have improved performance over the lower-order filters in terms of the roll-off rate; i.e., they have a sharp transition between passband and stopband. On the other hand, these higher-order filters tend to be less stable, which reflects deterioration in the transient state response in the form of ringing effects. Achieving a balanced compromise between transient response and stability is crucial when determining a filter's order. Simultaneously managing both aspects poses significant challenges. To address this, fractional calculus is employed in filter design, resulting in what are termed fractional-order filters. These filters offer an additional degree of flexibility in system design, enabling precise adjustments to passband ripple, roll-off rate, and stopband attenuation [1-3]. Further, the responses of fractional-order filters can be altered without varying numerical values of the passive components since there is an additional freedom to adjust the responses by varying the order α of the filter.

To leverage the benefits outlined earlier, considerable efforts have been directed toward developing electronic filters using fractional-order principles. Radwan et al. initially proposed fractional-domain first-order filters, including low-pass, high-pass, band-pass, and band-reject types [3], later expanding their work to second-order systems [4]. Subsequently, Ali et al. introduced active and passive fractional-order Butterworth filter designs and investigated KHN and Sallen-Key filter topologies within the framework of fractional calculus [5]. Nowadays, current mode active building blocks (CMABBs) are becoming more popular in modern analog signal processing. They operate by processing electrical signals in the form of currents rather than voltages.

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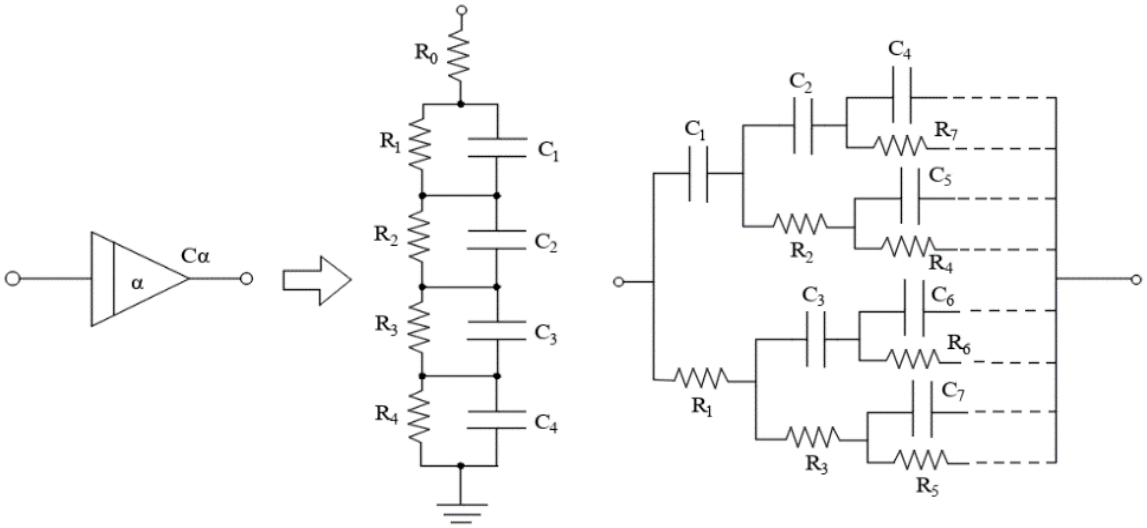

Fig. 1. Approximation of fractional capacitor using Foster type ladder and nested tree network

This approach offers several advantages, such as higher speed, greater bandwidth, and lower power consumption compared to voltage mode circuits. To avail these advantages, several fractional-order filters have been realized using various current-mode active building blocks [6-13]. In fractional-order filters, fractance devices (FDs) replace traditional capacitors and inductors. These FDs serve as fractional energy-storage components and are classified into fractional-order capacitors and fractional-order inductors. The current-voltage relations of the fractional-order capacitor (C) and inductor (L) are defined in Eqs. (1) and (2), respectively [14].

$$i = c(d^{\alpha}v/dt^{\alpha}) \tag{1}$$

$$v = L(d^{\alpha}i/dt^{\alpha}) \tag{2}$$

where α denotes the order of differentiation. It is a non-negative, non-integer value, typically considered within the range $0 < \alpha < 1$.

Regrettably, FDs are not commercially available as discrete components. Nevertheless, various Mathematical approximation techniques, including continued fraction expansion (CFE), regular Newton method, and Taylor series expansion, enable the implementation of FDs through semi-infinite *R-C* tree or ladder circuits [9-15], as illustrated in Fig. 1.

As previously discussed, the current *R-C* network-based approximation requires a large number of passive components to simulate a single fractional capacitor. Consequently, the physical structure of fractional-order filters becomes bulky and expensive due to the use of fractional capacitors instead of conventional integer-order capacitors. Additionally, these ladder network-based FDs reduce power efficiency and introduce more noise into the system. These drawbacks present significant challenges in the design and implementation of fractional-order systems.

In modern times, power-efficient and compact electronic devices are highly required. However, existing fractional-order filter realization methods, particularly those relying on tree or ladder network-based FDs, fail to meet these demands. These FDs not only make the system more costly and noisy but also less reliable. As a result, there is a clear need for new techniques that enhance energy efficiency, compactness, reliability, and noise performance in fractional-order filters.

To address these challenges, some efforts have been made to reduce the size of FDs (fractional-order capacitors and inductors) through alternative mathema-tical approximation methods. One such approach is the impedance equalization technique, which approximates fractional capacitors using *R-C* pairs and fractional inductors using *R-L* pairs. This method has been applied in the design of Wien bridge oscillators [14, 16].

Similarly, admittance equalization techniques have been employed to approximate FDs using just two passive components [17]. Studies show that replacing semi-infinite ladder networks with these impedance and admittance equalization-based FDs significantly improves the performance of fractional-order oscillators in terms of power efficiency, phase noise, cost, and compactness [14, 16-17]. Despite these advancements, the compact *R-C/R-L* pair-based FDs have not yet been applied to enhance the performance of fractional-order filters.

In this paper, we present the application of the novel *R-C* pair-based fractance device (FD) as an alternative to the traditional ladder network-based FDs used in fractional-order filter designs. The primary limitation of ladder network-based FDs is their inherent complexity, bulkiness, and power inefficiency, which hinder their

suitability for modern compact electronic systems. The proposed *R-C* pair-based FD significantly reduces the number of passive components required, making the design more compact, cost-effective, and energy-efficient.

One of the key contributions of this work is the application of the *R-C* pair-based FD to the design of a VDTA-based fractional-order universal filter, capable of realizing multiple filter responses, including low-pass, high-pass, band-pass, and band-stop. The results from SPICE and MATLAB simulations highlight the improved performance of the proposed design, particularly in terms of roll-off rate, stop-band attenuation, resonant peak, and quality factor, compared to conventional methods. Furthermore, Monte Carlo simulations validate the reliability and tolerance of the design, demonstrating its robustness for practical applications.

This research introduces a compact and energy-efficient *R-C* pair-based fractance device (FD) that addresses key limitations of traditional ladder network-based fractional-order filter designs, offering a scalable, reliable, and high-performance solution essential for modern electronic systems demanding miniaturization and enhanced efficiency. By significantly reducing passive component count and power consumption, this work not only overcomes the complexity, bulkiness, and inefficiency of conventional FDs but also aligns with the United Nations Sustainable Development Goals (SDGs). Specifically, it supports SDG 9 (Industry, Innovation, and Infrastructure) by fostering innovative filter designs for advanced communication and signal processing applications, and SDG *7* (Affordable and Clean Energy) by promoting eco-friendly electronics that minimize environmental impact and enable sustainable technology deployment in resource-constrained settings. This contribution lays a foundation for further advancements in efficient fractance device implementations, driving the development of accessible and sustainable electronic systems.

2 Admittance equalization based FDs

The admittance equalization technique is based on the fact that the admittance of a fractional capacitor is equal to the admittance of an *R-C* parallel pair [17]. For example, the admittance of a fractional capacitor of order α and pseudo-capacitance C_f is equal to the overall admittance of a parallel pair of resistor *R* and capacitor *C* as expressed in the following relation:

$$s^{\alpha}C_f = sC + \frac{1}{R} \tag{3}$$

where $s = j\omega$, in which ω is angular frequency in radians/second. The relation given in Eqn. (3) is modified by using Euler's formula to realize a fractional-order capacitor, as given below.

$$\omega^{\alpha}\left(\cos\frac{\alpha\pi}{2} + j\sin\frac{\alpha\pi}{2}\right)C_f = \frac{1}{R} + j\omega C \tag{4}$$

Using Eqn. (4), the expression for obtaining the numerical values of resistance *R* and capacitance *C* can be expressed as

$$R = \cos(\alpha\pi/2)/\omega^{\alpha}C_f \tag{5}$$

$$C = \omega^{(\alpha-1)}C_f/\sin(\alpha\pi/2) \tag{6}$$

The parallel pair of resistor *R* and a conventional capacitor *C* whose numerical values are given in Eqns. (5) and (6) will act as a fractional capacitor C_f of order α as illustrated in Fig. 2. Thus, using the admittance equalization based technique, it is possible to approximate fractional capacitors using two passive components only.

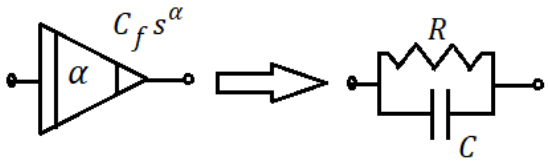

Fig. 2. Schematic of the admittance equalization technique based FD as an *R-C* pair

The *R-C* pair-based fractional differentiators exhibit optimal performance at a specific frequency, ω, making them particularly effective for single-frequency applications, such as sinusoidal oscillators. For low-pass and high-pass filters, the cutoff frequency is critical, while for band-pass and band-stop filters, the center frequency is the key. Building on this concept, a fractional-order filter is designed using *R-C* parallel pair-based FDs, with ω selected as the cutoff (or center frequency for bandpass and band reject filters). To validate this design, these *R-C* parallel pair-based FDs are utilized in the realization of a VDTA-based universal filter in the following section.

3 Fractional-order universal filter

The schematic of the current-mode universal filter with three input terminals and one output terminal is shown in Fig. 3.

This filter consists of a voltage differencing transconductance amplifier (VDTA) as an active device and two fractional capacitors, C_1 and C_2 of order α and β, respectively. The VDTA has two differential input terminals v_p and v_n, where the input voltage difference $v_p - v_n$ drives the operation [17-18]. The associated input currents i_p and i_n are typically negligible in ideal scenarios. Internally, the VDTA converts the differential

input voltage into currents at high impedance nodes Z and ZC, resulting in output currents i_z and i_{zc}, which are proportional to the first transconductance gain g_{mF} of the VDTA.

Additionally, the VDTA generates output currents i_{x+} and i_{x-} at the output terminals $x+$ and $x-$, which are related to the second transconductance gain g_{ms}. These trans-conductance gains, $g_{mF,}$ and g_{ms}, determine the behaviour of the VDTA, making it a key component for applications requiring differential signal processing and voltage-to-current conversion.

The current-voltage relation of the VDTA terminals can be expressed as [18-21]:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 & 0 \\ 0 & 0 & g_{mS} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{zc} \\ v_z \end{bmatrix} \quad (7)$$

This fractional-order universal filter acts as low-pass, band-pass, high-pass, and band-stop for the following four different cases.

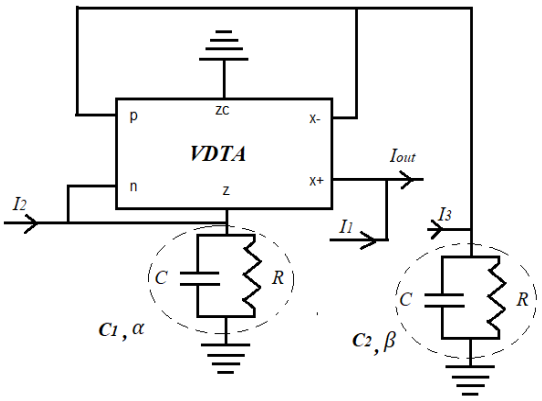

Fig. 3. Proposed compact structure of the current-mode filter

Case 1: Fractional-order low-pass filter

$I_3=I_{in}$ (input current signal), $I_1=I_2=0$, the transfer function is

$$\frac{I_{out}}{I_{in}} = \frac{g_{mF}g_{mS}/C_1C_2}{s^{(\alpha+\beta)} + (g_{mF}/C_1)s^{\beta} + (g_{mF}g_{mS}/C_1C_2)} \quad (8)$$

Case II: Fractional-order band-pass filter

$I_2=I_{in}$, $I_1=I_3=0$, the transfer function is

$$\frac{I_{out}}{I_{in}} = \frac{(g_{ms}/C_1)s^{\beta}}{s^{(\alpha+\beta)} + (g_{mF}/C_1)s^{\beta} + (g_{mF}g_{mS}/C_1C_2)} \quad (9)$$

Case III: Fractional-order high-pass filter

$I_1= -I_2= -I_3=I_{in}$ and the transfer function is

$$\frac{I_{out}}{I_{in}} = \frac{s^{(\alpha+\beta)}}{s^{(\alpha+\beta)} + (g_{mF}/C_1)s^{\beta} + (g_{mF}g_{mS}/C_1C_2)} \quad (10)$$

Case IV: Fractional-order band-stop filter

$I_1=-I_2=I_{in}$, $I_3=0$ and the transfer function is

$$\frac{I_{out}}{I_{in}} = \frac{s^{(\alpha+\beta)} + (g_{mF}g_{mS}/C_1C_2)}{s^{(\alpha+\beta)} + (g_{mF}/C_1)s^{\beta} + (g_{mF}g_{mS}/C_1C_2)} \quad (11)$$

The cutoff or central frequency of the fractional order universal filter can be approximated as

$$\omega_c \cong \left\{\frac{g_{mF}g_{mS}}{C_1C_2}\right\}^{\frac{1}{\alpha+\beta}} \quad (12)$$

It is evident that the cutoff frequency, ω_c, is influenced not only by the device gain parameters and the values of the capacitors but also by the orders of the capacitors, denoted as α and β. As a result, the fractional-order universal filter offers additional parameters that can be used to fine-tune its characteristics. To demonstrate this flexibility, numerical simulations were conducted in the MATLAB environment, as shown in Fig. 4.

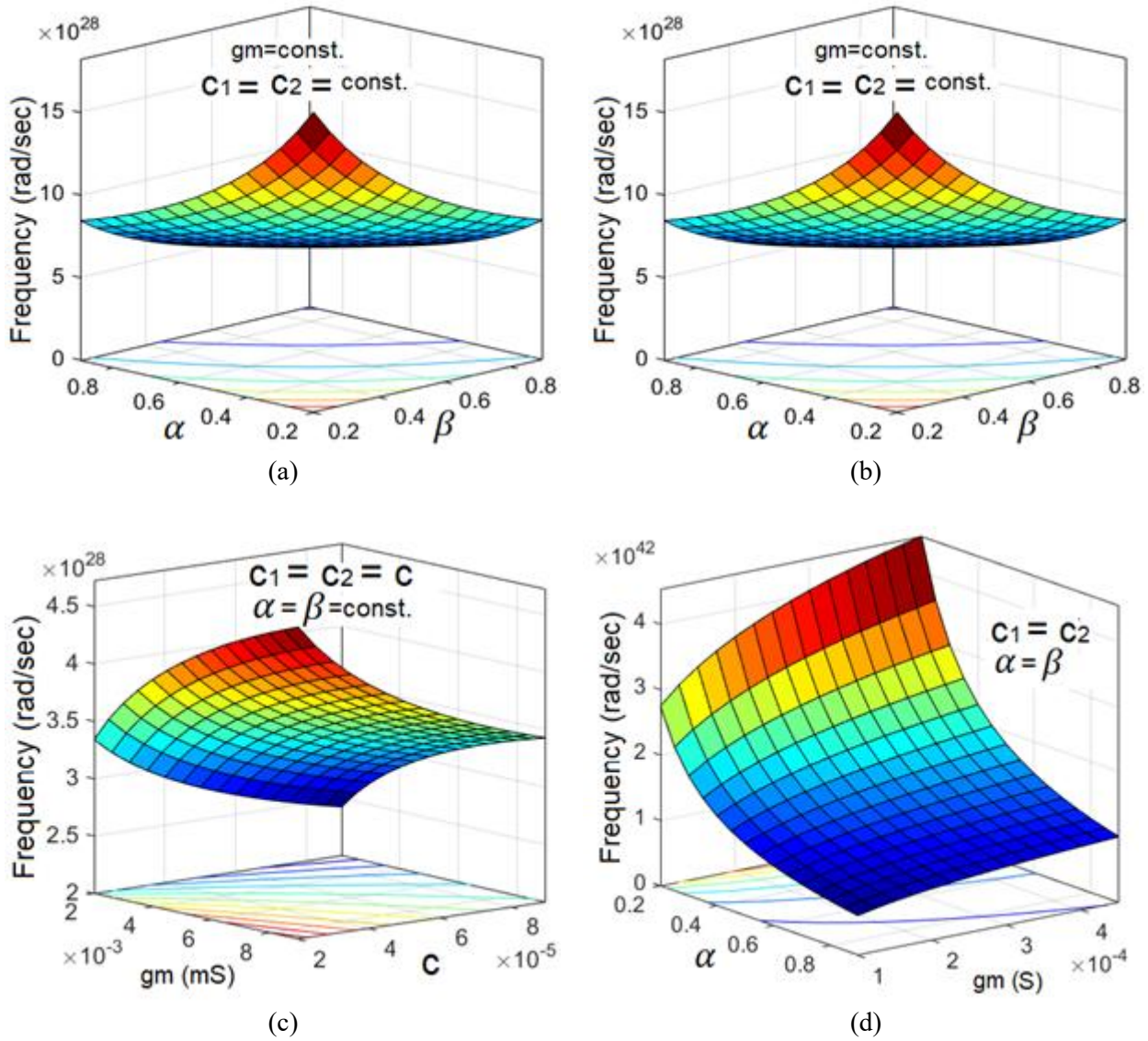

Fig. 4. Frequency dependency on various filter parameters

These simulations highlight the relationship between the cutoff frequency and the device gain, the values of the passive components, and the fractional-order of the capacitors.

4 Stability analysis

Stability analysis plays a vital role in the design of any filter, ensuring that the system operates predictably and remains stable under different input conditions. For fractional-order systems, such as universal filters, stability analysis becomes even more important due to the complex behaviour introduced by fractional dynamics. It allows designers to assess whether the filter will perform without leading to unwanted oscillations or instability over time. To analyze the stability of the proposed fractional universal filter, a pole-zero analysis is required.

Unlike traditional filters, the pole-zero analysis for fractional-order systems is carried out in the W-plane. This complex W-plane is related to the s-plane for fractional-order systems of the form $\delta = n/k$, where n and k are positive integers [22]. Additionally, the W-plane is linked to the k-plane Riemann surface, in which the 1st sheet belongs to the conventional s-plane or the physically defined region of the W-plane [23]. The remaining k-1 sheets are physically not defined and related to the undefined region of the W-plane. The presence of poles and zeros in this undefined region does not affect the system stability. The stability of the proposed fractional-order universal filter is evaluated by analyzing pole locations across various scenarios, as shown in Fig. 5.

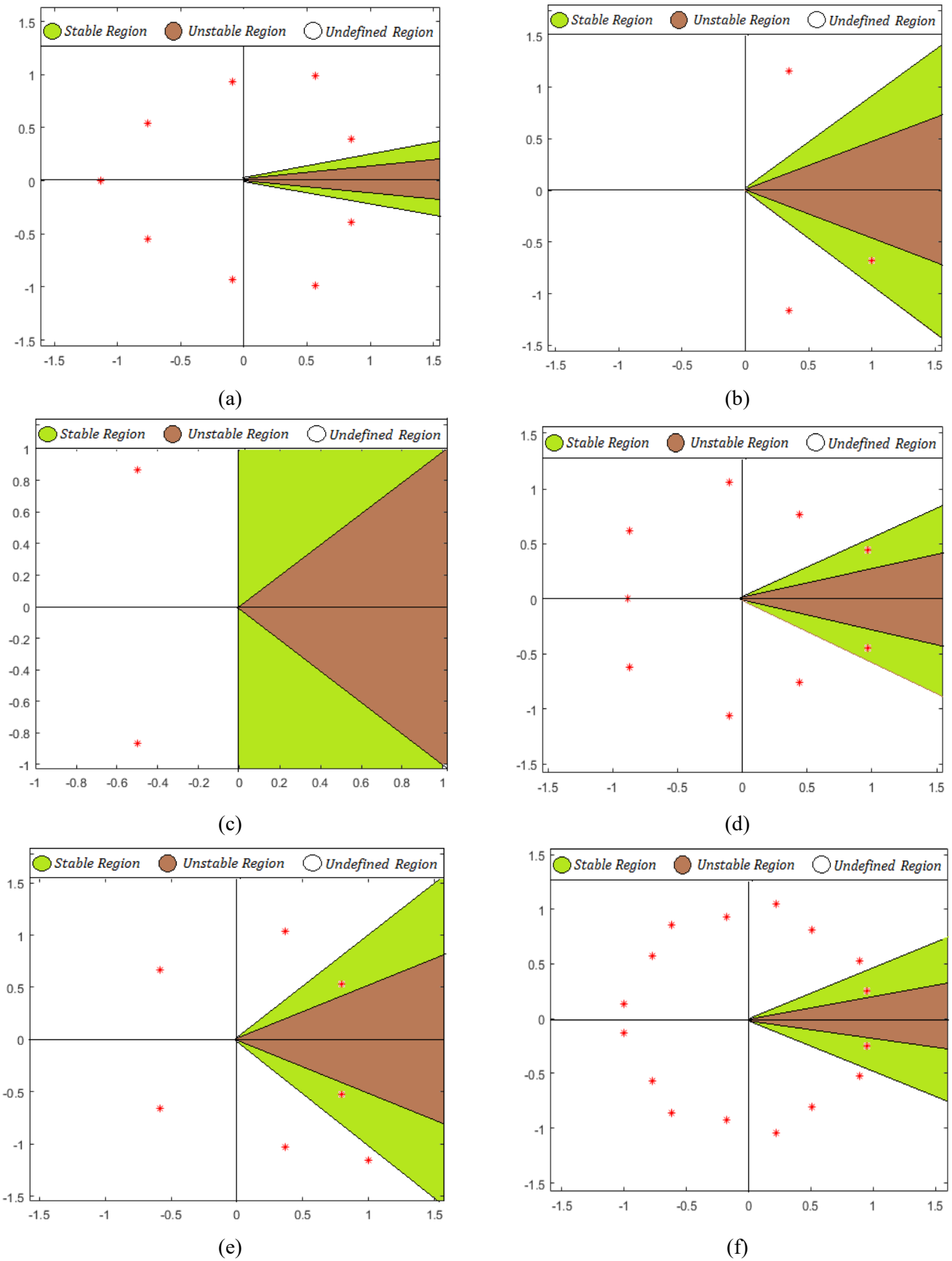

Fig. 5. Pole plot of fractional-order universal filter for (a) α=0.3, β=0.6, (b) α=0.4, β=0.2, (c) α=β=0.5, (d) α=0.6, β=0.3, (e) α=0.6, β=0.8, (f) α=0.7, β=0.9

In all cases, the poles are positioned within the stability region or the physically undefined region. As no poles reside in the unstable region for any scenario, the fractional-order filter consistently delivers a stable output.

5 Circuit simulation

Now, the proposed fractional-order universal filter is simulated in the SPICE environment. Initially, the CMOS-based VDTA, consisting of 18 MOSFETs, is simulated using the 180 nm CMOS technology parameters as shown in Fig. 6. The transistor aspect ratios of VDTA are listed in Tab. 1, and the supply voltages are taken as $V^+ = -V^- = 0.9$ V, whereas the biasing current through transistors M5-M6 and M17-M18 are fixed at 150 µA [18]. In this simulation, the values of α and β are set to 0.8 and 1, respectively. The pseudo-capacitances C_1 and C_2 are fixed at $20\ \text{pFs}^{\alpha-1}$ and $130\ \text{pFs}^{\beta-1}$, resulting in a computed cutoff (or center) frequency of 10 MHz. The simulation is first conducted using the *R-C* parallel pair-based FDs, followed by a similar simulation with conventional Foster-type *R-C* ladder network-based fractional capacitors. This ladder network-based capacitor consists of four capacitors and five resistors. The results of both simulations are compared thoroughly, as illustrated in Fig. 7.

Table 1. W/L ratio of the used transistors in VDTA

Transistors	M_1, M_2, M_5, M_6	M_3, M_4, M_7, M_8	M_9 – M_{12}	M_{13}, M_{18}	M_{14} – M_{17}
W (µm)	32.2	52.4	42	15	17.5
L (µm)	1.4	1.4	1.4	1.4	1.4

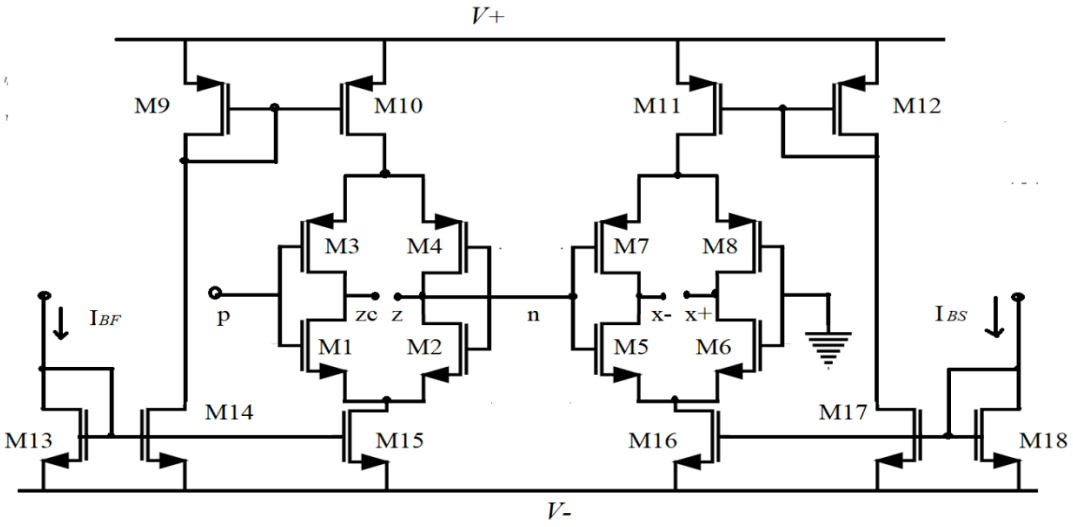

Fig. 6. CMOS schematic of VDTA [18]

It is observed that the proposed *R-C* parallel pair-based FDs deliver an improved response over the traditional *R-C* ladder network-based design, particularly in terms of roll-off rate and stop-band attenuation. For the bandpass filter, the *R-C* parallel pair-based FDs also show significantly better results in terms of resonant peak and quality factor. This performance comparison is summarised in Tab. 2. This comparison indicates that the proposed single *R-C* pair-based FD effectively replicates the behaviour of the conventional *R-C* ladder-based fractional capacitors, providing consistent and reliable filtering performance. This single *R-C* pair-based FD not only enhances the performance of the proposed fractional-order universal filter in terms of magnitude response but also offers advantages in cost, complexity, noise, and power consumption, as it requires fewer passive components. The proposed scheme is further evaluated against existing state-of-the-art circuits, with a summary presented in Tab. 3.

To further evaluate reliability, a Monte Carlo simulation was conducted to compare the two schemes, as shown in Fig. 8. This analysis was performed with a 5% tolerance in the values of the passive components over 100 runs. The results indicate that the low-pass and

band-stop filters exhibit similar reliability in both cases. However, for the high-pass and band-pass filters, the *R-C* ladder-based design is less tolerant to variations in gain, while the newly proposed *R-C* pair-based design shows greater tolerance to frequency variations.

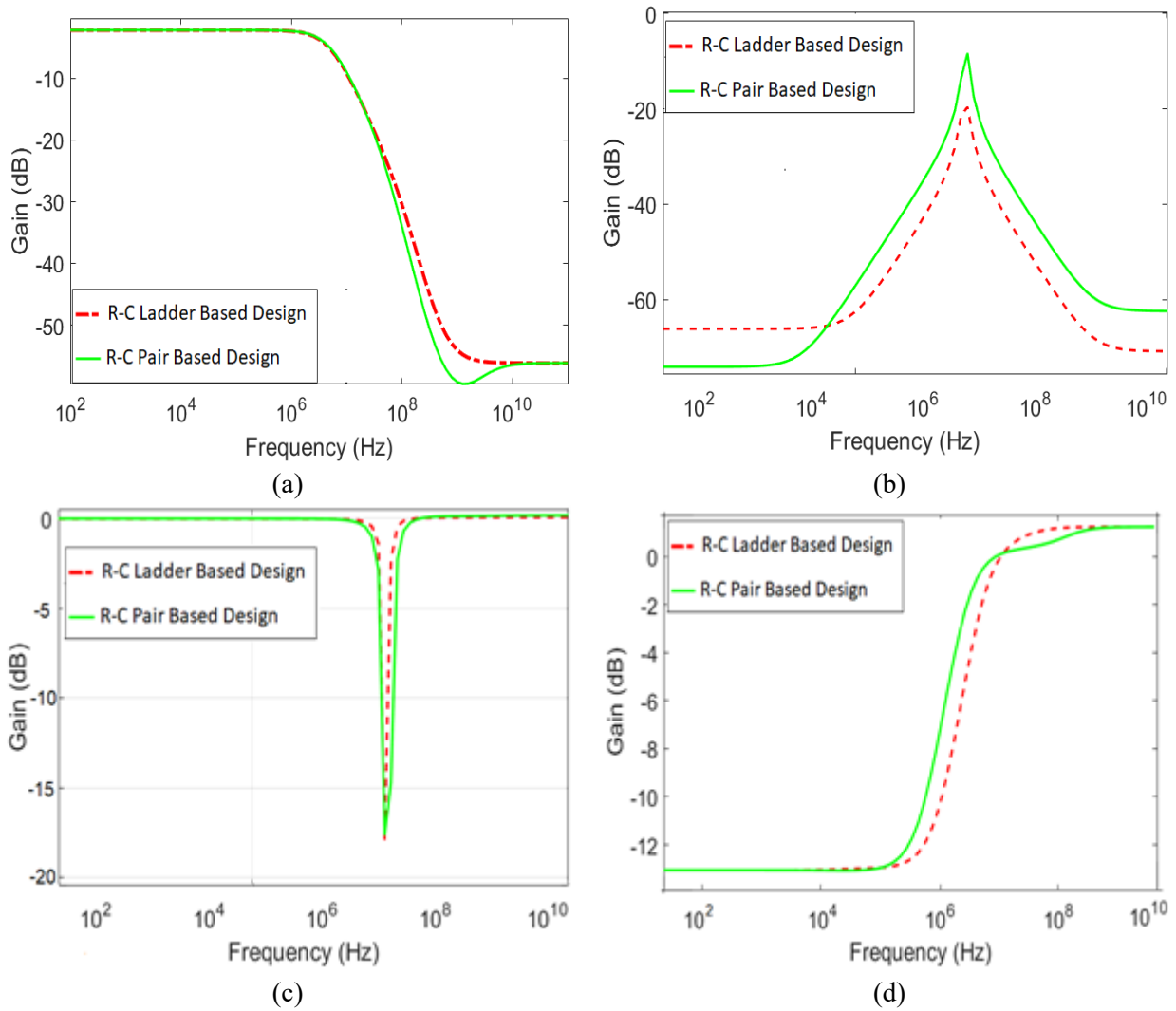

Fig. 7. LTSpice response of the fractional-order universal filter as (a) lowpass filter, (b) bandpass filter, (c) bandstop filter, and (d) highpass filter

Table 2. Comparison of proposed and existing *R-C* ladder based fractional-order filters

Design specifications		Transition bandwidth	Max. stop band attenuation	3-dB bandwidth (for BPF/BSF)	Components per FDs
Existing *R-C* ladder network based design	Lowpass	100 MHz	–58 dB	NA	9
	Highpass	100 MHz	–13 dB	NA	9
	Bandpass	90 MHz	–68 dB	3.3 MHz	9
	Bandstop	60 kHz	–18 dB	1.3MHz	9
Proposed *R-C* pair based design	Lowpass	78 MHz	–60 dB	NA	2
	Highpass	85 MHz	–13 dB	NA	2
	Bandpass	65 MHz	–72 dB	3.2 MHz	2
	Bandstop	85 kHz	–18 dB	1.5MHz	2

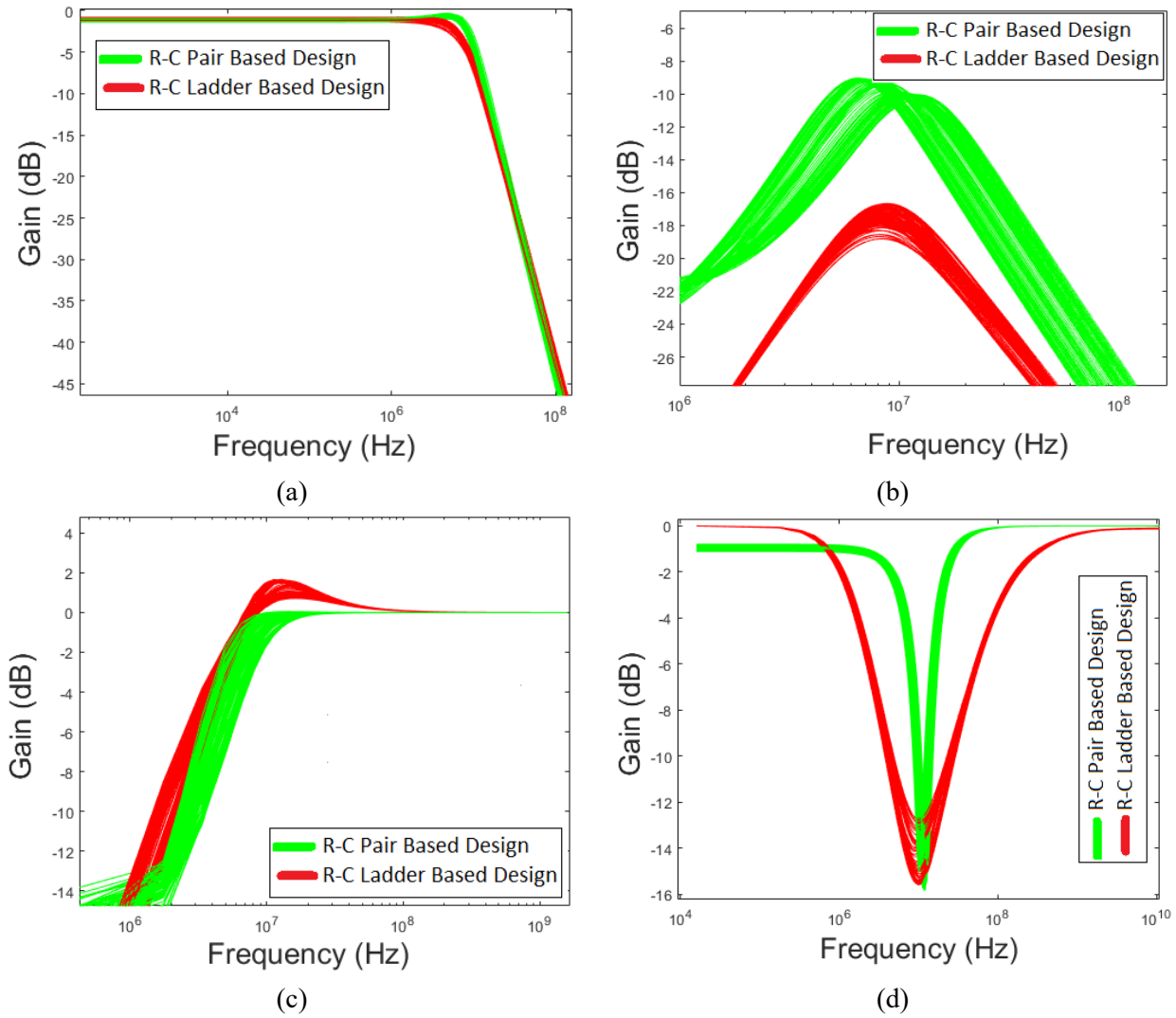

Fig. 8. Monte Carlo simulation for the (a) lowpass, (b) bandpass, (c) highpass, and (d) bandstop response

Table 3. Comparison with existing fractional-order filters

Reference	Filter realization	Active block	FD approximation scheme	Components per FDs	Total passive components
Varshney et al. [8]	Universal filter	CIM	Cauer-type *R-C* ladder	16	35
Nako et al. [7]	LPF and HPF	CFOA	Foster-type *R-C* ladder	9	11
Daryani and Aggarwal [12]	Chebyshev LPF	OTA/CCII	Foster-type *R-C* ladder	9	11
Khalil et al. [11]	LPF and HPF	CCII	Cauer-type *R-C* ladder	11	11
Verma et al. [9]	LPF, BPF and HPF	OTA	Foster-type *R-C* ladder	9	18
Proposed	Universal filter	VDTA	*R-C* pair	2	4

6 Conclusions

This paper presents a novel *R-C* pair-based FD as a compact and energy-efficient alternative to conventional *R-C* ladder network-based FDs for fractional-order filter design. By minimizing the number of passive components, the proposed FD overcomes the complexity, bulkiness, and power inefficiency of traditional designs. The FD, implemented in a VDTA-based fractional-order universal filter, exhibits improved roll-off characteristics, enhanced stop-band attenuation, and higher quality factors compared to previously reported ladder-based and FD emulation approaches. SPICE and MATLAB simulations validate these performance improvements, while Monte Carlo analysis confirms robustness under parameter variations. Aligned with SDG 7 and SDG 9, this work supports low-power, resource-efficient analog circuit design. The findings provide a foundation for future development of compact fractance devices with applications in communication systems, IoT hardware, and biomedical signal processing.

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