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High gain low noise figure LNA circuit employing variable gain amplifier

Dheeraj Kalra[1], Mayank Srivastava[2]

This paper presents the realization of high gain low Noise Figure (NF) Low Noise Amplifier (LNA) employing the variable gain amplifier. The high gain is achieved by cascading three stages while the low NF is achieved by employing the resistive feedback in the input stage. The linearity is achieved by employing the source degeneration technique. The variable gain amplifier gets turned on/off by the input signal causing the change in the transconductance of the LNA and hence the gain of LNA varies according to the input signal strength. The results show that maximum gain for the realized LNA is 21.34 dB at 1.72 GHz for M_7 ON position while during M_7 OFF position, the maximum gain achieved is 26.05 dB at 1.72 GHz frequency. The S_{11} value is less than –9 dB for the frequency range of 1.65 GHz to 3.9 GHz, i. e., having the bandwidth of 2.25 GHz and it is matched for the 50 Ω termination at input and output port. The minimum value of the NF during low conductance is 2.88 dB while during the high conductance it is 2.82 dB.

Keywords: LNA, variable gain amplifier, cascade stage, NF

1 Introduction

In today's world, there is a requirement for circuits which can operate at high frequency with low power consumption. LNA is a basic building block connected after the antenna in the receiver circuit whose function is to amplify the signal with less introduction of noise, i. e., its function is to improve the quality of signal. In the receiver circuit, performance of rest of receiver's circuit is governed by the performance of the LNA circuit. For the broadband LNA circuit, there is requirement of high gain, low NF, impedance matching at input and output port, low power consumption with gain stability. There are various topologies which are used to improve these parameters like distributive amplifier topology, source degeneration topology, feedback topology, noise cancellation technique, gain enhancement technique etc.

Over the years, numerous researchers have proposed various design improvements techniques to enhance LNA performance, addressing challenges related to bandwidth, linearity, and integration in modern communication systems. In [1], the distributed amplifier technology was introduced and it was simulated using the 180 nm CMOS technology. The design obtained a maximum gain of 20.5 dB and it is having the bandwidth of 35 GHz. The NF lying between 6.8 to 8 dB, layout design has been presented and it is having the chip area of 0.78 mm^2. In [2], the CMOS LNA has been presented using transformer feedback for the wideband matching and it has employed the noise cancellation technique also. The circuit simulation has been done using CMOS technology and has achieved the gain of 14 dB and NF of 1.8 dB for the frequency range 1.2 to 6.0 GHz. The second LNA is having bandwidth of 55-65 GHz with 16.4 dB gain and 6.8 dB NF. The transformer feedback provides good impedance matching as well as the noise cancellation. In [3], the triple path noise cancellation LNA is simulated for 1 to 20 GHz and it has used the PMOS NMOS dual complementary configuration. The triple path has effectively reduced the noise as the signal travels through the three paths. It has used the CG and CS configuration for the noise cancellation technique and it has achieved the area of 0.96 mm^2.

The book [4] has provided various analytical approach to design the RF integrated circuits. It mainly covers the basic concepts of the NF, noise analysis, impedance matching, gain enhancement techniques, the small signal analysis of the circuits, and the parasitic capacitances. In [5], the 40 nm band pass distributed amplifier was proposed which used the mirror transformation Norton transformation to reduce the size of inductors. The proposed LNA [5] has the maximum power gain of 7 dB, NF less than 6.2 dB, an area of 0.15 mm^2 and 11 dBm IIP3. In [6], 28 GHz CMOS LNA has used the g_m boosting technique. g_m boosting increases the circuit's transconductance, thereby improving gain, the circuit has achieved the maximum gain of 18.33 dB while NF of 3.25 dB and the frequency

[1] ECE Department, GLA University, Mathura, 281406, India
[2] ECE Department, NIT Jamshedpur, Adityapur, 831014, India
dheeraj.kalra@gla.ac.in

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range is 24.9 to 32.5 GHz. It has presented the stability performance for the millimetre wave frequencies. The study presented in [7] focuses design of a LNA operating in the 1.9 to 22.5 GHz frequency range. In this work, the parallel LC load with resistive shunt feedback has been employed to form the input matching network. A detailed small-signal analysis is performed, including mathematical expressions for both gain and NF. In [8], the wide band LNA design is proposed using the complementary CG and CS stages, which help in increasing the gain as well as the bandwidth of the circuit. The cascaded structure provided the large gain over the wide band. In [9], the CMOS LNA with multistage noise matching technique has been presented. It has achieved the gain of 16.6 dB and minimum value of NF is 3.30 dB. The multistage noise matching approach has effectively reduced the NF over the wide band. In [10], the L-type matching is proposed which effectively improves the matching at the input side and it has achieved the gain of 22.2 dB with NF of 3.0 dB. The mutual coupling has been done and it gives the wideband matching & gain flatness. In [11], a high frequency LNA has employed the pi matching network at the input side, it achieved the NF of 3.24 dB and the pi matching network is a good solution for the 50 Ω matching at the input side. In [12], circuit has been simulated for 23 to 32 GHz and it has used the Bi-CMOS LNA architecture. It has achieved the maximum gain of 12 dB while NF less than 5 dB. The Bi-CMOS technology helped in decreasing current consumption over the wideband frequency range. The paper high-lights the inherent trade-offs among critical parameters such as NF, gain, impedance matching, and power efficiency [13].

In [14], the LNA circuit is designed for the 2-20 GHz frequency range. The realized LNA used low pass matching network between common gate and common source stages which provide the stability in the circuit. The realized LNA has used the 90 nm GaAs pHEMT process technology and having the maximum gain of 25 dB with 1.5 dB NF. In [15] the dual reactive feedback and frequency-dependent feedback loops are used to design the LNA stages. The realized LNA has been simulated for the 6-14 GHz frequency range and achieved the gain of 27.55 dB with 1.21 dB minimum NF. In [16], a wideband 26.5-38 GHz LNA has been proposed which incorporates the variable gain control mechanism. The realized LNA has implemented the dual feedback loop to enhance the bandwidth and achieved the gain of 26.9-29.9 dB with 1.57-2.83 dB NF range. Designing LNAs for high-frequency applications remains a complex challenge due to these interdependent constraints [17]. The subsequent section discusses the implementation of the proposed circuit. Section 2 is explaining working of realized LNA along with the available LNA architectures. The derivation for the gain, impedance matching, NF has been done in this section. The small signal model is also presented. The results and discussion have been presented in section 3.

2 Realized circuit

There are various noise cancellation and noise reduction techniques, the traditional one is inverter based by using feedback resistance [3]. As shown in Fig.1 (a), the inverter along with feedback resistance is connected to provide stability, but this traditional LNA directly place noise over the input port. To reduce the noise effect at the input port, the inductor is connected as shown in Fig. 1 (b), so that there is less effect on the input referred noise. So, it becomes clear that the NF of Fig. 1 (b) LNA will be less than the NF of Fig. 1 (a) LNA. This architecture can be further improved by placing inductor as shown in Fig. 1 (c), the noise due to NMOS and PMOS will be having less effect on the input and the noise due to feedback resistance will get shorted by the parasitic capacitances of MOS. The concept of variable gain amplifier can be put as shown in Fig. 1(d) in which the gain of the circuit varies according to the input signal strength. The ON/OFF position of variable gain amplifier circuit will decrease/increase the transconductance of the circuit and henceforth the gain of the circuit also varies.

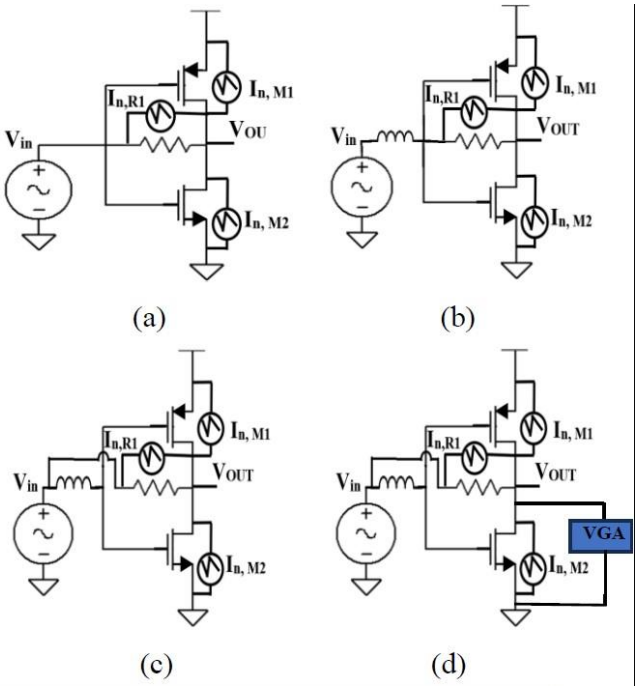


Fig. 1. Four-inverter based LNA architectures

The realized circuit is shown in Fig. 2, in which the first stage is an inverter-based noise removal technique. The second and third stages are the inductive coupled techniques to increase the gain of the circuit with flat

values. MOS M_1 connected in the common source configuration with L_2 acting as the source degeneration technique which is helpful to improve the linearity of the circuit. Inductor L_1 is helpful in the impedance matching of the circuit while resistance R_1 provide the feedback path to reduce the NF of the circuit. The inductor L_2 is connected at the input stage to cancel out the parasitic capacitances and improve the impedance matching. At the last stage the MOS M_7 act as the variable gain amplifier, the ON/OFF position of the MOS M_7 varies the total transconductance of the circuit resulted into the gain of the circuit. Table 1 depicts the components dimension used in the realized circuit.

Table 1. Component dimensions

Component	Dimension	Component	Dimension	Component	Dimension
M_1	192/0.18 µm	M_7	192/0.18 µm	L_3	800 pH
M_2	168/0.18 µm	R_1	300 Ω	L_4	600 pH
M_3	192/0.18 µm	R_2	60 Ω	L_5	820 pH
M_4	192/0.18 µm	R_3	40 Ω	L_6	600 pH
M_5	96/0.18 µm	L_1	380 pH	C_1	550 fF
M_6	192/0.18 µm	L_2	200 pH	V_{DD}	1.8 V

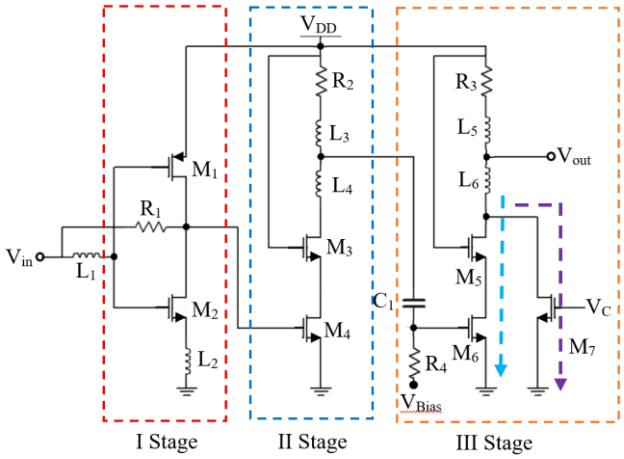
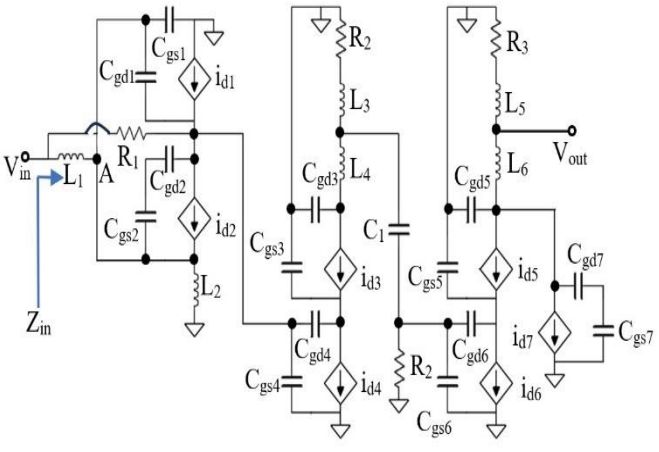


Fig. 2. Realized LNA circuit



where $i_{dj} = g_{mj} v_{gsj}$

Fig. 3. Small signal model of realized LNA

2.1 Input impedance

The input impedance matching minimizes signal reflections at the input port. The small signal model of the realized LNA is shown in Fig. 3. At node A, the effective input impedance is given by Eqn. (1).

$$C_{in} = (C_{gs1} + C_{gs2}) + (1 - A_{v1})(C_{gd1} + C_{gd2}) \quad (1)$$

where A_{v1} is the gain of stage I which will be negative as it is a CS configuration. The effect of source degeneration inductor L_2 at the input port as real resistance is given by Eqn. (2).

$$R_{eff,L2} = \frac{(g_{m1} + g_{m2})L_2}{C_{in}} \quad (2)$$

The feedback resistance R_1 effectively seen at node A is given by

$$R_{eff,R1} = \frac{R_1}{1 - A_{v1}} \quad (3)$$

So, the total input impedance is given by

$$Z_{in}(\omega) = j\omega L_1 + \left[j\omega C_{in} + \frac{1}{R_{eff,L2}} + \frac{1}{R_{eff,R1}} \right]^{-1} \quad (4)$$

Substitute the values of $R_{eff,L2}$ and $R_{eff,R1}$.

$$Z_{in}(\omega) = \omega L_1 + \left[j\omega C_{in} + \frac{C_{in}}{(g_{m1} + g_{m2})L_2} + \frac{1 - A_{v1}}{R_1} \right]^{-1} \quad (5)$$

The real and imaginary parts of $Z_{in}(\omega)$ at desired frequency can be given as

$$Re[Z_{in}(\omega)] = \left(\frac{(g_{m1}+g_{m2})L_2}{C_{in}}\right) \quad (6)$$

$$Im[Z_{in}(\omega)] = \left(\omega L_1 - \frac{1}{\omega C_{in}}\right) \quad (7)$$

The values of the components can be chosen such that $Z_{in} = 50\ \Omega$.

2.2 Gain calculation

The overall gain is the product of the gains of three stages.

$$A_v = A_1.A_2.A_3 \quad (8)$$

The gain of stage I is given by

$$A_1 = \frac{v_{\text{out1}}}{v_{in}} = \frac{i_{d2}\cdot Z_{\text{load 1}}}{v_A} = \frac{g_{m2}(R_1 \| j\omega L_1)}{1+g_{m2}j\omega L_2} \quad (9)$$

where $Z_{\text{load 1}}$ is the load impedance of stage I.

The gain of stage II is given by

$$A_2 = g_{m4}(R_1 \| j\omega L_3 \| j\omega L_4) \quad (10)$$

The gain of stage III is given by

$$A_3 = g_{m6}(R_3 \| j\omega L_5 \| j\omega L_6) \quad (11)$$

The total gain is

$$A_v = \left[\left(\frac{g_{m2}(R_1 \| j\omega L_1)}{1+g_{m2}j\omega L_2}\right) \times (g_{m4}(R_1 \| j\omega L_3 \| j\omega L_4)) \times (g_{m6}(R_3 \| j\omega L_5 \| j\omega L_6))\right] \quad (12)$$

The gain is dependent on the transconductance parameters which changes according to the ON/OFF state of MO7 M_7. Henceforth the state of M_7 decides the maximum value of S_{21}.

2.3 Noise analysis

The noise sources due to MOS M_1, M_2 and feedback resistance are $\overline{i_{n1}^2} = 4kT\gamma g_{m1}$, $\overline{i_{n2}^2} = 4kT\gamma g_{m2}$, and $\overline{v_{nR1}^2} = 4kTR_1$, respectively [16], where k is the Boltzmann constant, T is temperature in kelvins, and γ value is 0.67 for long channel. The total equivalent input noise voltage is given by

$$\overline{v_{neq.}^2} = \overline{v_{nR1}^2} + \frac{\overline{i_{n1}^2}}{g_{m1}^2} + \frac{\overline{i_{n2}^2}}{g_{m2}^2} \quad (13)$$

The noise factor (F_1) of stage I is given as

$$F_1 = 1 + \frac{\gamma}{g_{m1}R_s} + \frac{\gamma}{g_{m2}R_s} + \frac{R_1}{(1-A_{v1})R_s} \quad (14)$$

where R_s is the source resistance.

The effective noise contributions from the second and third stages are given by

$$F_2 = 1 + \frac{N_2}{N_{1out}A_2} \quad (15)$$

$$F_3 = 1 + \frac{N_3}{N_{2out}A_2} \quad (16)$$

where N_{1out} is the noise output of stage I which is the input referred noise for stage II, $N_2$is the noise contributions of stage II, $N_{2out}$is the noise output of stage II, i. e., input noise for stage III and N_3 is the noise contribution of stage III. When referred back to stage I input; the noise factor of stage II and III are $\frac{F_2-1}{A_1}$ and $\frac{F_3-1}{A_1.A_2}$ respectively. So, the total noise factor [4] can be written as

$$F_{Total} = F_1 + \frac{F_2-1}{A_1} + \frac{F_3-1}{A_1.A_2} \quad (17)$$

3 Simulation results

The realized circuit is simulated using the 180 nm CMOS technology on Cadence Virtuoso software. Figure 4 shows the NF simulation for the realized LNA during ON and OFF position of the MOS M_7 for the frequency range of 1 GHz to 7 GHz. As it can be clearly seen that the minimum value of the NF during low conductance is 2.87 dB while during the high conductance it is 2.82 dB.

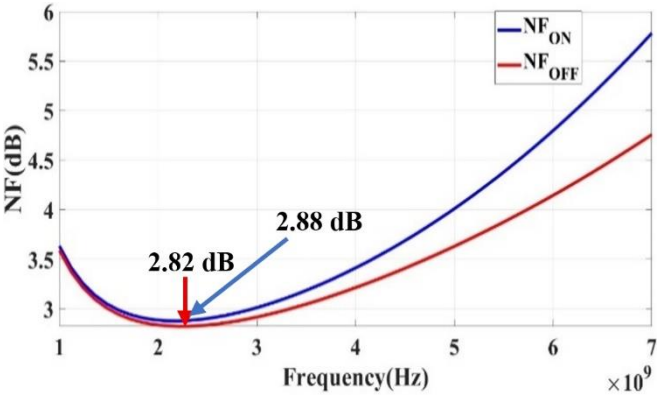


Fig. 4. NF simulation for ON and OFF conditions of MOS M_7

Figure 5 shows the input reflection coefficient for the realized LNA circuit during the ON (low conductance) position of MOS M_7 and OFF (high conductance) position of MOS M_7 for the frequency range of 1 to 7

GHz. As shown in Fig. 5, the S_{11} value is less than –9 dB for the frequency range of 1.65 GHz to 3.9 GHz, i. e., having the bandwidth of 2.25 GHz. It is interesting to see that during the high and low transconductance value of the realized circuit the input reflection coefficient is same. The gain of the circuit should be as high as possible. Figure 6 shows the gain of realized circuit using the variable gain amplifier topology. During the ON position of MOS M_7 the maximum gain achieved is 21.34 dB at 1.72 GHz while during M_7 OFF position, the maximum gain achieved is 26.05 dB at 1.72 GHz frequency. The achieved bandwidth is 2.25 GHz in accordance with the input impedance matching. As shown in Fig. 6, the blue curve is showing the gain during the ON position of MOS M_7 and red colour is showing the gain value for MOS M_7 OFF position.

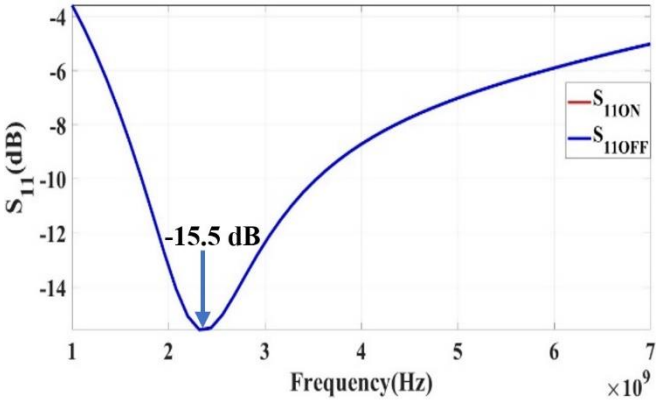


Fig. 5. S_{11} simulation for ON and OFF conditions of MOS M_7

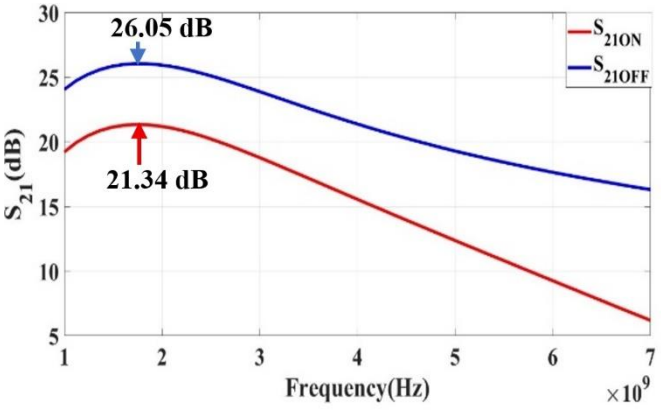


Fig. 6. S_{21} simulation for ON and OFF conditions of MOS M_7

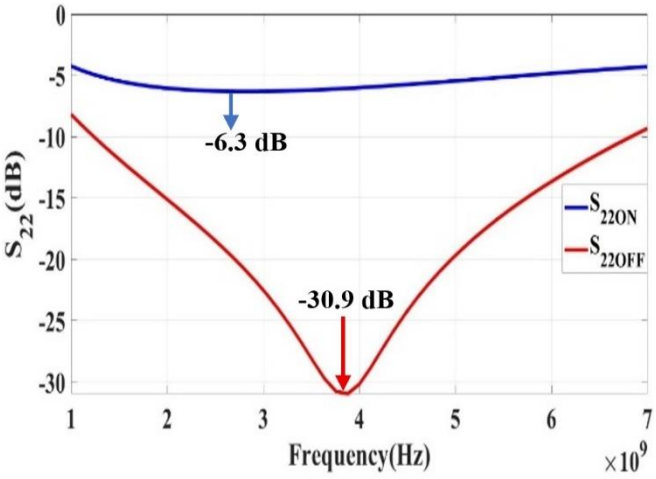


Fig. 7. S_{22} simulation for ON and OFF conditions of MOS M_7

Figure 7 shows the output impedance matching for the realized LNA and it is clearly shown that the value of S_{22} is less than the –10 dB for the desired frequency band during the OFF position on MOS M_7. The process corner simulation is showing in Fig. 8 for all the four corners of S_{11} and S_{21}. The results are showing that the values are in the range. This simulation is used to check the robustness of the circuit for the process variations. The comparison with other references is given in Tab. 2.

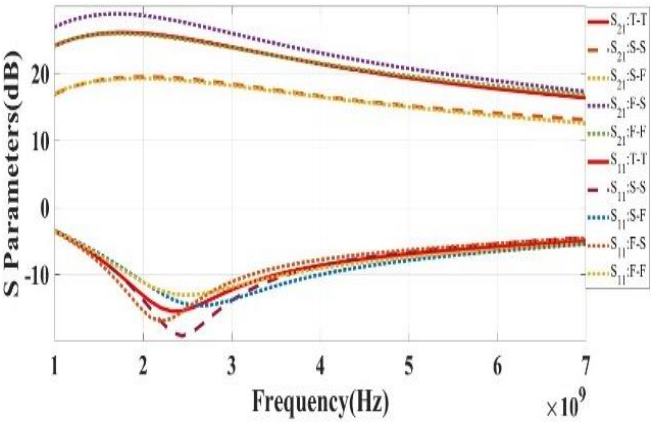


Fig. 8. Process corner simulation of S_{11} & S_{21} for OFF condition of MOS M_7

4 Conclusion

The LNA circuit realized using the 0.18 µm CMOS technology in Cadence Virtuoso software. The variable gain amplifier techniques employed to vary the gain of the circuit according to the input signal strength. The cascaded stages helped in increasing the gain of the circuit. The results show the high gain for the realized LNA is 21.34 dB at 1.72 GHz while during M_7 OFF position, the maximum gain achieved is 26.05 dB at 1.72 GHz frequency. The S_{11} value is less than –9 dB for the frequency range of 1.65 GHz to 3.9 GHz, i. e., having the bandwidth of 2.25 GHz and it is matched for the 50 Ω termination at input and output port. The minimum value of the NF during low conductance is 2.87 dB while during the high conductance it is 2.82 dB. The comparison Tab. 2 shows the various parameters with other references.

Table 2. Comparison of realized LNA parameters with other references

Reference	Frequency (GHz)	Gain (dB)	NF (dB)	Power (mW)	Supply voltage (V)	Process
[3]	1-20	12.8	3.3	20.3	1.6	65 µm
[6]	24.9-32.5	18.33	3.25	20.52	1.2	65 nm
[8]	7.6-29	10.7	4.5	12.1	1.0	65 nm
[9]	7.2-27.3	16.6	3.3	13.2	1.5	65 nm
[10]	22-47	22.2	3.0	9.5	1.2	65 nm
This work	1.65-3.9	26.05	2.82	10	1.8	0.18 µm

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