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Unique 3-input XOR gate for nanocomputation in QCA nanotechnology

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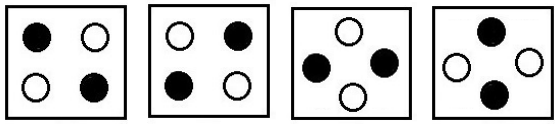
The scaling of metal oxide semiconductor field effect transistor (MOSFET) causes many limitations in current scaled technology nodes. The secondary effects limit the application of MOSFETs in nanoscaled logic circuits. Many alternative ways are suggested for the innovation of new technological developments. Quantum-dot cellular automata (QCA) nanotechnology is getting key attention in the current scenario due to the ability of fast, power- and area-efficient implementations of the logic circuits. The exclusive OR (XOR) gate is the basic building block of many logic applications. Hence, this paper proposes an optimized novel structure of a 3-input XOR (XOR3) gate, which is successfully verified for the logic designs of a 4-bit parity generator, a 4-bit full adder, and a 4-bit binary to gray code converter. The proposed XOR3 gate consists of 8 QCA cells only and 2 clock phases. The reliability concern in terms of fault-tolerant analysis for the proposed XOR3 gate is also presented in the paper. The proposed designs are compared with the existing designs and show the improved performance metrics. The QCA Designer-E tool is used for circuit simulations. The energy dissipation values are estimated using the QCA Designer-E and the QCA Pro tools. The proposed XOR3 gate, 4-bit parity generator, 4-bit full adder, and 4-bit binary to gray code converter save a total of 20%, 26.32%, 26.40%, and 17.24% of cells, respectively, in comparison with the best-reported similar design.

Keywords: MOSFET; QCA; XOR3; fault-tolerant; parity generator; full adder; binary to gray code converter, energy-efficient

1 Introduction

The rapid demand of the portable systems motivates the researchers to work at lower technology nodes in order to make the systems more compact and fast. MOSFET technology is the prime aspect to develop the advanced portable systems. MOSFET technology works properly for the logic implementation in the above ultra-nanoscaled technology nodes. But MOSFET technology faces the challenge of material breakage in the below ultra-nanoscaled technology nodes. It leads the researchers to explore the alternative technologies for further growth of the field [1]. There are various alternative ways available, like fin-type field effect transistor, carbon nanotube field effect transistor, graphene nanoribbon field effect transistor, QCA, etc., in this field [2-4]. QCA nanotechnology contains numerous advantages, such as lower energy dissipation, fast, lower area occupancy, etc., which encourage the researchers to develop the systems using QCA nanotechnology [5].

QCA nanotechnology works on the movement of electrons in a QCA cell. Two electrons are available in a QCA cell out of four quantum-dots. So, the movement of electrons is possible in the empty quantum-dots. The specific location of an electron pair in a QCA cell introduces the theory of logic formation. Therefore, binary logic is identified by the location of the electron pair in a QCA cell [6]. The identification of logic low and logic high for a QCA cell is presented in Fig. 1.



(a) (b) (c) (d)

Fig. 1. Identification of logic: (a) low in 90°, (b) high in 90°, (c) low in 45°, (d) high in 45°

A QCA cell is available in two types: regular or 90° cell and rotated or 45° cell [7]. Figure 1 represents both 90° and 45° cells. In the case of a rotated cell, the quantum-dots are available in the rotated way as depicted in Figs. 1(c) and 1(d). It is preferred that a single type of cell be utilized in a QCA circuit. Both types of cells can be utilized in case of crossover required.

In a QCA circuit, there are a number of QCA cells depending on the implementation of the logic function. Therefore, these QCA cells may be connected in different configurations. If the number of QCA cells are connected back to back, then it forms a QCA wire, which

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acts similarly to conventional electrical wire to flow the signal in the form of electrons [8].

In comparison to the MOSFET technology, QCA nanotechnology does not contain current and voltage sources. The flow of electrons in a wire is accomplished with the application of a QCA clock [9]. Hence, the effective implementation of the QCA circuits is finished with the accurate use of QCA clocks. If the QCA clock is not adequately utilized, then chances of logic failure are high, and output deviates from the actual behaviour. A QCA clock includes four phases: switch, hold, release, and relax [10]. A QCA clock for one cycle is shown in Fig. 2. Each clock phase lags 90° with the consecutive phase.

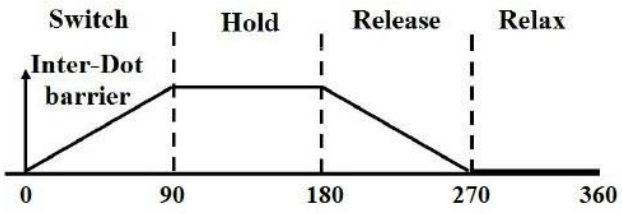


Fig. 2. A QCA clock with phases

The crossover is an important scheme to utilize in complex circuits, where different QCA wires pass the logic values from one place to another place. The complexity of the QCA circuit is decided by the type of crossover in QCA nanotechnology. Possibly, there are two categories of crossover: single and multiple layers [11]. A coplanar mechanism, where applied clock phases are separated by 90°, is a single-layer crossover. Another mechanism for single-layer QCA circuits is the application of 45° and 90° cells for the QCA wires. QCA circuit provides the facility to design the circuits in multiple layers in order to access the different locations. The physical implementation of multiple layers is quite difficult.

QCA nanotechnology consists of inverter and majority gate as the fundamental logic circuits [12]. There are various kinds of inverter and majority gate designs in QCA nanotechnology depending on the number of QCA cells and configurations. A simple inverter can be designed in a corner-to-corner configuration. The simplest majority gate is 3-input, where 2-input AND and OR functions can be designed in order to develop any digital circuit [13]. A corner-to-corner configuration of an inverter and a 3-input majority gate is shown in Fig. 3.

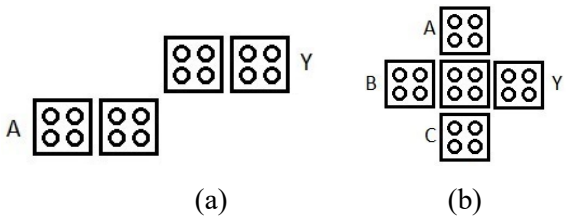


Fig. 3. Fundamental logic: (a) inverter, (b) 3-input majority gate

The target of this research paper is to develop an XOR3 gate with minimum QCA cells. The XOR operation is broadly used in many applications, including parity generator, adder, code converters, etc. Hence, an efficient design of the XOR gate provides performance improvement of the several digital circuits over the parameters. The proposed XOR3 gate is designed with the specific cell arrangement and the utilization of adequate clock phases. The proposed XOR3 gate is checked for the different parameter's performance and the comparison with the existing counterparts. Fault-tolerant analysis is done for a single cell missing and addition defects of the proposed XOR3 gate. Further, a 4-bit parity generator, a 4-bit full adder, and a 4-bit binary to gray code converter are also designed with the support of the proposed XOR3 gate. All the proposed designs are single-layered and have the capability of easy extension. The QCA Designer-E tool is used for the design and analysis of the proposed circuits. The brief of the contribution of this research article is given as follows:

- Unique configuration of 3-input XOR gate, which consists of only 8 QCA cells
- Fault-tolerant and energy dissipation analysis of the proposed XOR3 gate
- Design of 4-bit parity generator, 4-bit full adder, and 4-bit binary to gray code converter using the proposed XOR3 gate
- The suggested designs are easy to use for higher-order circuits

The rest of this research paper is categorized as follows: Section 2 briefs the existing XOR3 gates in the literature. The proposed XOR3 gate is developed and analysed in section 3. The modular circuit designs using the proposed XOR3 gate are presented in section 4. The comparative analysis of the proposed circuits is presented in section 5. Section 6 highlights the conclusion of this research work.

2 Existing XOR3 gates in QCA nanotechnology

This section introduces and highlights the existing XOR3 gate in QCA nanotechnology. Due to the importance of the XOR gate, many efforts by the researchers are done to generate the functionality of the XOR gate in QCA nanotechnology. The key works related to the XOR3 gate are presented with the QCA schematics for easy understanding. The number of QCA cells and the number of clock phases for the XOR3 gate in QCA nanotechnology are identified and mentioned in this section.

An efficient design of a 3-input XNOR gate was developed using 9 QCA cells and 0.5 clock delay [14]. The XOR3 gate can be generated by inverting the output of the XNOR gate. Therefore, the XOR3 gate consists of 11 QCA cells and a 0.50 clock delay. The QCA schematic of the XOR3 gate is shown in Fig. 4(a). An XOR3 gate was suggested in QCA nanotechnology, which uses the explicit interaction of the cells [15]. The suggested XOR3 gate contains a total of 12 QCA cells and a 0.50 clock delay. The QCA schematic of the suggested XOR3 gate is shown in Fig. 4(b). A total of 12 QCA cells and a 0.50 clock delay were required to design an XOR3 gate in QCA nanotechnology [16]. The QCA schematic of the investigated XOR3 gate is presented in Fig. 4(c). A cell interaction-based XOR3 gate was proposed in QCA nanotechnology [17]. The proposed XOR3 gate comprises a total of 17 QCA cells and a 0.50 clock delay. The proposed XOR3 gate is depicted in Fig. 4(d).

A QCA-based XOR3 gate was investigated with a total of 10 QCA cells and a 0.50 clock delay [18]. The QCA schematic for the investigated XOR3 gate is shown in Fig. 4(e). Another XOR3 gate was suggested using 10 QCA cells and a 0.50 clock delay [19]. The QCA schematic for the suggested XOR3 gate is displayed in Fig. 4(f). A novel structure of the XOR3 gate was suggested [20]. The novel structure of XOR3 consists of 14 QCA cells and a 0.50 clock delay. Figure 4(g) shows the QCA schematic of the suggested XOR3 gate. A half distance-based XOR3 gate was developed using cell interaction in QCA nanotechnology [21]. The developed XOR3 gate contains a total of 14 cells and a 0.50 clock delay. The QCA schematic for the XOR3 gate is shown in Fig. 4(h).

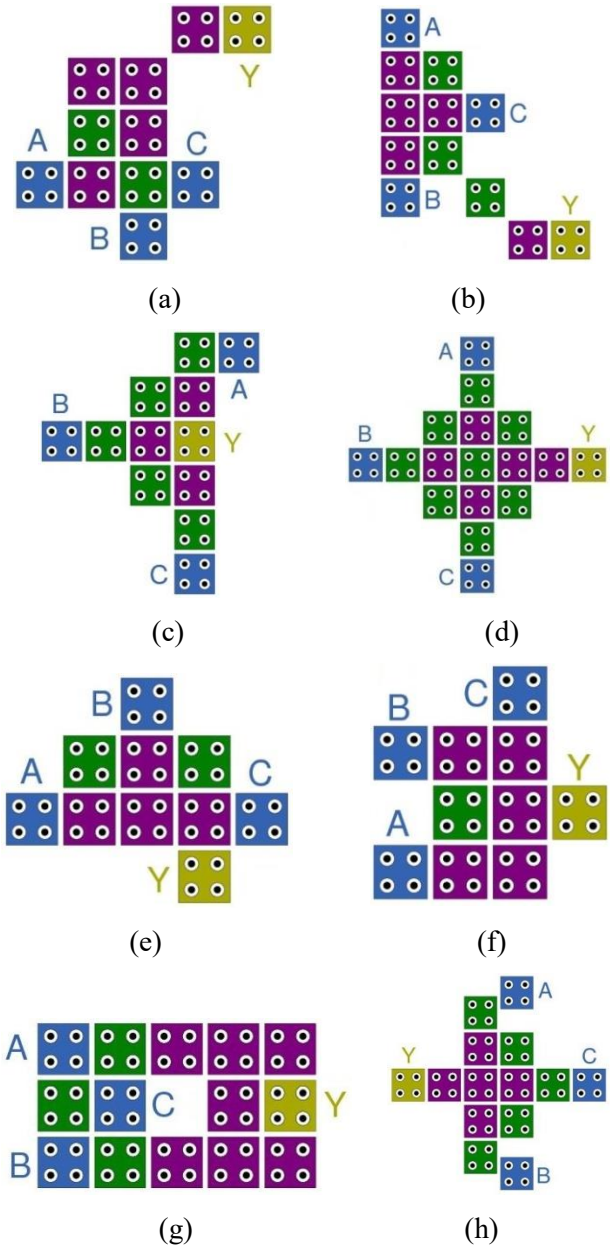


Fig. 4. XOR3 gate in (a) [14], (b) [15], (c) [16], (d) [17], (e) [18], (f) [19], (g) [20], (h) [21]

3 Proposed XOR3 gate

In order to make an efficient system design, fundamental elements pay key attention. The XOR gate is commonly used in many arithmetic and logical operations. Therefore, an effective design of an XOR gate is a prime requirement for the higher-level of systems. This section initially proposes an efficient and optimized QCA-based design of the XOR3 gate. The idea of design is the explicit interaction of QCA cells, which causes a minimum cell-based XOR3 design. The XOR gate produces logic 1 if there are an odd number of 1's in a sequence. The truth table of the XOR3 gate is given in Tab. 1, where A, B, and C are the inputs and Y is the output.

Table 1. Truth table of XOR3 gate

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The logical function of the XOR3 gate is obtained from Tab. 1. The output Y is related to inputs A, B, and C as given in Eqn. (1).

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \otimes B \otimes C \quad (1)$$

The QCA schematic and the output waveforms of the proposed XOR3 gate are depicted in Fig. 5. A bistable approximation simulation engine with default values is utilized for the schematic and output waveforms.

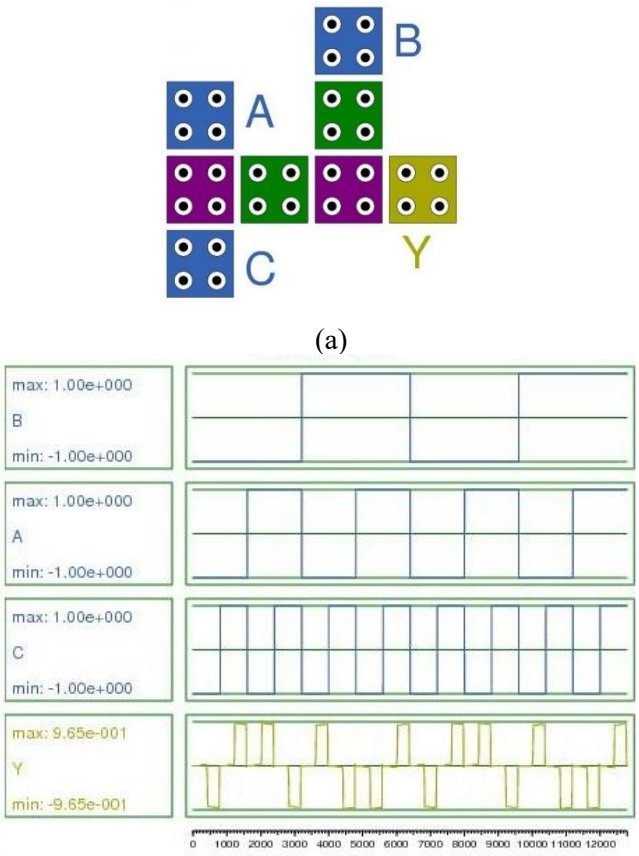


Fig. 5. Proposed XOR3 gate: (a) QCA schematic, (b) output waveforms

The proposed XOR3 gate consists of only 8 QCA cells and a 0.50 clock delay. The QCA schematic occupies an area of 0.005 μm^2. The output Y produces the XOR function of inputs A, B, and C, with the cell interaction. A, B, and C are entered in the first phase of the clock, while Y generates the XOR function in the second phase of the clock.

The fault-tolerant nature of the proposed XOR3 gate is checked for a single cell missing and addition faults. For the calculation of fault-tolerant behavior of the proposed XOR3 gate, a coordinating structure of the proposed XOR3 gate is plotted with the cell numbers. The cell number provides the easy identification of the corresponding cell, where the fault is estimated. Input and output cells are presumed to be in exact positions and do not cause any fault. Figure 6 presents a coordinating structure for the proposed XOR3 gate for fault calculation.

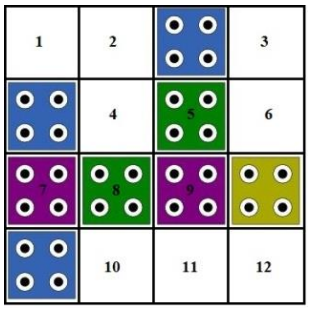


Fig. 6. Coordinating structure of the proposed XOR3 gate for fault calculation

The cells inside the QCA schematic, such as 5, 7, 8, and 9, cause cell missing faults, while the empty cells, i.e., 1, 2, 3, 4, 6, 10, 11, and 12, in the coordinating structure originate the cell addition faults. In a single-cell defect, each cell is observed individually for any fault. Table 2 presents missing and addition cell fault calculations for the proposed XOR3 gate.

Table 2. Fault calculation for the proposed XOR3 gate

Cell	Output	Fault
1	01101001	0
2	01101001	0
3	01101001	0
4	00110011	4
5	01110001	2
6	00001111	4
7	10001110	6
8	00001111	4
9	11110000	4
10	01010101	4
11	00001111	4
12	01101001	0

Table 2 depicts the fault in the output sequence. The output is matched with the exact sequence and estimated the fault. There are a total of 32 faults out of 12 sequences of 8-bit. It reflects 33.33% faults for the proposed XOR3 gate. In terms of reliability, the proposed XOR3 gate is 66.67% fault-tolerant.

The energy dissipation of the proposed XOR3 gate is also performed using the QCA Pro tool at different kink energy levels [22]. The energy dissipation analysis is necessary to check the energy-efficient behavior of the QCA circuits. The power maps are exported from the QCA Pro tool for different kink energy levels. Figure 7 depicts the power maps for the proposed XOR3 gate at different kink energy levels.

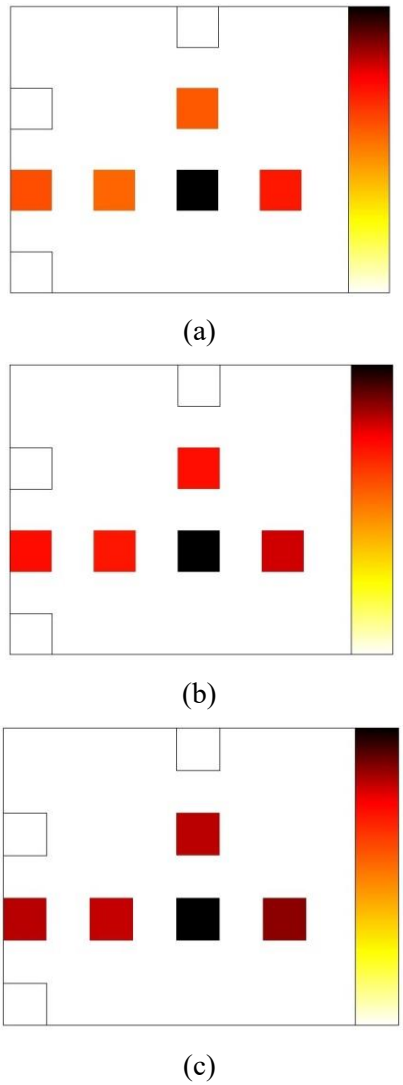


Fig. 7. Power maps for the proposed XOR3 gate at kink energy level of (a) 0.5 (b) 1.0 (c) 1.5.

The proposed XOR3 gate is easily converted to a 2-input XOR gate by fixing any input at -1 polarization and acts as a 2-input XNOR gate by fixing any input at +1 polarization. Similarly, higher inputs XOR and XNOR operations can be generated by cascading the stages of the proposed XOR3 gates in a suitable manner with reduced numbers of QCA cells. A 3-input exclusive NOR (XNOR) is the inverted form of XOR3 logic and is also used in many applications. An XNOR produces logic 1 if the number of 1's in the input sequence is even. The operation of the XNOR3 gate can easily be generated using the proposed XOR3 gate. One input is inverted in the XOR3 gate to make the output for the XNOR3 gate. The logical function for the output of the XNOR3 gate is provided in Eqn. (2).

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}C = \overline{A \otimes B \otimes C} \quad (2)$$

The proposed XNOR3 gate also consists of 8 QCA cells and a 0.50 clock phase. The QCA schematic for the XNOR3 gate and the output waveforms are shown in Fig. 8.

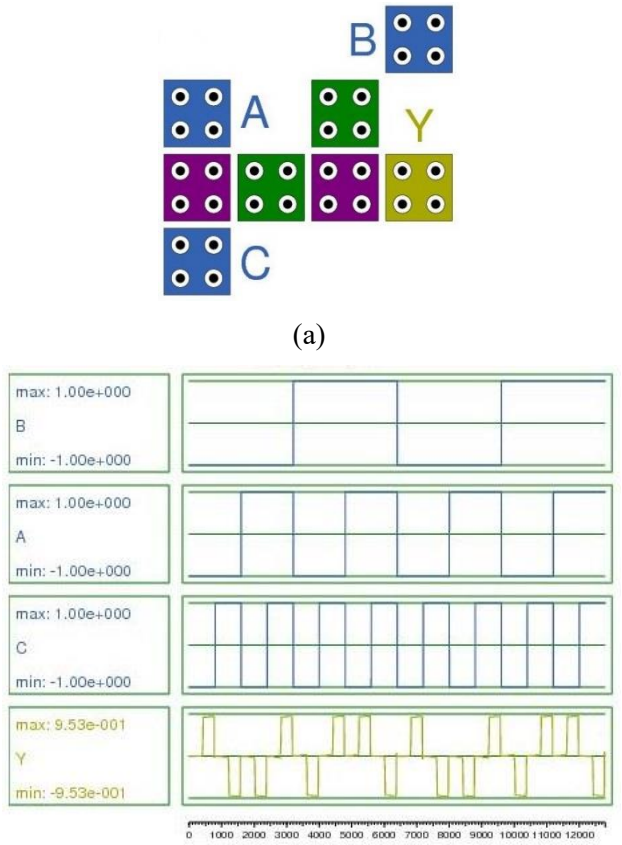


Fig. 8. Proposed XNOR3 gate: (a) QCA schematic, (b) output waveforms

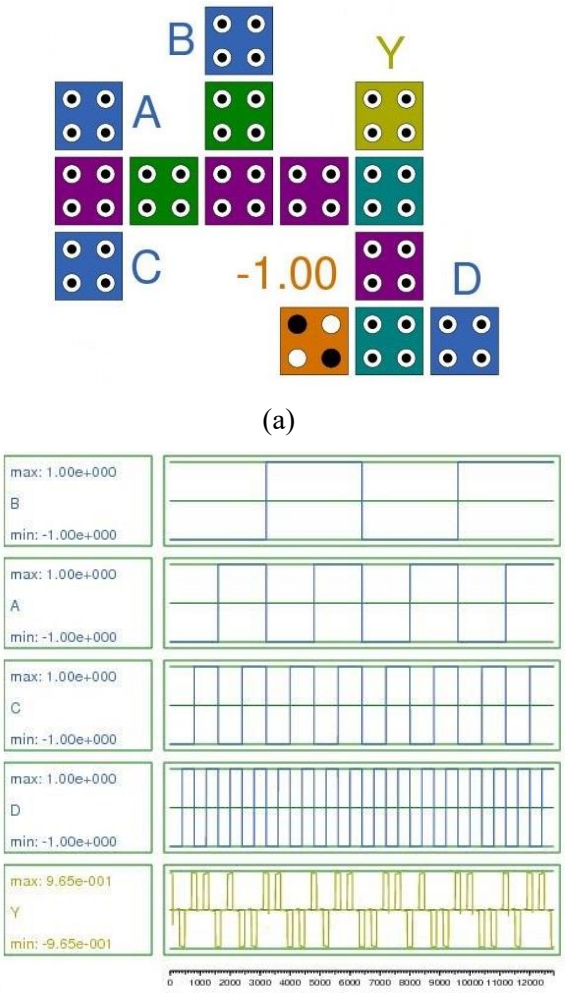


Fig. 9. 4-input even parity generator: (a) QCA schematic, (b) output waveforms

4 Proposed modular designs

The possibility of implementation of other logic applications using the proposed XOR3 gate is explored in this section. This section includes the designs of a 4-bit parity generator, a single-bit full adder, a 4-bit full adder, and a 4-bit binary to gray code converter using the proposed XOR3 gate. The correct responses of the implemented QCA circuits are provided using the bistable approximation engine in the QCA Designer-E tool.

4.1 Four-bit parity generator

The parity generators are needed in the field of data communication. A 4-bit parity generator is designed using the two proposed XOR3 gates, as shown in Fig. 9(a).

The proposed 4-bit parity generator contains only 14 QCA cells and a 0.75 clock phase. A 4-bit even parity generator is a 4-input XOR operation. The logical function of the 4-bit even parity generator is mentioned in equation (3).

$$Y = A \otimes B \otimes C \otimes D \tag{3}$$

In Eqn. (3), Y is the output and A, B, C, D, are the inputs for the parity generator. The QCA schematic and output waveform for the 4-bit even parity generator are depicted in Fig. 9. Figure 9(b) shows the accurate implementation of the 4-bit parity generator.

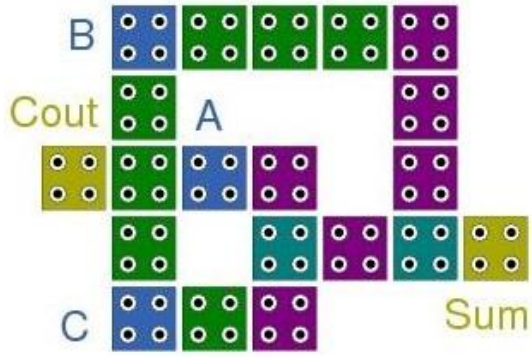
4.2 Single-bit full adder

A single-bit full adder using the proposed XOR3 gate is implemented in QCA nanotechnology. The sum output of the full adder is the output of the proposed XOR3 gate, while the carry output is the output of a 3-input majority gate. The logical functions for sum and carry outputs are given in equations (4) and (5), respectively.

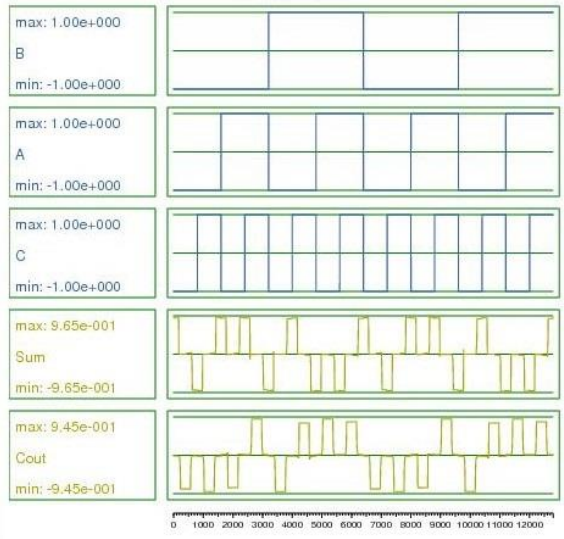
$$Sum = A \otimes B \otimes C \tag{4}$$

$$Cout = AB + BC + AC \tag{5}$$

The implemented full adder consists of only 20 QCA cells and a 0.75 clock phase. The configuration of the proposed full adder is simple and easy to understand for the sum and carry outputs. The sum output is the XOR3 operation, while carry output is the majority operation of three inputs. The QCA schematic and the input-output waveforms of a single-bit full adder are given in Fig. 10.



(a)



(b)

Fig. 10. Proposed single-bit full adder: (a) QCA schematic, (b) output waveforms

4.3 Four-bit full adder

The proposed single-bit full adder can also be extended for higher-bit input signals. A 4-bit ripple carry adder is implemented using the proposed single-bit full adder, as shown in Fig. 11. It consists of only 92 QCA cells and 2 clock phases. The stages of the 4-bit full adder are connected one-by-one in order to accurately propagate the carry input. The structure of the 4-bit full adder can be utilized for the implementation of other higher-order full adders.

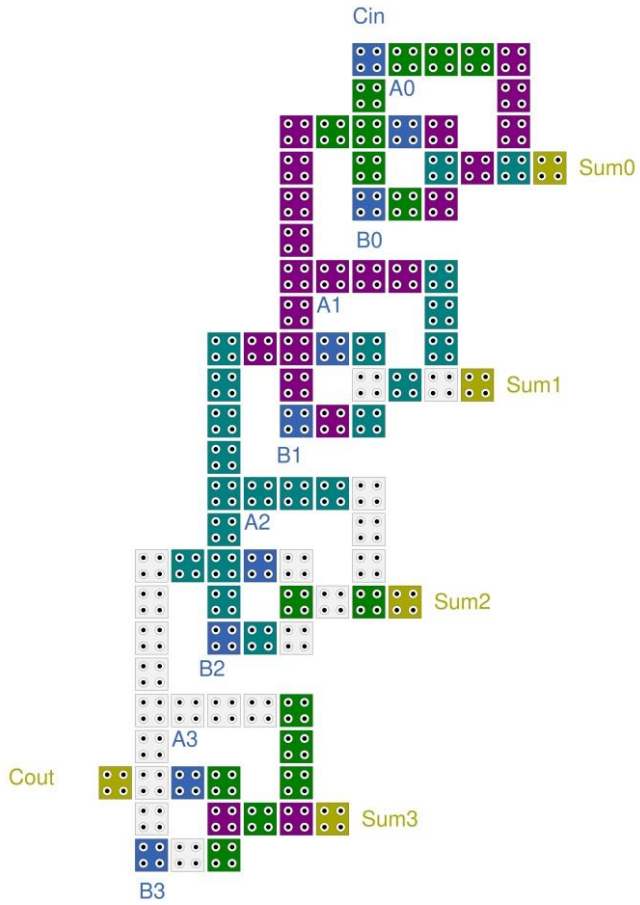
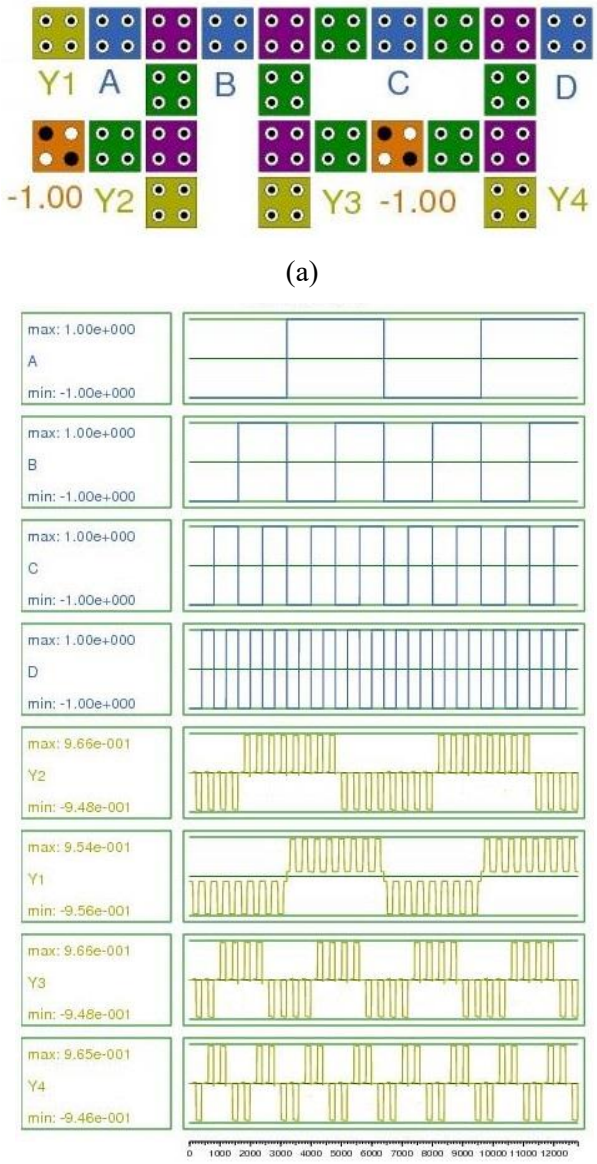


Fig. 11. Proposed 4-bit full adder

4.4 Four-bit binary to gray code converter

A 4-bit binary to gray code converter is also implemented using the proposed XOR3 gate. 24 QCA cells and 0.50 clock phases are utilized for the design of the 4-bit binary to gray code converter. The schematic diagram and output waveforms for the 4-bit binary to gray code converter are presented in Fig. 12. Figure 12(b) reflects the proper implementation of the binary to gray code converter.



(a)

(b)

Fig. 12. Proposed 4-bit binary to gray code converter: (a) QCA schematic, (b) output waveforms

5 Comparison results

This section discusses the comparative results of the proposed QCA-based structures with the existing similar type of designs. The various performance parameters in QCA nanotechnology are compared. The number of QCA cells, clock phases, cell area, layout area, % area utilization, and design cost, are considered for evaluating the performance criteria. The QCA Designer-E tool with the bistable approximation engine is utilized for the fair estimation of the proposed works. Table 3 lists the comparative results of the XOR3 gate.

Table 3 illustrates that the proposed XOR3 gate outperforms in terms of QCA cell count and cell area. The proposed XOR3 gate has only 8 QCA cells and improves the cell count by 20% in comparison with the best-reported XOR3 gate [18, 19]. All the XOR3 designs are have two clock phases for generating the precise logic functionality. The layout area depends on the number of horizontal and vertical plane cells. The structure of the QCA circuit causes a distinct layout area irrespective of the equal number of QCA cells. The cell area to layout area ratio is noted as area utilization. The design cost is measured as per Eqn. (6) [23].

$$Design\ cost = layout\ area \times Clock^2 \tag{6}$$

The comparative analysis of the other modular circuits is also given in this section. The proposed 4-bit parity generator is compared with the existing similar type of designs, and the results are noted in Tab. 4 for the same set of parameters.

Table 3. Comparative results of the XOR3 gate

XOR3	Cells	Clock	Cell area (μm^2)	Layout area (μm^2)	% area utilization	Design cost
[14]	11	0.50	0.0036	0.0081	44	0.0020
[15]	12	0.50	0.0039	0.0097	40	0.0024
[16]	12	0.50	0.0039	0.0097	40	0.0024
[17]	17	0.50	0.0055	0.0159	34.69	0.0040
[18]	10	0.50	0.0032	0.0065	50	0.0016
[19]	10	0.50	0.0032	0.0052	62.50	0.0013
[20]	14	0.50	0.0045	0.0049	93.33	0.0012
[21]	14	0.50	0.0045	0.0117	38.89	0.0029
Proposed	8	0.50	0.0026	0.0052	50	0.0013

Table 4. Comparative results of the 4-bit parity generator

Parity generator	Cells	Clock	Cell area (μm^2)	Layout area (μm^2)	% area utilization	Design cost
[24]	76	1.75	0.0246	0.0674	36.54	0.2064
[25]	37	1.50	0.0120	0.0389	30.83	0.0875
[26]	86	1.50	0.0279	0.0800	34.82	0.1800
[27]	19	0.75	0.0062	0.0156	39.58	0.0088
[28]	92	1.75	0.0298	0.0875	34.07	0.2680
[29]	85	1.25	0.0275	0.0778	35.42	0.1216
Proposed	14	0.75	0.0045	0.0097	46.67	0.0055

Table 4 depicts that the proposed 4-bit parity generator has improved the performance metrics in terms of cell count, clock, cell area, layout area, % utilization of area, and the design cost. The proposed 4-bit parity generator is a single-layer implementation. The design presented in [26] is a multi-layer implementation. The comparative simulation results of the proposed 4-bit full adder are provided in Tab. 5.

Table 5. Comparative results of the 4-bit full adder

Full adder	Cells	Clock	Cell area (μm^2)	Layout area (μm^2)	% area utilization	Design cost
[15]	156	2.25	0.0505	0.1516	33.33	0.7675
[21]	269	3.50	0.0872	0.2974	29.30	3.6432
[28]	256	1.50	0.0829	0.3428	24.20	0.7713
[30]	125	2.75	0.0405	0.1264	32.04	0.9559
Proposed	92	2.00	0.0298	0.0969	30.75	0.3876

Table 5 shows that the proposed 4-bit full adder improves the cell count by 26.40% in comparison with the best-reported design [30]. The design cost is improved by 49.50% with respect to the best-reported design [15]. The proposed 4-bit binary to gray code converter is also compared for the performance parameters, and the simulation results are presented in Tab. 6. The design presented in [26] is a multi-layer design, while the others are single layers.

Table 6. Comparative results of the 4-bit binary to gray code converter

Binary to gray code	Cells	Clock	Cell area (μm^2)	Layout area (μm^2)	% area utilization	Design cost
[19]	29	0.50	0.0094	0.0181	51.79	0.0045
[26]	99	0.75	0.0321	0.0674	47.60	0.0379
[31]	92	0.75	0.0298	0.0674	44.23	0.0379
Proposed	24	0.50	0.0078	0.0130	60	0.0032

The energy dissipation of the proposed XOR3 gate is also compared and listed in Tab. 7 using the QCA Pro tool. The total energy dissipation is the overall addition of the switching and leakage energy dissipation. All three kink energy levels are mentioned for the average energy dissipation comparison.

Table 7. Average energy dissipation for the XOR3 gate using the QCA Pro tool

Design	Leakage (meV)			Switching (meV)			Total (meV)		
	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
[14]	3.94	9.79	15.90	6.77	5.41	4.42	10.71	15.20	20.32
[16]	1.54	4.85	8.27	10.58	9.32	8.02	12.11	14.17	16.28
[17]	7.30	17.77	28.56	8.61	6.57	5.15	15.91	24.34	33.71
[18]	2.57	7.14	12.31	11.08	9.63	8.33	13.65	16.77	20.64
[19]	2.73	7.28	12.46	10.41	9.09	7.83	13.14	16.37	20.29
Proposed	2.26	5.94	9.82	4.67	3.66	2.92	6.93	9.60	12.74

It can be seen from Tab. 7 that the proposed XOR3 gate diminishes total energy dissipation in comparison with the existing XOR3 gates. The proposed XOR3 gate reduces the total energy dissipation by 42.77%, 32.25%, and 21.74% as compared to the best-reported design [16] at 0.5, 1.0, and 1.5 kink energy levels, respectively.

The energy dissipation values using the QCA Designer-E tool with the default values of the coherence vector simulation engine are also presented for the proposed XOR3 gate along with the existing designs. Table 8 shows the average and total energy dissipation for the XOR3 gate. A QCA cell comprises input, output, and environmental energy dissipation components. The environmental component appears during the logic transition between the cells.

Table 8. Comparative results of energy dissipation using the QCA Designer-E tool for the XOR3 gate

XOR3	Average (meV)	Total (meV)
[14]	0.965	10.5
[15]	0.670	7.37
[16]	1.82	20.0
[17]	2.18	24.0
[18]	0.398	4.38
[19]	0.960	10.5
[20]	1.45	15.9
[21]	0.974	10.61
Proposed	0.947	10.4

6 Conclusion

QCA nanotechnology is the suitable alternative to MOSFET technology to overcome the nanoscale design challenges. MOSFET technology possesses many restrictions to apply them for future nanoscale circuits. The XOR gate plays an important role in building many digital applications. Hence, an efficient, optimized, and fault-tolerant XOR3 gate is proposed in this paper. The available XOR3 gates are compared with the proposed gate for various design parameters and energy dissipation. The QCA Designer-E and QCA Pro tools are applied for QCA schematics, verification, and power maps. The analyses for different modular designs are also presented in the paper, which shows an easy configuration of the proposed XOR3 gate and circuits that can be designed using the proposed XOR3 gate. The design costs are improved by 37.50%, 49.50%, and 28.89% w.r.t. the best-reported similar works in the proposed 4-bit parity generator, 4-bit full adder, and 4-bit binary to gray code converter, respectively. The proposed units can be implemented in processor design to make it more energy-efficient for nanocomputation.

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