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G_m-C simulation of floating frequency-dependent negative conductance and applications to active LC ladder filter

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This paper presents a simulator for floating frequency-dependent negative conductance (FDNC) using the G_m-C technique with adjustable transconductance cells and grounded capacitors. The proposed configuration eliminates the need for passive resistors and component matching, resulting in a compact, resistorless design highly suitable for IC integration. The FDNC circuit offers precise electronic tunability of the equivalent M-element via external bias currents, which makes it particularly beneficial for processing analog signals. To validate its functionality, the proposed FDNC is applied to implement second-order low-pass and fourth-order band-pass active ladder filters. Simulations with TSMC 0.18-µm CMOS technology confirm the electronic tunability of M-element values between 1.95 nF/s and 18.22 nF/s, as well as filter cutoffs, demonstrating frequency operation from 20 kHz to 300 kHz. The design exhibits high accuracy, low component sensitivity, and excellent compatibility with integrated circuit realization, thereby representing a robust solution for modern analog filter synthesis.

Keywords: G_m-C technique, Frequency-Dependent Negative Conductance (FDNC), transconductance amplifier, ladder filter, immittance function

1 Introduction

Frequency-dependent negative conductance (FDNC) is an indispensable active component in the design of advanced circuits for analog signal processing and various applications [1]. This element is especially valuable in the synthesizing active ladder filters and has found applications in the development of nonlinear systems, such as chaotic oscillators [2]. Over the past decades, numerous approaches have been proposed to implement FDNC circuits using diverse types of active building blocks [3-13]. Nonetheless, many of these methods encounter practical limitations, including reliance on component matching conditions, utilization of floating passive elements, or the requirement for an extensive array of active devices.

For instance, the FDNC configurations in [3-5] utilize three current conveyors and demand precise component matching. Likewise, the FDNC structure in [6] necessitates multiple passive components and exhibits similar matching constraints. In [8, 9], floating FDNC simulators that utilize current-feedback operational amplifiers (CFOAs) as active components were proposed; however, these designs need four CFOAs and five passive elements. Additionally, within the same CFOA platform, seven different lossy floating FDNC simulators were introduced in [10, 11], each using two or three CFOAs along with three passive elements. The FDNC proposed in [13] is a compact, resistorless architecture; however, it is designed in a grounded configuration. Furthermore, some techniques [3, 7-12] employ floating resistors and cap-citors, which are not ideal for integrated circuit (IC) realization due to poor layout compatibility and parasitic effects. In filter theory, the M-element represents a synthetic immittance component used in ladder filter realizations. It provides a frequency-dependent negative conductance characterristic that behaves similarly to an inductive element in certain configurations. This synthetic element allows passive ladder prototypes to be transformed into active, tunable filter structures without requiring bulky physical inductors, making it parti-cularly valuable for integrated circuit applications.

The transconductance amplifier (G_m cell) has emerged as a highly versatile building block for analog circuit design, which facilitates electronically tunable implementation of various active functions. It serves as a fundamental element in modern devices such as current differencing transconductance amplifier (CDTA), voltage differencing transconductance amplifier (VDTA), current conveyor transconductance amplifier (CCTA), and full-balanced voltage differencing buffered amplifier (FB-VDBA) [14, 15]. G_m-C architectures are particularly advantageous for IC implementations, primarily due to their low power

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consumption, compact silicon area, and high electronic tunability. By eliminating floating passive elements and utilizing only on grounded capacitors, these designs effectively reduce parasitic effects and simplify layout, making them ideal for scalable and low-noise analog signal processing applications. The inherent electronic tunability of G_m cells makes these components excellent choices for applications in gain control circuits, analog multipliers, and continuous-time filters. Recent trends in analog IC design emphasize the importance of compact, low-power, and electronically controllable architectures. The preference for using only grounded capacitors and elimination of floating passive resistors is particularly desirable for minimizing chip area and improving noise immunity in CMOS implementations.

Motivated by these advantages, this study presents a floating FDNC configuration realized solely with G_m-cells and grounded capacitors. The proposed circuit eliminates the need for passive resistors and component matching, resulting in a resistorless, canonical structure that is well-suited for integration. Importantly, the equivalent M-element value of the simulator can be accurately tuned via external bias currents. To validate the theoretical framework, the proposed design is applied to second-order Butterworth low-pass (LP) and fourth-order band-pass (BP) filters, and their performances are then verified through PSPICE simulation with TSMC 0.18-μm CMOS technology. By leveraging the simplicity and electronic controllability of G_m-C based design, the proposed FDNC circuit contributes not only to fundamental circuit theory but also to practical applications in tunable filter design and analog signal synthesis.

2 Proposed floating FDNC configuration

Figure 1 depicts a straightforward CMOS implementtation of the tunable G_m cell, which forms the core circuit of the proposed design. The circuit primarily consists of a floating current source [16]. The transconductance value (G_m) for this component can be ascertained from the transconductance of the output transistor, which can be estimated as:

$$G_m = \frac{i_o}{\left(v^+ - v^-\right)} = \left(\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}}\right) + \left(\frac{g_{m3}g_{m4}}{g_{m3}+g_{m4}}\right), \quad (1)$$

and

$$g_{mi} = \sqrt{K_{n(p)} I_B}\,, \ (i = 1, 2, 3, 4). \quad (2)$$

In above expressions, g_{mi} denotes the transconductance of the transistor M_i, and K_n and K_p represent the transconductance parameter for NMOS transistors M_1 and M_2, as well as PMOS transistors M_3 and M_4, respectively. Additionally, I_B refers to an external DC bias current used in this configuration. It is important to note that in Eqns. (1, 2), the value of G_m can be electronically modified by altering the bias current I_B.

In the tunable G_m cell shown in Fig. 1, the floating current source plays a key role in the overall FDNC design. Because the current source is floating (not referenced to ground), the G_m cell can provide symmetrical current outputs that can be connected between arbitrary nodes in the circuit. This feature enables accurate realization of floating impedances, which is critical for the FDNC configuration. Moreover, the floating structure simplifies biasing and allows wide-range electronic tuning of G_m through the control current, thereby enhancing linearity, tunability, and adaptability of the proposed FDNC topology to different frequency ranges.

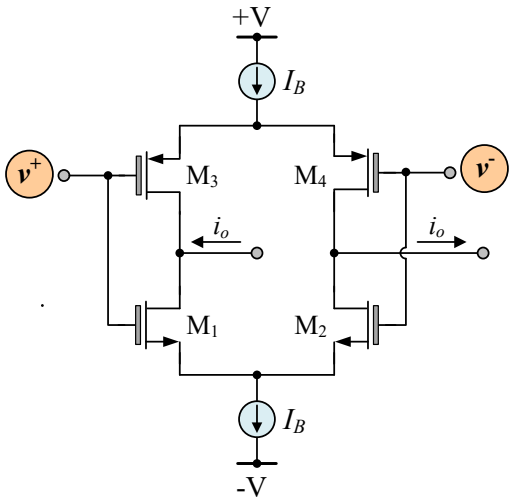


Fig. 1. Tunable G_m cell

Figure 2 shows the schematic diagram of an electronically tunable floating FDNC realization and its symbolic representation, which is based on three G_m-cells depicted in Fig. 1 and two grounded capacitors. Notably, as indicated in Fig. 2(a), this configuration employs only 12 MOS transistors and all-grounded capacitors. This design achieves a resistorless and canonical structure. The analysis of the configuration illustrated in Fig. 2 provides the following simulated floating impedance:

$$Z_{in}(s) = s^2 M = s^2 \left(\frac{C_1 C_2}{G_{m1} G_{m2} G_{m3}}\right). \quad (3)$$

In Eqn. (3), M denotes the equivalent immittance value, commonly referred to as the M-element, which characterizes the strength of the frequency-dependent negative conductance in the FDNC circuit. This parameter is key in ladder filter synthesis, where

the M-element serves as a tunable, active substitute for inductive components, enabling compact and electronically adjustable filter designs. Therefore, from equation (3), the equivalent M-element value is easily obtained as:

$$M = \frac{C_1 C_2}{G_{m1} G_{m2} G_{m3}}, \tag{4}$$

and its schematic representation can also be shown in Fig. 2(b).

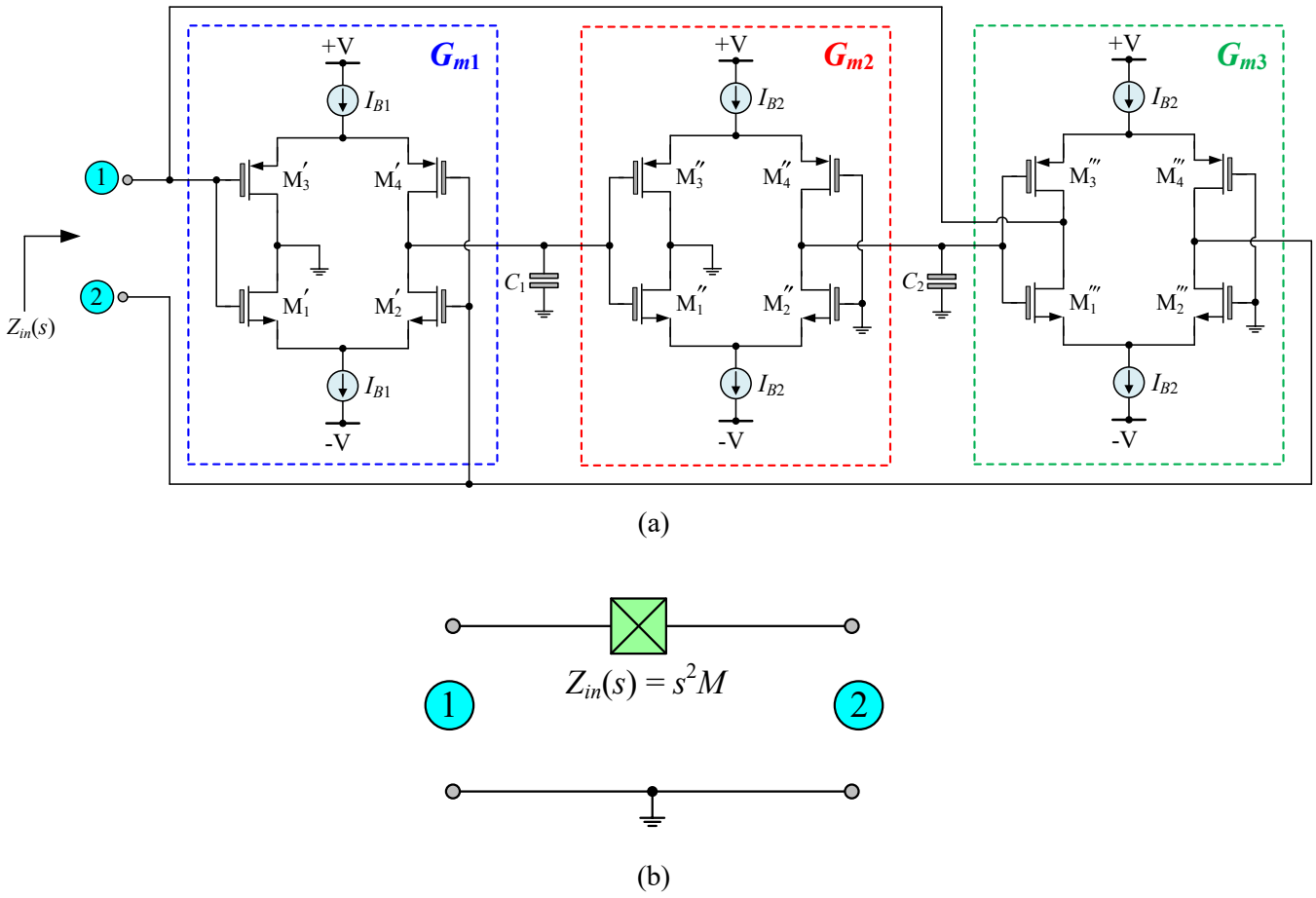


Fig. 2. Proposed floating DNC circuit: (a) CMOS circuit implementation; (b) symbolic representation

As discussed above, the realized FDNC is particularly advantageous for its electronic controllability, achieved through the adjustment of G_{mk} ($k = 1, 2, 3$). This circuit consists solely of G_m cells and grounded capacitors, thereby making it suitable for IC implementation. In the circuit presented, the desired floating impedance function is realized without the need for component matching or cancellation constraints.

According to Eqn. (3), the sensitivities of the proposed FDNC circuit regarding both active and passive circuit components are evaluated. The sensitivity figures for G_{mk}, C_1, and C_2 are all low and can be expressed as follows:

$$S_{G_{m1}}^{M} = S_{G_{m2}}^{M} = S_{G_{m3}}^{M} = -1, \tag{5}$$

and

$$S_{C_1}^{M} = S_{C_2}^{M} = 1. \tag{6}$$

3 Performance simulations

This section evaluates the performance of the proposed FDNC circuit in Fig. 2 through numerical simulation. The tunable G_m cell was simulated using the schematic CMOS design shown in Fig. 1(a) with DC bias voltages set to ±0.9 V. Simulations were conducted with PSPICE program, which is based on TSMC 0.18-μm CMOS real process parameters. The dimensions W(μm)/L(μm) of the MOS transistors employed in the G_m cell implementation are specified as (24 μm /0.18 μm) for M_1-M_2, and (30 μm /0.18 μm) for M_3-M_4.

The simulated frequency responses of the input impedance Z_{in} for the proposed FDNC circuit in Fig. 2 are presented in Fig. 3. These responses are derived from varying the bias current I_B and are compared with the expected results. The synthetic floating FDNC is

realized with $C_1 = C_2 = 1$ nF, and $I_B = I_{B1} = I_{B2} = I_{B3}$ (where $G_m = G_{m1} = G_{m2} = G_{m3}$). By adjusting I_B to 40 μA, 100 μA, and 200 μA, the corresponding equivalent M-element values are determined to be 18.22 nF/s, 4.63 nF/s, and 1.95 nF/s, respectively. Figure 3 confirms that the circuit operates effectively over 20 kHz to 300 kHz. Additionally, the simulation results are closely aligned with the expected values and confirm that the Z_{in} values can be precisely adjusted by varying the biasing current I_B.

4 Applications to active ladder filter design

4.1 Second-order Butterworth LP filter

To demonstrate the application of the floating FDNC realization illustrated in Fig. 2 and to assess its performance, a second-order Butterworth LP ladder filter, as shown in Fig. 4(a), is selected as a prototype network. This filter design is known for its smooth frequency response and minimal ripple in the passband. By implementing the floating FDNC structure, we can analyze the filter's stability and frequency characteristics under various load conditions. The simplified version of the normalized RLC passive prototype of Fig. 4(a) for $\omega_c = 2\pi f_c = 1$ rad/s employs the following component values: $R_s = R_L = 1$ Ω, $L_1 = 1.414$ H, and $C_2 = 1.414$ F [17].

Parameters k_m and k_f are scaling factors introduced to simplify the design and analysis of the proposed circuit. Specifically, k_m is the magnitude scaling factor that adjusts the impedance or admittance level of the circuit without affecting its frequency characteristics. This is particularly useful for matching the design to practical component values or optimizing power consumption and area. Similarly, k_f is the frequency scaling factor, which allows the desired frequency response to be shifted or tuned to a different frequency band without altering the normalized characteristics of the design. By applying k_f, the design equations derived for normalized frequencies can be directly scaled to meet practical frequency specifications, enabling easier implementation and adaptability to various applications.

To achieve a practical cutoff frequency of $f_c = 159$ kHz, the variable impedance scaling method with a magnitude scaling constant of $k_m = 10^2$ and a frequency scaling constant of $k_f = 10^6$ has been applied. Consequently, the component values in Fig. 4(a) will be scaled to $R_s = R_L = 100$ Ω, $L_1 = 0.14$ mH, and $C_2 = 14.14$ nF. Using a network transformation method for *RLM* simulation of the *RLC* passive prototype, the equivalent *RLM* version is shown in Fig. 4(b), where the M-element is designed with FDNC in Fig. 2 using $I_B = 230$ μA ($G_m = 0.88$ mA/V) and $C_1 = C_2 = 1$ nF. Thus, by multiplying the scaling factors $k_m = 10^3$ and $k_f = 10^6$, the component values for the derived *RLM* network in Fig. 4(b) are determined to be $L_{Rs} = L_{RL} = 1$ mH, $M_1 = 1.414$ nF/s, and $R_{C2} = 1.414$ kΩ.

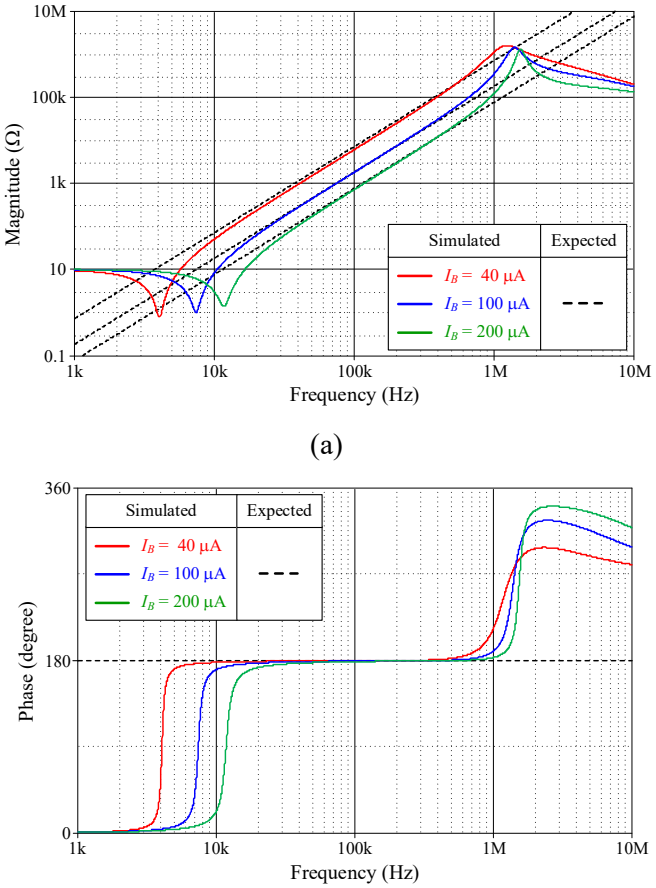


Fig. 3. Expected and simulated frequency responses of the synthetic FDNC circuit in Fig. 2: (a) magnitude-frequency behavior; (b) phase-frequency behavior

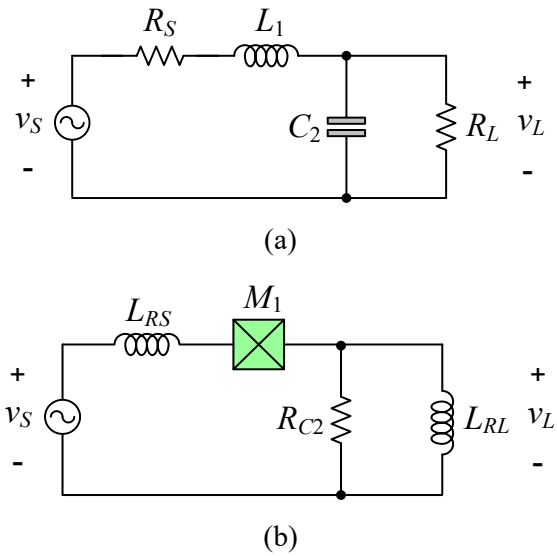
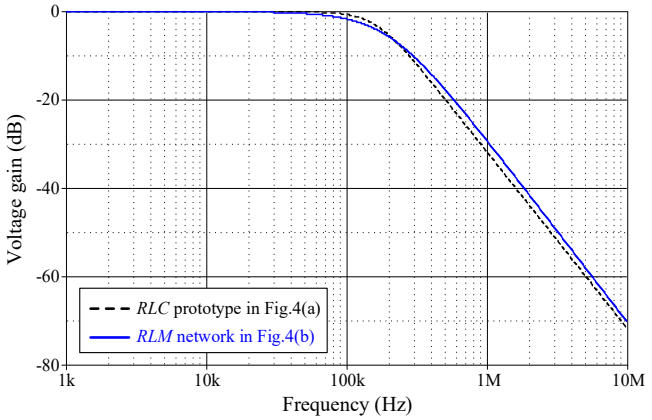
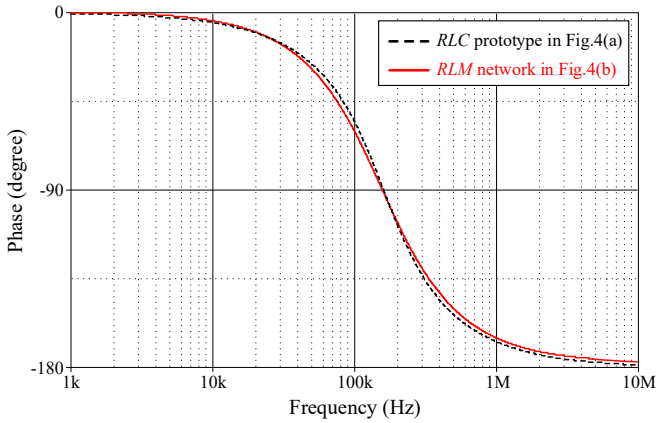


Fig. 4. Second-order Butterworth LP filter: (a) RLC passive prototype; (b) equivalent RLM network with floating FDNC in Fig. 2

Figure 5 depicts the gain- and phase-frequency responses of both filters. The simulated f_c from the *RLM* filter network was observed at approximately 143 kHz, which is close to the design value of 159 kHz. The slight deviation can be attributed to the second-order effects and parasitic element present in the CMOS implementation of the G_m cells, as well as tolerances in capacitor values. Importantly, both gain and phase responses in Fig. 5 exhibit behavior characteristic of a Butterworth filter, with a maximally flat magnitude in the passband and smooth roll-off beyond the cut off. This observation confirms that the FDNC-based implementation preserves the essential features of the original RLC prototype even under practical CMOS-level simulation.



(a)



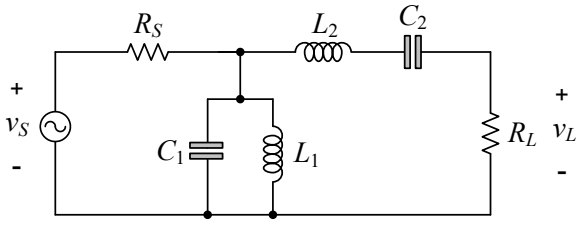
(b)

Fig. 5. Simulated frequency responses of second-order Butterworth LP filters shown in Fig. 4: (a) magnitude-frequency behavior; (b) phase-frequency behavior

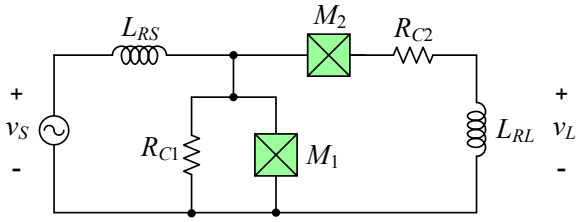
4.2 Fourth-order BP filter

To further demonstrate the applicability of the FDNC realization shown in Fig. 2, the fourth-order BP filter was constructed and simulated. The normalized *RLC* passive prototype is depicted in Fig. 6(a), with the following parameters: $R_S = R_L = 1\ \Omega$, $L_1 = 0.707$ H, $L_2 = 1.414$ H, $C_1 = 1.414$ F, and $C_2 = 0.707$ F [17]. Thus, to obtain the designed f_c of 159 kHz, the *RLC* passive prototype is scaled using $k_m = 3\times10^3$ and $k_f = 10^6$, yielding $R_S = R_L = 3$ kΩ, $L_1 = 2.25$ mH, $L_2 = 4.50$ mH, $C_1 = 0.45$ nF, and $C_2 = 0.225$ nF.

Based on the same network transformation and using $k_m = 10^3$ and $k_f = 10^6$, the design values for the active and passive components in the circuit realization of the transformed RLM network shown in Fig. 6(b) are as follows: $R_{C1} = 1.414$ kΩ, $R_{C2} = 0.707$ kΩ, $L_{RS} = L_{RL} = 976$ µH, $M_1 = 0.456$ nF/s, and $M_2 = 0.914$ nF/s. The *M*-elements in this realization were simulated using FDNC in Fig. 2 with $I_B = 30$ μA ($G_m = 0.31$ mA/V) and $C_1 = C_2 = 0.1$ nF for M_1, and $I_B = 260$ μA ($G_m = 0.99$ mA/V) and $C_1 = C_2 = 1$ nF for M_2.



(a)



(b)

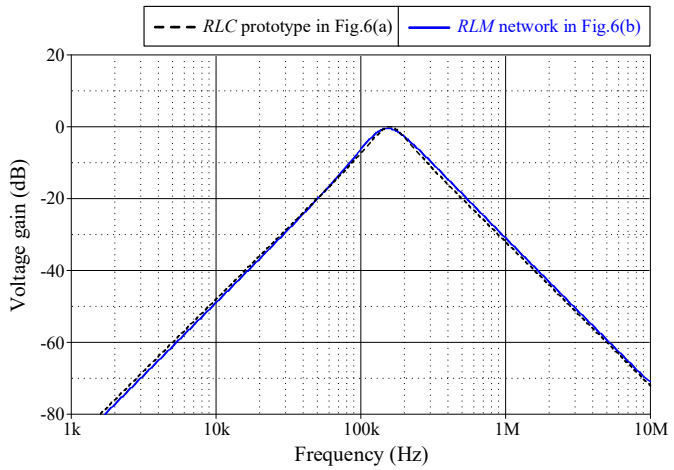
Fig. 6. Fourth-order BP filter: (a) RLC passive prototype; (b) equivalent RLM network with FDNC in Fig. 2

Figure 7 shows the gain and phase response plots of the *RLC* passive BP filter prototype in Fig. 6(a) and the transformed *RLM* network in Fig. 6(b). The simulation results indicate the simulated f_c frequency of 157.2 kHz aligns closely with the intended design frequency of 159 kHz, which validates the accuracy of the FDNC-based *M*-element realization across various frequency bands. The use of two distinct FDNC elements (M_1 and M_2), each tuned by separate bias currents and capacitor values, highlights the versatility and independent controllability of the proposed architecture. Fig. 7 also shows that the sharpness of the BP characteristic, along with minimal deviation in the phase response, further supports the effectiveness of this approach.

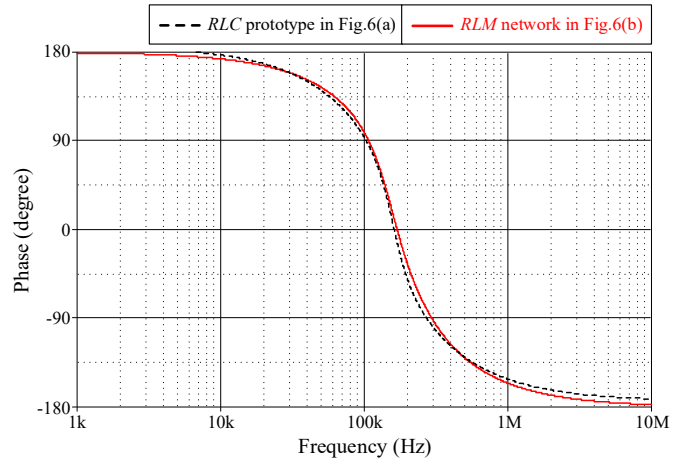
While the FDNC-based filter designs achieve compactness and tunability, future work could investigate the linearity and noise performance under varying biasing conditions, which are critical in precision analog systems.

5 Comparison to conventional approaches

Compared with existing FDNC realizations using CFOAs, current conveyors, or matched resistor–capacitor networks [3-13], the proposed design achieves the following: (i) only three G_m cells and two grounded capacitors are required; (ii) no floating elements, minimizing silicon area and parasitic effects; (iii) efficient biasing of G_m cells reduces overall energy demand; and (iv) electronic control of the M-element enables precise parameter adjustment without redesign. These advantages make the proposed FDNC particularly well-suited for modern IC-based analog signal processing applications, where compactness, power efficiency, and design flexibility are critical.



(a)



(b)

Fig. 7. Simulated frequency responses of fourth-order BP filters in Fig. 6: (a) magnitude-frequency behavior, (b) phase-frequency behavior

6 Conclusions

This paper has introduced a design approach for simulating a floating frequency-dependent negative conductance (FDNC) using a G_m-C configuration composed of solely electronically tunable transconductance amplifiers (G_m-cells) and grounded capacitors. The proposed FDNC circuit is free from passive resistors and component matching requirements, thereby offering a highly suitable canonical resistorless structure for integrated circuit implementation. The equivalent M-element value can be controlled electronically by external bias currents, allowing for precise controllability. Extensive simulations based on TSMC 0.18-µm CMOS parameters verified the theoretical performance of the FDNC, confirming its operational validity over a wide frequency range and its reliable tunability. Furthermore, the proposed FDNC was successfully applied to second-order Butterworth low-pass and fourth-order band-pass ladder filters. The simulated frequency responses of these filters demonstrate close agreement with the expected theoretical results, thus validating the practical applicability of the proposed design. Future work will focus on layout-level validation, chip-level implementation, and experimental hardware testing to further evaluate performance under real-world conditions and optimize the design for advanced analog signal processing applications.

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