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HEURISTIC APPROACH IN RING VOLTAGE CONTROLLED OSCILLATOR DESIGN FOR V.C.O. BASED ANALOG TO DIGITAL CONTERTERS

BY

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Abstract. This paper introduces a procedure that relies on Computer Aided Design tools (industry compatible SPICE simulator and MATLAB) to get a first rapid design solution for a ring voltage controlled oscillator (VCO) that can be further analyzed and optimized for usage in a VCO based analog to digital converter (ADC). Due to the fact that linearity is a key performance metric of an ADC a special attention will be given to this characteristic during the design and for this matter control mechanism will be analyzed. To exemplify the design procedure two different delay cell topologies (simple inverter and pseudo-differential cross-coupled inverters) will be analyzed and designed in a 130 nm CMOS technology.

Keywords: CMOS; VCO; VCO ADC; nonlinearity; CAD design.

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1. Introduction

Nowadays global trends of digitalization, electrification of cars, autonomous driving, IoT etc. push integrated circuits specifications - energy efficiency, power supply level, area - to their limits. Therefore, in the attempt to design a circuit that will better suit the specifications new paradigms appear or even old ones (Hovin *et al*., 1997) find a better implementation in current context. One idea from the latter category brings back to life time-encoding analog to digital converters (ADCs).

In a few words, these ADCs take advantage of fast switching times in short channel technology nodes (less than 180 nm) - which create higher accuracy in time - and use time related quantities - frequency, phase - to encode information (Kim *et al*., 2010; Zhong and Sun, 2022).

At the core of these ADCs stand ring controlled oscillators - either by voltage or by current - that have a digital like topology (the simplest one being a chain of inverters) and digital like output waveforms. This fact enables a mostly digital implementation of an ADC that comes with benefits of voltage supply scaling (Gielen *et al*., 2020a, b). Even though delay cell structure can be as simple as a basic inverter their time delay modelling for an analog behaviour (needed to design a voltage controlled oscillator, VCO) can became too tedious for rapid and precise enough hand calculations (Abidi, 2006).

Therefore, in this work it is firstly presented a method that allows to get a bird's eye view of how design parameters influence tuning curve and biasing of two ring oscillators. In the ending part of the paper, using the characterization already proposed, an analysis of the nonlinearity of voltage controlled oscillators will be performed.

2. Characterization of Ring VCO Tuning Curve

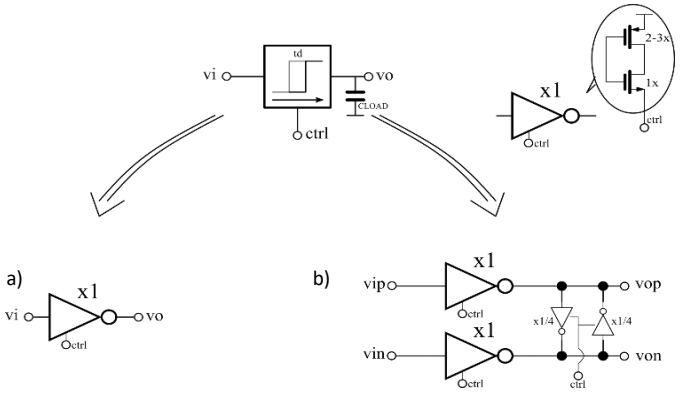


Fig. 1 − a) simple inverter as a delay cell; b) pseudo-differential cross-coupled inverters as delay cell.

Due to their compatibility with the philosophy of mostly digital circuitry and supply voltage scaling required by VCO based ADCs two different delay cells were chosen for analysis: a simple inverter and pseudo-differential cross-coupled connected inverters (Borgmans *et al.*, 2021). As highlighted by Borgmans et al. it is advisable to make a simple but intuitive analysis of the working of cells in Fig. 1. In this way it can be observed that it is expected that delay of cells (τ_d) to depend: directly proportional with loading capacitance (C_{LOAD}) from each node and voltage drop across entire ring (V_{RING}) and inversely proportional with current that drives the ring (I) (Borgmans *et al.*, 2021).

$$\tau_d \sim \frac{C_{LOAD} \cdot V_{RING}}{2 \cdot I} \tag{1}$$

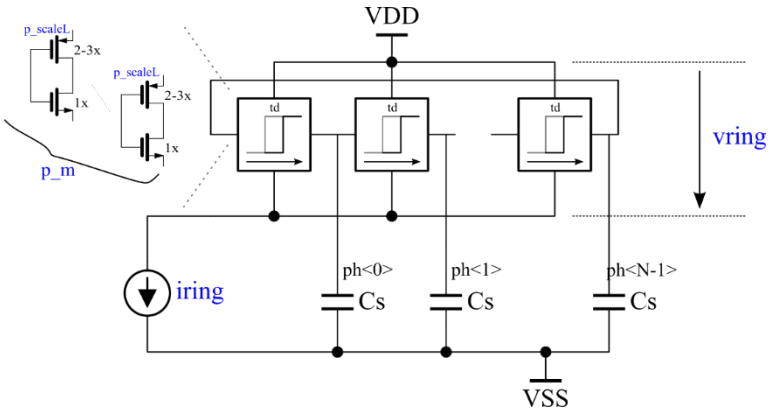


Fig. 2 − Ring oscillator architecture used for transistor level characterization.

Generically speaking these delay cells can be placed in a ring oscillator with architecture presented in Fig. 2 where additional capacitance is added to account for wiring and buffers used to connect to digital circuits. Each delay cell will have two parameters: *p_m* – representing the number of delay cells in parallel – and *p_scaleL* – that will control the channel length of both n-type and p-type transistors, specifying by how many times is higher than minimum length. To be noted are also quantities *iring* and *vring* that are the quasi-static current through ring and, respectively, quasi-static voltage across it. This architecture was easily implemented at transistor level and parametric simulations were performed for both delay cells.

Results were saved in a file compatible with MATLAB tool and postprocessed resulting graphs from Fig. 3 and Fig. 4. By investigation of data from graphs below one can observe that intuition regarding delay cells is verified. Load capacitance in nodes increases time delay of cells and as a consequence the frequency of oscillation is decreasing. In both figures it can be seen that for same control current, as we increase number of cells in parallel (through *p_m*) or

channel length of transistors (through *p_scaleL* – each column from figures has different factor of multiplication), frequency of oscillation reduces. Also, for same parametrization (*p_m* and *p_scaleL*) when current is increased oscillation frequency also has a positive variation, confirming that delay of a cell is inversely proportional to control current.

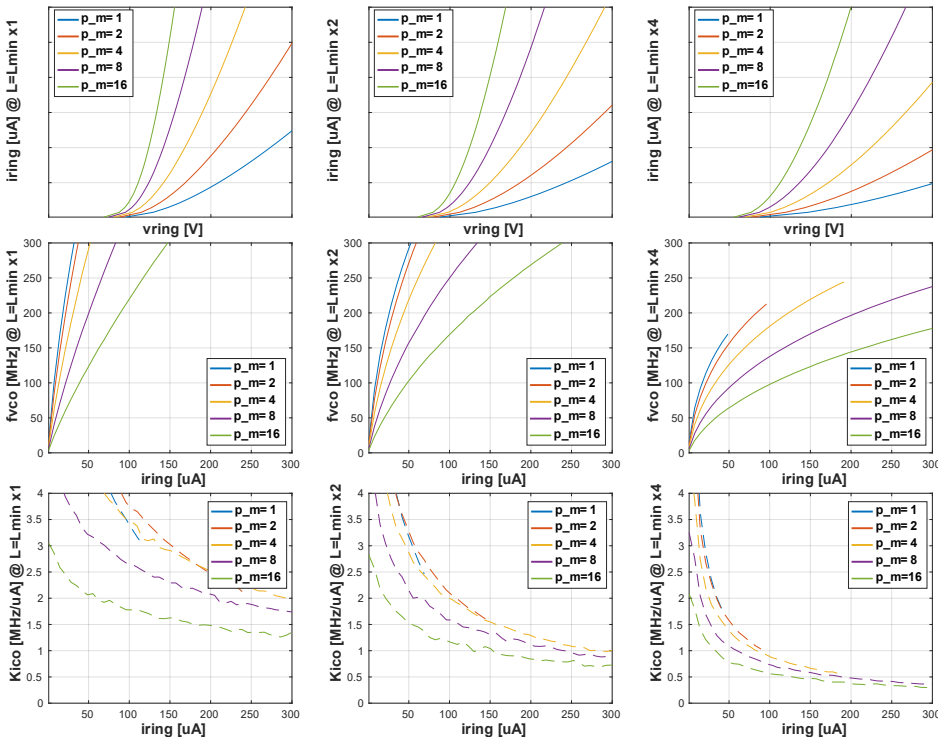


Fig. 3 – N=15 stage ring oscillator with simple inverter characterization; Data postprocessed with MATLAB: first row presents I-V characteristics of ring oscillator, second row presents tuning curve, third row outlines first derivative of frequency with respect to control current.

I-V characteristics is similar with a FET diode which is consistent with previous findings (Borgmans *et al.*, 2021). Having information laid out in this format helps the designer to orient himself when requirements for control current source are derived. First rows from Fig. 3 and Fig. 4 indicate maximum voltage drop on ring and by knowing supply voltage then the headroom available for control current source is determined.

As highlighted earlier one key performance parameter of the VCO is its linearity. Simulations done for both delay cells show clearly that tuning curve of the oscillator is highly nonlinear, especially for larger area implementation of

delay cells. In next section this comportment will be addressed and a transistor level voltage-to-current converter will be designed.

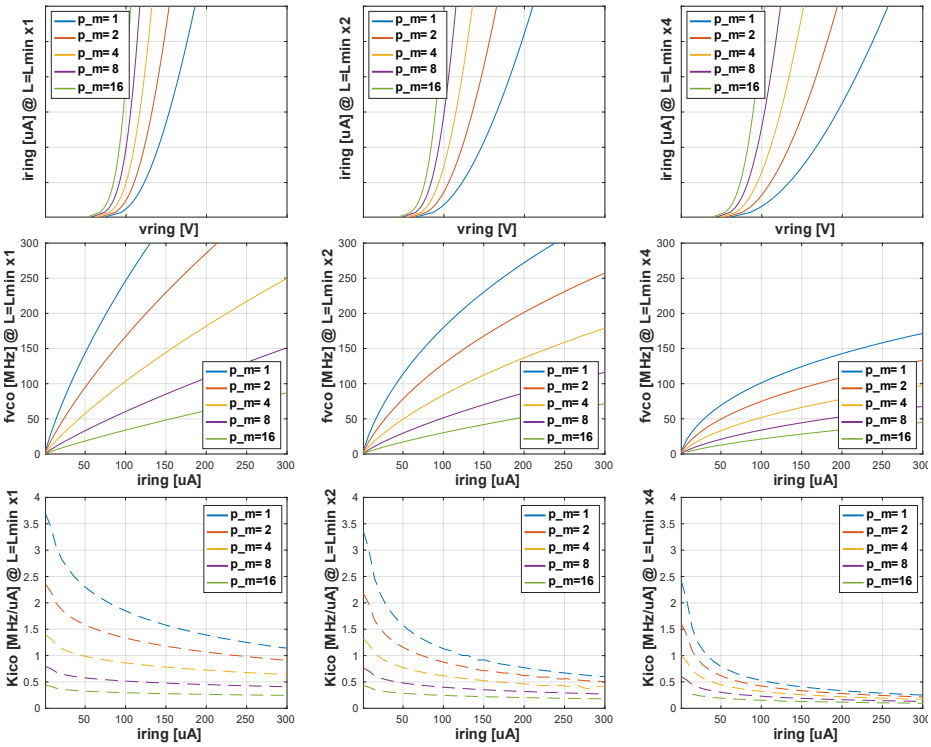


Fig. 4 – N=15 stage ring oscillator with pseudo-differential cross-coupled inverters characterization; Data postprocessed with MATLAB: first row presents I-V characteristics of ring oscillator, second row presents tuning curve, third row outlines first derivative of frequency with respect to control current.

3. Nonlinearity Study of Ring VCO

Study of ring VCO nonlinearity is made more efficient by data previously generated. VCO oscillating frequency *fvco* dependency on control current *iring* can be found in Fig. 3 and Fig. 4. Based on this information a transconductor can be designed to meet requirements of VCO to be used in ADC: *KVCO* – voltage-to-frequency gain, f_0 – free-running frequency and *ftune* – frequency range around f_0 for which oscillator control is linear.

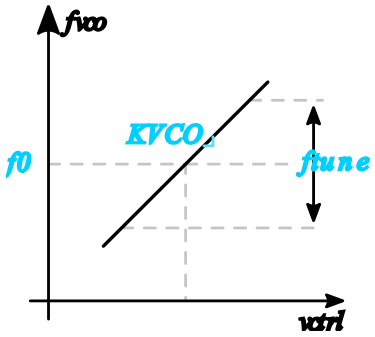


Fig. 5 – Ideal tuning curve of a voltage controlled oscillator.

In same philosophy of heuristic approach for design it can be noted that control characteristic of simulated ring oscillators has a form that resembles that of a power function, Eq. (2). Therefore, we propose to use curve fitting tool from MATLAB to find *a* and *b* parameters for equation that will describe frequency variation and will also be further used to faster design the required transconductor without performing long simulation with entire circuit.

$$fvco = a \cdot iring^{b} \tag{2}$$

Remark must be done that determined parameters *a* and *b* will only help at generating a function that is valid in the range of the data set available. Also function found through curve fitting has approximation errors, as it can be seen in Fig. 6, that will impact linearity results.

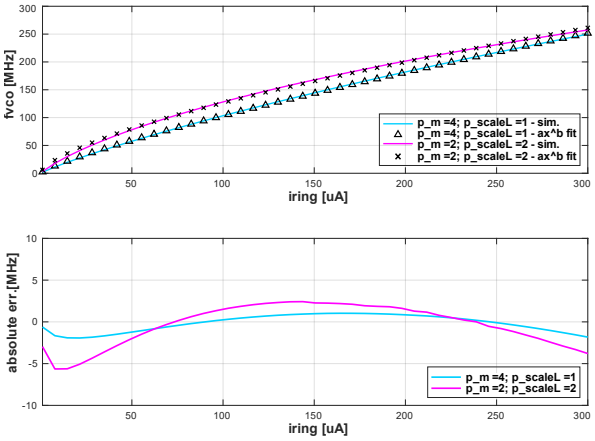


Fig. 6 – Curve fitting of current control characteristics with cross-coupled inverters.

One classic approach to linearize a system response is to use inverse function of a nonlinear block in cascade with it. Same strategy is studied in this work, aiming to design a VCO with: *KVCO* = 256 [MHz/V], f_0 = 150 [MHz] and *ftune* = 200 [MHz]. For implementation it was chosen a 15-stage ring oscillator with pseudo-differential cross-coupled inverters and design parameters *p_m* = 4 and *p_scaleL* = 1. Current control characteristics for this configuration is described in Fig. 6 and inverse function used for linearization is given by Eq. (3).

$$iring = \left(\frac{KVCO}{a}(vctrl\text{-}v0)\right)^{\frac{1}{b}} \tag{3}$$

where *vctrl* is the control voltage of the oscillator and *v0* is a constant voltage approximately equal to threshold voltage of the transistor used to implement the equation (M0 from Fig. 7).

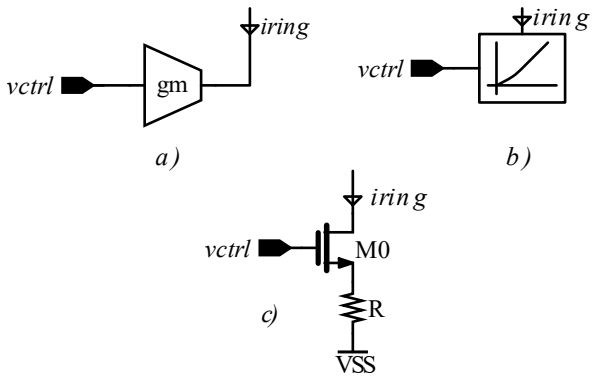


Fig. 7 – Transconductors used to control ring oscillator: a) nonlinearity uncompensated gm-stage, b) behavioural current source with imposed nonlinearity, c) transistor level nonlinear gm-stage.

To highlight transistor level implementation strengths and limitations, design was done with all transconductors presented in Fig. 7. Analysing results of simulations from Fig. 8 the following can be noted: using a nonlinearity uncompensated gm-stage will, as expected, have same performances as current related control characteristics; behavioural current source with imposed nonlinearity has its linearity performance limited to accuracy of approximation done by curve fitting (Fig. 6); transistor level nonlinear gm-stage improves performance only at low frequencies. Considering an accepted relative error of gain variation of +/- 10 [%], it can be seen that dynamic range of [-0.2, 0.3] [V] (that would be obtained with an uncompensated gm-stage) extends to [-0.45, 0.25] [V]. At frequencies around f_0 it can be observed that nonlinearity is not

compensated by inverse function, in fact it indicates that source degenerated stage operates linearly in that range.

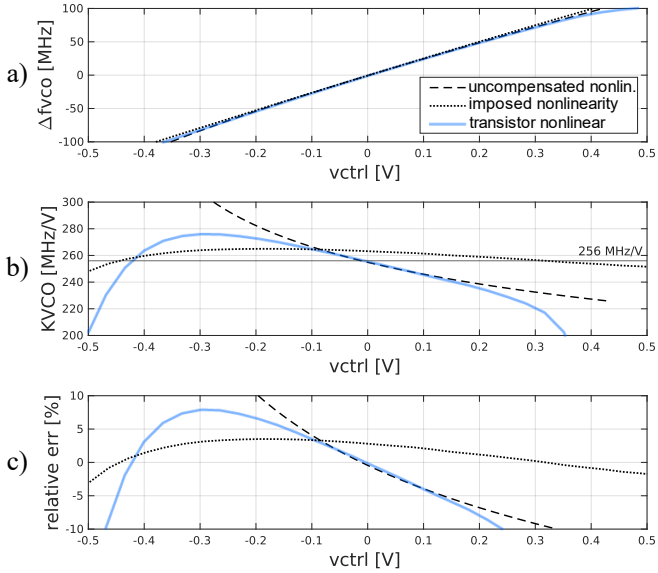


Fig. 8 – Simulation of N=15 stage ring oscillator with pseudo-differential cross-coupled inverters with control circuits from Fig. 7: a) frequency of VCO around f_0 =150 [MHz], b) *KVCO* graph, c) relative error between target *KVCO* of 256 [MHz/V] and simulated one.

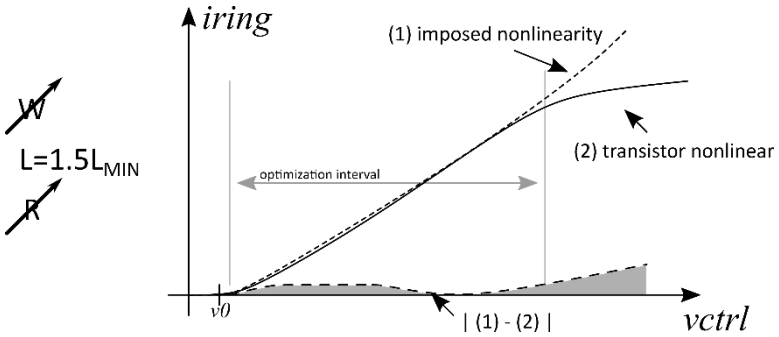


Fig. 9 – Design of transistor level transconductor using an optimization algorithm.

Transistor level transconductor was designed with available circuit simulator and optimization algorithm within environment (Fig. 9). Therefore, according to Eq. (3) a target behavior of current was modeled. Through a D.C. sweep simulation *iring* current of the transconductor (from Fig. 7c) was obtained and absolute error between these two was calculated. Objective of the

optimization algorithm was set to minimize area under absolute error's graph while adjusting width of transistor (*W*) and electrical resistance (*R*) of degeneration resistor.

4. Conclusions

A heuristic approach that allowed understanding performances of two ring oscillators – designed in a 130 nm CMOS technology – was presented. As highlighed in introduction, section 2 presents a systematic way to use simulator and MATLAB scripting to extract information on how I-V characteristics and frequency-to-control current characteristics are influenced by sizing of the delay cells. In section 3, based on data extracted with previously presented method, a study of linearity achieved with predistortion of control current was performed. Transistor level implementation, in comparison with a perfectly linear control, has a voltage related tuning curve with better linearity performance at low frequency. Its relative error is within 10% with *vctrl* up to -0.45 [V], while a linear transconductor would exceed this limit at *vctrl* around -0.2 [V].

For further improvements, as literature suggests (Borgmans *et al*., 2021), input equivalent noise estimations can be added to graphs as they depend on ring oscillator I-V function's derivative and sizing of transistors. Also, *a* and *b* coefficients' dependence on *p_m* and *p_scaleL* parameters should be studied to create a complete model of current related tuning curve.

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ABORDARE EURISTICĂ ÎN PROIECTAREA OSCILATORULUI CONTROLAT ÎN TENSIUNE PENTRU CONVERTOARE ANALOG-NUMERICE BAZATE PE O.C.T.

(Rezumat)

Această lucrare introduce o procedură care se bazează pe unelte de Proiectare Asistată de Calculator (simulator SPICE utilizat în industrie și MATLAB) pentru a obține o soluție rapidă de proiectare a unui oscilator controlat în tensiune (OCT), care poate fi analizat și optimizat pentru utilizarea în convertoare analog numerice bazate pe OCT. Pentru că liniaritatea este o metrică de performanță importantă a unui convertor, se va acorda o atenție deosebită acestui parametru în timpul proiectării. Pentru a exemplifica procedura de proiectare două topologii diferite pentru celulele de întârziere (un inversor simplu și inversoare cuplate pseudo-diferențiale) vor fi analizate și proiectate într-o tehnologie CMOS de 130 nm.